

# Improved MOSFET Short-Channel Device Using Germanium Implantation

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**Abstract**—Germanium doping in silicon tends to suppress any enhancement in dopant diffusion due to excess point defects. By performing a dual implantation of germanium and the normal source-drain dopant, lateral diffusion of the source-drain profile can be controlled, thus resulting in improved short-channel device behavior.

## I. INTRODUCTION

AS MOSFET gate dimensions are reduced, it becomes necessary to scale the device oxide thickness and source-drain junction depth in order to maintain constant electric fields in the device. As the source-drain junction depth is reduced, short-channel behavior is improved since the threshold voltage becomes less dependent on gate length and the subthreshold currents are lowered due to a reduction in subsurface channel conduction.

Germanium doping in silicon has been shown to lower the number of silicon point defects in the wafer, and thereby reduce the diffusion of dopants [1]. Pfiester and Griffin [1] showed that the normal phosphorus kink and tail are absent when high concentration phosphorus is co-diffused with germanium. In this study, germanium implantation is performed to reduce the diffusion of a source and drain dopant and to improve the short-channel device characteristics.

## II. PROCESS FABRICATION AND ANALYSIS

The test devices were fabricated in a p-type wafer with resistivities of  $14 \Omega \cdot \text{cm}$ . A  $175\text{-}\text{\AA}$  gate oxide was thermally grown followed by the deposition of a  $500\text{-}\text{\AA}$  layer of undoped polysilicon. A shallow boron channel implant was used to adjust the long-channel threshold to  $0.75 \text{ V}$ . A second deposition of  $3000 \text{ \AA}$  of undoped poly was then performed. The overlap capacitance was minimized by using  $1000\text{-}\text{\AA}$  oxide sidewall spacers which were formed by depositing  $1300 \text{ \AA}$  of undoped oxide and reactive ion etching. The source-drain regions were then thermally reoxidized to grow a  $200\text{-}\text{\AA}$  implant screen oxide layer.

At this point in the fabrication, two splits on the source-drain implantation were performed. The first set received a phosphorus implant of  $2.5 \cdot 10^{15}/\text{cm}^2$  at an energy of  $45 \text{ keV}$ . The second set received the same phosphorus implant as well as a prior  $5.0 \cdot 10^{15}/\text{cm}^2$  germanium implant at  $125 \text{ keV}$ . Both

sets of wafers then received a furnace anneal of  $12 \text{ min}$  at  $900^\circ\text{C}$ . Finally, both sets received a deposition of LTO oxide, contact, and metal definition to complete the processing.

As was shown by Pfiester and Griffin [1], the germanium implantation reduces the phosphorus tail diffusion of a high-concentration phosphorus dose. As shown in Fig. 1, the spreading resistance measurement with the germanium implant results in a shallower junction depth with no enhanced tail diffusion. These one-dimensional profiles are fit with SUPREM-IV [2] to account for the anomalous diffusion effects in the structure. For the germanium-doped junction, the phosphorus diffusivity was enhanced by a factor of  $7.5$  to account for the transient damage annealing. For a low-temperature short-time anneal the transient damage enhancement can be significant, and has been modeled by an enhancement of the dopant diffusivity [3].

As suggested by Hu *et al.* [4], normal phosphorus diffusion can be treated as diffusing in two portions, one with interstitials and the other with vacancies. In order to simplify the model, no recombination was allowed between the interstitial and vacancy streams of the profile. The interstitial stream which forms the tail profile was calculated using an enhancement factor of  $60$ . Approximately  $12$  percent of the implanted dose was assumed to be diffusing with the enhanced diffusivity.

Fig. 2 shows SEM pictures of the devices for both device cross sections. The device cross sections were prepared using a standard Wright etch. Fig. 2(a) shows the cross section of a germanium-doped device and Fig. 2(b) shows one without the germanium. Both the SEM photographs and spreading resistance measurements indicate that the germanium reduces the phosphorus diffusion in both the lateral and vertical directions and produces shallower source-drain junctions.

## III. ELECTRICAL DEVICE MEASUREMENTS AND SIMULATIONS

The effective channel length was calculated using the method proposed by Suci and Johnston [5] which is based on peak transconductance measurements that are corrected for the series resistance and vertical mobility reduction. The germanium-implanted devices showed an effective channel length that was consistently  $1500 \text{ \AA}$  greater than the phosphorus-only implanted devices for the same drawn channel length. This result is consistent with Fig. 2 which showed less lateral diffusion for the germanium-implanted devices. The MOSFET series resistance was  $33$  and  $46 \Omega$  for the phosphorus and germanium/phosphorus source-drain structures. This resulted in a drain saturation current with  $V_{DS} = V_{GS} = 5 \text{ V}$  of  $18.1$

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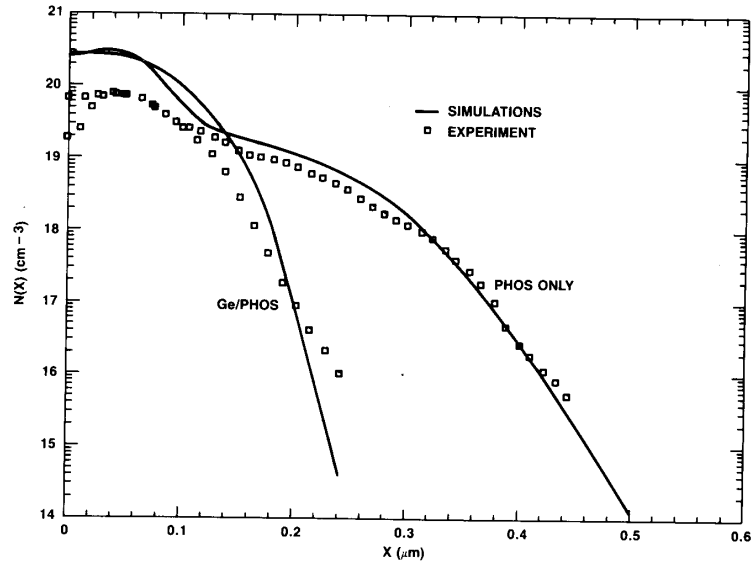


Fig. 1. Spreading resistance measurements and simulated profiles for both Ge/P and P-only junctions.

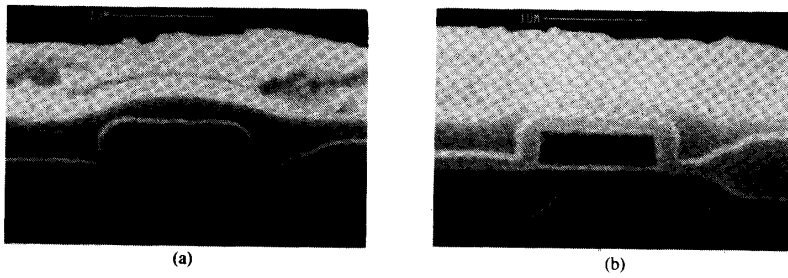


Fig. 2. SEM cross sections of both the (a) Ge/P and (b) P source-drain devices.

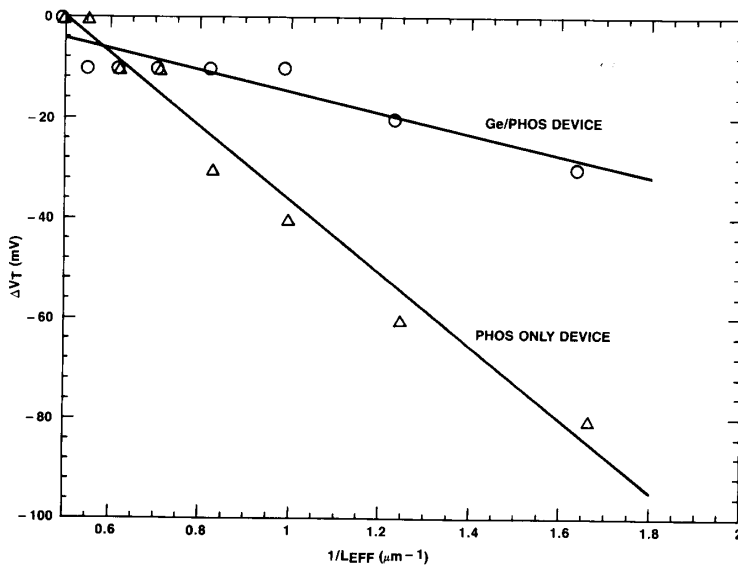


Fig. 3. Threshold-voltage shift as a function of the inverse electrical channel length.

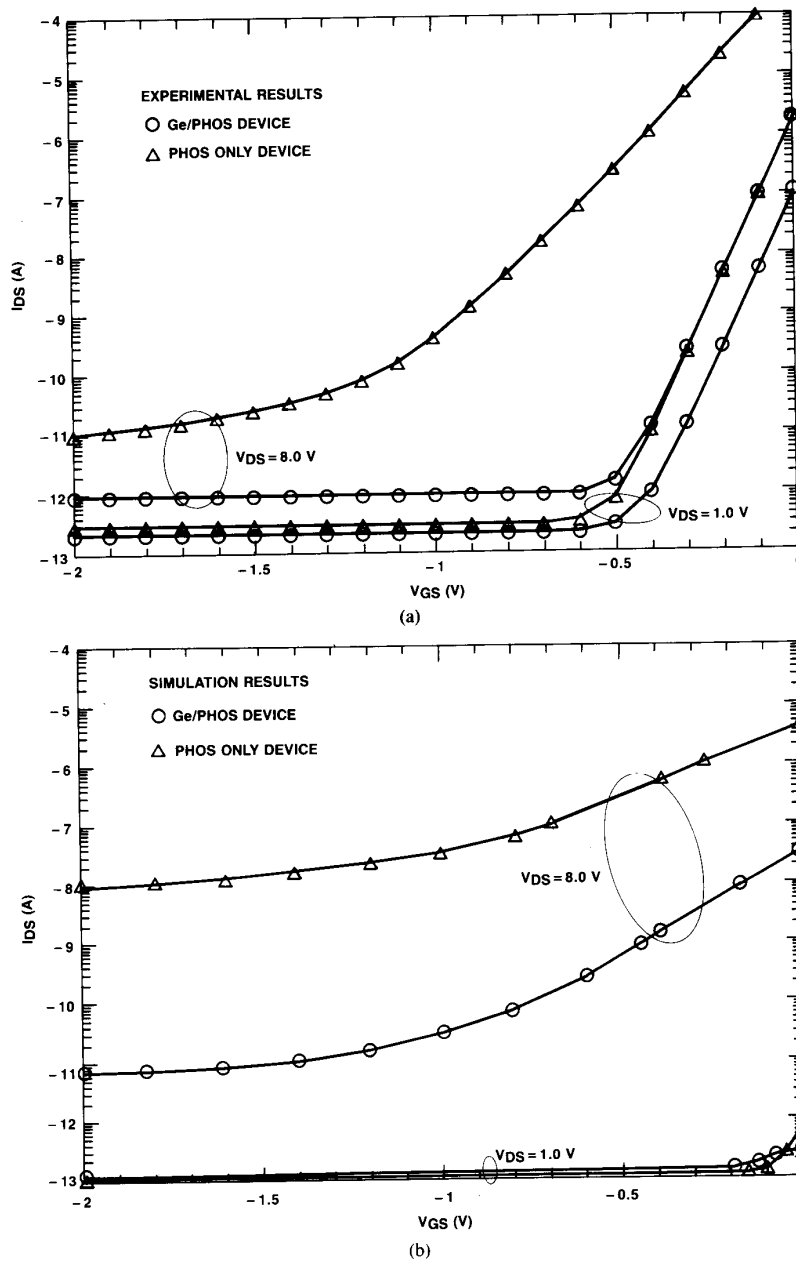


Fig. 4. Subthreshold current for both types of NMOS devices as a function of gate voltage: (a) measured currents, and (b) simulated result. The effective channel length for both device types is  $0.73 \mu\text{m}$ .

and 17.2 mA for the corresponding  $0.73\text{-}\mu\text{m}$  channel length devices.

The threshold-voltage shift with  $V_{DS} = 0.1$  V as a function of the inverse effective channel length is shown in Fig. 3. The devices with the germanium implant show less of a dependence on channel length than the junctions with only phosphorus. Based on a simple model for threshold-voltage dependence on channel length [6], the threshold-voltage shift is a function of the junction depth of the source and drain. The data indicate that the junction depths are smaller for the germanium-implanted devices.

Fig. 4(a) shows the measured subthreshold drain currents for a  $0.73\text{-}\mu\text{m}$  channel length NMOS transistor as a function of the  $V_{GS}$  for both the germanium/phosphorus devices and the phosphorus-only devices. With a  $V_{DS}$  of 1.0 V, there is little difference in the subthreshold current. For a  $V_{DS}$  of 8.0 V, there is a large difference between the two sets of devices since most of the current is flowing below the surface. In this regime of operation, the subthreshold drain current is very sensitive to the source-drain junction depth. Consequently, the germanium/phosphorus-implanted devices exhibit improved short-channel subthreshold behavior.

Simulations of the data were done using SUPREM-IV to generate doping profiles for PISCES [7], which was used to calculate the subthreshold current. The results of this calculation, shown in Fig. 4(b), show the same behavior as the experimental devices. Although the agreement is not quantitatively correct, the simulations verify that the subsurface current flow is smaller in the germanium/phosphorus co-diffused source-drains due to a shallower junction depth.

The quality of the source-drain junction was not significantly degraded by the germanium implantation. The room-temperature reverse leakage currents at 5 V were similar for both junction types and were measured to be less than 10 nA/cm<sup>2</sup> and 10 pA/cm for the area and edge components, respectively. The corresponding sheet resistance measurements were 57.5  $\Omega$  and 73.1  $\Omega$  for the phosphorus and germanium/phosphorus junctions.

#### IV. CONCLUSION

In summary, germanium/phosphorus co-implantation has been shown to result in shallower source-drain junctions than phosphorus implantation alone. Improvements in short-channel behavior occur as a result of the shallower junctions. The

germanium/phosphorus devices show less threshold-voltage dependence on channel length as well as reduced subthreshold current. In addition, no significant degradation to the source-drain junction quality was observed.

#### REFERENCES

- [1] J. R. Pfister and P. B. Griffin, "Anomalous co-diffusion effects of germanium on group III and V dopants in silicon," *Appl. Phys. Lett.*, vol. 54, no. 6, p. 471, Feb. 8, 1988.
- [2] M. E. Law, C. S. Rafferty, and R. W. Dutton, "New N-well fabrication techniques based on 2D process simulation," in *IEDM Tech. Dig.* (Los Angeles, CA), Dec. 1986, p. 518.
- [3] R. B. Fair and J. E. Rose, "A deep decision tree approach to modeling submicron silicon technologies," presented at the Int. Conf. Computer Aided Des., Santa Clara, CA, Nov. 1987.
- [4] S. M. Hu, P. Fahey, and R. W. Dutton, "On models of phosphorus diffusion in silicon," *J. Appl. Phys.*, vol. 54, no. 12, p. 6912, Dec. 1983.
- [5] P. I. Suci and R. L. Johnston, "Experimental derivation of the source and drain resistance of MOS transistors," *IEEE Trans. Electron Devices*, vol. ED-27, p. 1540, 1980.
- [6] L. Yau, "A simple theory to predict the threshold voltage of short channel IGFET's," *Solid-State Electron.*, vol. 17, p. 1059, 1974.
- [7] C. S. Rafferty, M. R. Pinto, and R. W. Dutton, "Iterative methods in semiconductor device simulation," *IEEE Trans. Computer-Aided Des.*, vol. CAD-4, no. 4, p. 462, Oct. 1985.