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# NOTES

## INFLUENCE OF A SELECTIVELY ION-IMPLANTED COLLECTOR ON BIPOLAR TRANSISTOR ELECTRICAL CHARACTERISTICS

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### NOTATION

| | |
|---|---|
| $\beta_{d.c.}$ | d.c. collector current gain |
| $f_t$ | maximum cut-off frequency |
| $V_{CE}$ | collector–emitter voltage |
| $V_A$ | Early voltage |
| $V_{CB}$ | collector–base voltage |

### 1. INTRODUCTION

With the development of double-polysilicon, self-aligned bipolar technology, the lateral feature size of bipolar transistors has been scaled down. This reduces the parasitic capacitance and resistance, and leads to improved device performance. To get further improvement in device speed, a corresponding scaling of the vertical feature size is necessary. However, progress in vertical scaling is difficult to achieve. As a result of B-channeling during the intrinsic base formation, it is virtually impossible to avoid the undesired spreading of base profile. Worse, the channeling becomes more significant when the implantation energy is low, which means control of the B-ion-implantation becomes even more critical in the fabrication of modern shallow-base, high-speed bipolar transistors. To overcome this difficulty, a new process technology, Selectively ion-implanted collector (SIC), has been proposed[1,2].

During the fabrication of a bipolar transistor, P-ions are implanted into the epi-collector region near the collector–base junction after the formation of the intrinsic base, and form a high-concentration collector layer. This implantation is self-aligned to the intrinsic base implant, and consequently is localized to the intrinsic base–collector junction. This offers a lower parasitic capacitance than an increase in the epi-doping level.

The purpose of this work is to explore the influence of the SIC implantation energy and dose on device performance. The MOSAIC-3[3] process was simulated using SUPREM-III[4] and a SIC step was added. The implantation energy and dose were varied, and the resulting profiles were used as input to PISCES-II[5]. The simulations were of the intrinsic device only and did not include the parasitic resistance and capacitance associated with the base, collector and emitter contacts.

### 2. DEVICE PERFORMANCE

As expected, the d.c. peak current gain ($\beta_{d.c.}$) increases with more compensation of the intrinsic base. In general, the highest gain is found for the lowest energy and highest dose, which is due to the base compensation and reduction of the base Gummel number. A 70% improvement is possible with a dose of $10^{13}\,cm^{-2}$ and an energy of 250 keV. The maximum cut-off frequency ($f_t$) as a function of energy and dose is shown in Fig. 1. Since the SIC layer shortens the base width without adding significantly to the capacitance, $f_t$ is larger for smaller energies and higher doses. Again, since the primary effect is due to compensation of the base, there is an energy–dose tradeoff. For a given dose, an energy can be chosen which matches the $f_t$ of a transistor with higher dose and smaller energy. A SIC layer of $10^{13}\,cm^{-2}$ and 250 keV results in an improvement of 90% in $f_t$.

The SIC step also limits the high current effects. The heavier doping beneath the base delays the onset of base widening. Figure 2 shows the collector current at maximum cut-off frequency. In general, the collector current maximum is increased for increasing SIC dose and increases for shallower implants. The maximum collector current is 70% higher than without a SIC at $10^{13}\,cm^{-2}$ and 250 keV. Without any additional mask steps, the SIC can result in improvement in the current gain, maximum cut-off frequency and collector current at maximum cut-off. The SIC applicability will depend on the circuit application, as the drawbacks are specific to the application circuit. This is explored more in the next section.

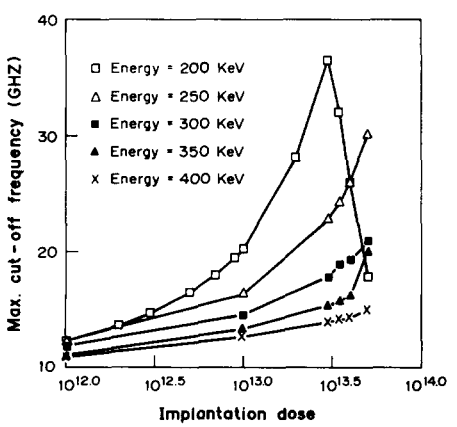


Fig. 1. Maximum cut-off frequency as a function of SIC implantation energy and dose.

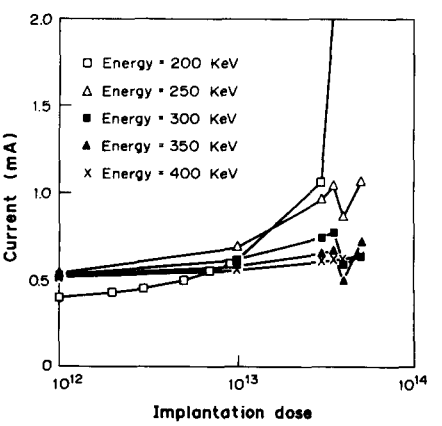


Fig. 2. Collector current at maximum cut-off frequency as a function of SIC implantation energy and dose.

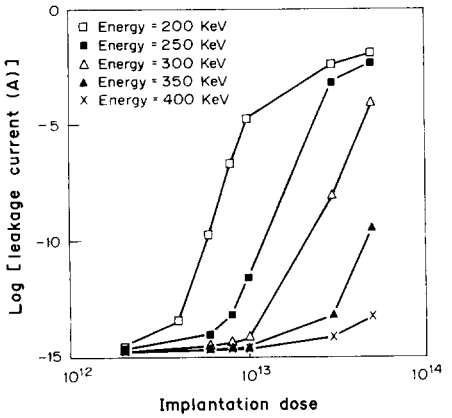


Fig. 3. Collector–emitter current with the base open at $V_{CE}$ = 5 V as a function of SIC implantation energy and dose.

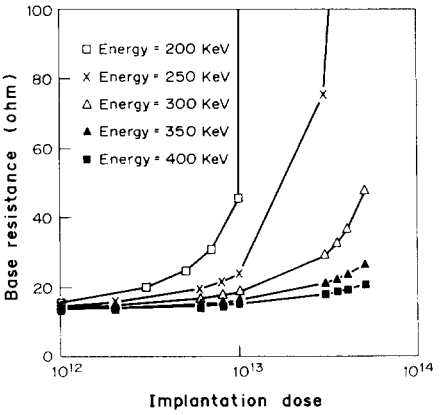


Fig. 4. Pinched base resistance for a 1 × 1 μm emitter as a function of SIC implantation energy and dose.

## 3. CIRCUIT APPLICATIONS OF THE SIC

### *3.1. Analog*

In typical analog applications, the circuit gain is determined, in part, by the output resistance of the bipolar device. In saturation, the dependence of the collector current upon $V_{CE}$ results from the basewidth variation due to the changing in the width of the collector–base space-charged region as a result of changing $V_{CE}$. As the doping is increased beneath the base layer, the basewidth is far more sensitive to changes in $V_{CE}$. Typical analog devices are designed with thick, lightly-doped epi-layers to minimize the effect of $V_{CE}$ on basewidth. Consequently, the SIC will substantially degrade the Early voltage, $V_A$. The MOSAIC process used as a base for this study is a digital process and does not have a good Early voltage without the SIC step. The Early voltage is reduced from 37 to 5.3 V for a SIC dose of $10^{13}$ cm$^{-2}$ and energy of 250 keV. In general, the SIC will not be of benefit to analog applications.

### *3.2. BiCMOS digital*

Roseel and Dutton[6] showed that the BiCMOS gate delay is dominated by a term from the MOS transistors and the base transit time of the bipolar device. The base transit time is the dominant delay component of the maximum cut-off frequency, and therefore the SIC should improve BiCMOS gate performance substantially. However, if the SIC energy is too low or the dose too high, the device will punch through and this limits the maximum SIC that can be used. Until the onset of punch through, however, the device performance continues to increase. Figure 3 shows the emitter–collector current at a collector–emitter voltage of 5 V and the base open as a function of the SIC implant energy and dose. This current could limit the applicability of BiCMOS in a logic setting by changing the final logic levels and by increasing the overall chip power dissipation. An open-base current of under one nanoampere can be achieved with a SIC dose of $10^{13}$ cm$^{-2}$ and an energy greater than 250 keV.

### *3.3. ECL bipolar circuits*

In ECL circuits, the gate performance is limited by the base transit time and the base resistance. The base transit time is decreased, but the base resistance is also increased. Figure 4 plots the pinched base resistance as a function of the SIC dose and energy. The base resistance was computed with $V_{CB}$ set to zero and a small potential applied across the base layer. As is expected, the base resistance is increased when the SIC has a large dose or a low energy, and is nearly doubled for a $10^{13}$ cm$^{-2}$ dose and an energy of 250 keV. However, the value of the computed base resistance is rather small and will be dominated by parasitics. A SIC process step is likely to improve the performance of ECL circuits.

## 4. SUMMARY AND CONCLUSION

The influence of a SIC on bipolar device electrical characteristics has been examined by computer simulation. It is shown that the SIC structure achieves improvement in d.c. current gain, cut-off frequency and current drive at high frequency. There are some drawbacks associated with the technique. For analog circuit applications, the Early voltage is substantially reduced. In BiCMOS applications, the primary limiting factor is the collector–emitter current with the base open. In ECL circuits, the base resistance is increased. The same performance levels can be achieved across a wide range of doses and energies by increasing the energy with increasing dose. Choosing the SIC implantation dose and energy is a compromise between the advantages and disadvantages in device performance for a specific application. In these simulations, the proper choice of implantation dose and energy leads to over 80% improvement in current gain and cut-off frequency. The SIC is recommended for BiCMOS processes and ECL digital applications, but not analog applications due to the decrease in Early voltage.

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