Effect of implant temperature on dopant diffusion and defect morphology for Si implanted GaAs

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Experimental observations of dopant diffusion and defect formation are reported as a function of implant temperature in Si implanted GaAs. The diffusion of Si during post-implant annealing decreases by a factor of 2.5 as the implant temperature increases from -2 to 40 °C. In this same temperature range, the maximum depth and density of extrinsic dislocation loops increase by factors of 3 and 4, respectively. Rutherford backscattering channeling measurements indicate that Si implanted GaAs undergoes an amorphous to crystalline transition at Si implant temperatures between -51 and 40 °C. A unified explanation of the effects of implant temperature on both diffusion and dislocation formation is proposed based on the known differences in sputter yields between crystalline and amorphous semiconductors. The model assumes that the sputter yield is enhanced by amorphization in the lower temperatures, thus increasing the excess vacancy concentration. Estimates of excess vacancy concentration are obtained by simulations of the diffusion profiles and are quantitatively consistent with a realistic sputter yield enhancement.

I. INTRODUCTION

Increasing the reliability and yields of GaAs and other III-V devices requires accurate knowledge and control of doping profiles. As device dimensions shrink, increasingly shallower junction depths and tighter control of channel doping will be required, necessitating precise placement of dopant atoms. The most widely used n-type dopant for fabricating GaAs devices is ion-implanted silicon. The reasons for this are the lack of a viable Si solid source technology, the generally low diffusivity of implanted Si, its ease of implantation, and its relatively low mass, leading to smaller implant damage effects. Unfortunately, the diffusion of silicon has been found to vary over a large range of values, depending on processing conditions.[1-5] These process conditions are often not well controlled, leading to large variations in reported diffusivities and anomalous diffusion behavior.[4]

Recently, Haynes and Holland reported dramatic variations in implant damage as a function of temperature for Si implanted GaAs.[6] For example, in 6×10^{14} cm^{-2} Si implants, the effective fraction of displaced atoms at the peak of the damage profile [from Rutherford backscattering (RBS) channeling measurements] decreased from 95% to 15% as the temperature was increased from 20 to 30 °C. For this reason,

the as-implanted defect morphologies of nominal "room temperature" Si implants into GaAs can vary dramatically. Moreover, the diffusion of implanted Si has been found to increase with decreasing implant energy, making shallow implants potentially more sensitive to implant temperature variations.[7,8] This variation in damage density with implant temperature may be responsible for much of the discrepancy in previous studies of implanted Si diffusion.

Another factor that has not been well understood is the effect, if any, of extended defects, primarily dislocation loops, on dopant diffusion. Allen *et al.* speculated that dislocation loops might be responsible for the variation in their diffusion data.[4] In a previous article, we reported correlations between loop density and Si diffusion and concluded that the loops were reacting to the same source of vacancies that were assisting the diffusion although the source of the additional vacancies was not identified.[7] In this article, we report on the effects of well controlled implant temperature variations on Si diffusion and defect morphology. A relationship between defect morphology, as given by RBS channeling and transmission electron microscopy (TEM), and Si redistribution is demonstrated. We estimate the excess vacancy concentration that is needed to explain the enhanced diffusion and show that sputtering, enhanced by amorphization at the lower implant temperatures, provides a plausible source for the required number of extra vacancies. The results of

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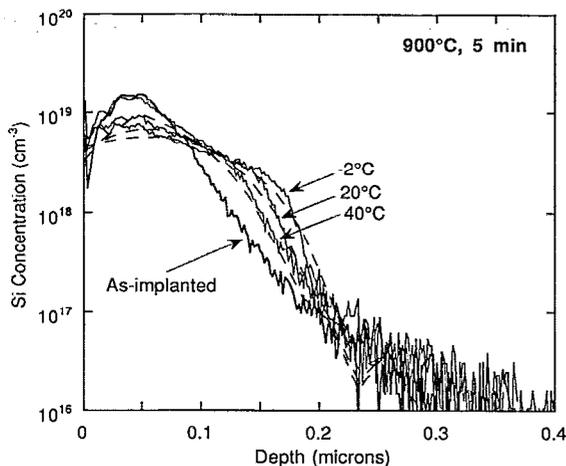
FIG. 1. SIMS profiles of as-implanted and annealed 40 keV, 1×10^{14} cm^{-2} Si implants. The annealed profiles and their SUPREM-IV.GS simulations (dashed lines) are labeled with the implant temperature. The SIMS profile of a sample implanted at 80 °C was similar to the 40 °C sample.
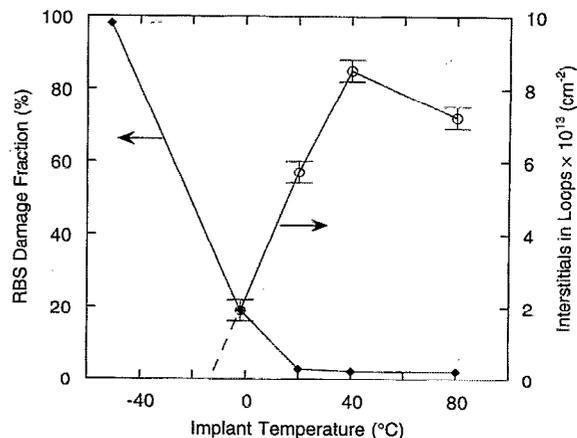

FIG. 2. Concentration of interstitials bound by type I dislocation loops and RBS damage fractions vs implant temperature. The bound interstitial concentrations were measured from the PTEM micrographs in Fig. 3.

this work provide a better understanding of the relationship between dopant redistribution and implant damage, and should improve the reliability and reproducibility of Si implants into GaAs.

II. EXPERIMENTAL PROCEDURE

⟨100⟩ semi-insulating LEC GaAs wafers were implanted at 7° off normal with 40 keV, 1×10^{14} cm^2 ^{29}Si$^+$ at implant temperatures of −51, −2, 20, 40, and 80 °C. The wafers were mounted to the wafer holder using silver paint and the temperature was controlled to within 2 °C. The current density for these experiments was 0.05 μA/cm^2. The as-implanted damage was characterized by RBS channeling measurements performed at room temperature. Prior to RBS measurement, the implanted samples were stored at 77 K to preserve the as-implanted damage. A 900 Å Si$_3$N$_4$ cap was deposited by plasma enhanced, chemical vapor deposition prior to furnace annealing at 900 °C. Dopant profiles were measured by secondary ion mass spectrometry (SIMS) at Charles Evans and Associates. Cross-sectional TEM (XTEM) samples were prepared by cutting strips, lapping, and Ar ion milling at room temperature. Plan-view TEM (PTEM) samples were jet etched using a 1:20 bromine-methanol solution. TEM observations were made using a JEOL 200CX and a JEOL 4000FX instrument. All micrographs were taken using bright-field, g_{220} two-beam conditions.

III. RESULTS AND DISCUSSION

A. Experimental results

Figure 1 shows SIMS plots of the redistribution of Si after annealing at 900 °C for 5 min for implants done at different temperatures. The box shaped profiles are indicative of a concentration or electron dependent diffusion coefficient. As the implant temperature is increased from −2 to 40 °C, the amount of diffusion decreases by a factor of 2.5.

Since Si diffusion in GaAs occurs via a vacancy-assisted mechanism,[4,9] the increase in diffusivity with decreasing implant temperature implies that the vacancy concentration is higher at lower implant temperatures. When the implant temperature was decreased to −51 °C, amorphization occurred during implantation and no diffusion was observed. For 30 min anneals, the Si diffusivity increased by a factor of 3 over the diffusivity at 5 min for all non-fully amorphized samples.[7] The higher temperature implants showed a greater increase in diffusivity than the lower temperature ones in this time period.

The RBS channeling yield of the as-implanted samples is also a strong function of temperature, as seen in Fig. 2. At temperatures above 40 °C, the yield is low, indicative of a crystalline lattice with minimal damage. As the temperature decreases from 40 to −2 °C, the damage fraction increases as isolated pockets of amorphous material form in the GaAs. At an implant temperature of −51 °C, the crystal forms a continuous amorphous layer with an average thickness of 450 Å. The surface of this channeling spectrum coincides with that of the random spectrum, indicating that the amorphous layer extends to the surface. The integrated damage profiles correspond to defect densities of 20, 4.0, 0.9, 0.6, and 0.6×10^{16} atoms/cm^{-2} for implant temperatures of −51, −2, 20, 40, and 80 °C, respectively. The channeling measurement becomes less sensitive at small point defect densities, however, so the small change in damage fraction between the 20 and 40 °C samples may represent a large difference in actual damage.

The as-implanted defect morphology, as revealed by TEM, shows a similar trend, as seen in Fig. 3. The as-implanted cross section of the −51 °C sample shows stacking faults and other defects indicating that an amorphous layer had formed and recrystallized. This recrystallization probably occurred during sample preparation. The −2 and 20 °C as-implanted samples exhibit "black dot" contrast, while no defects are visible in the 40 and 80 °C samples. Upon annealing, point defects in the crystalline samples coalesce into extrinsic, type I (subamorphization threshold) dis-
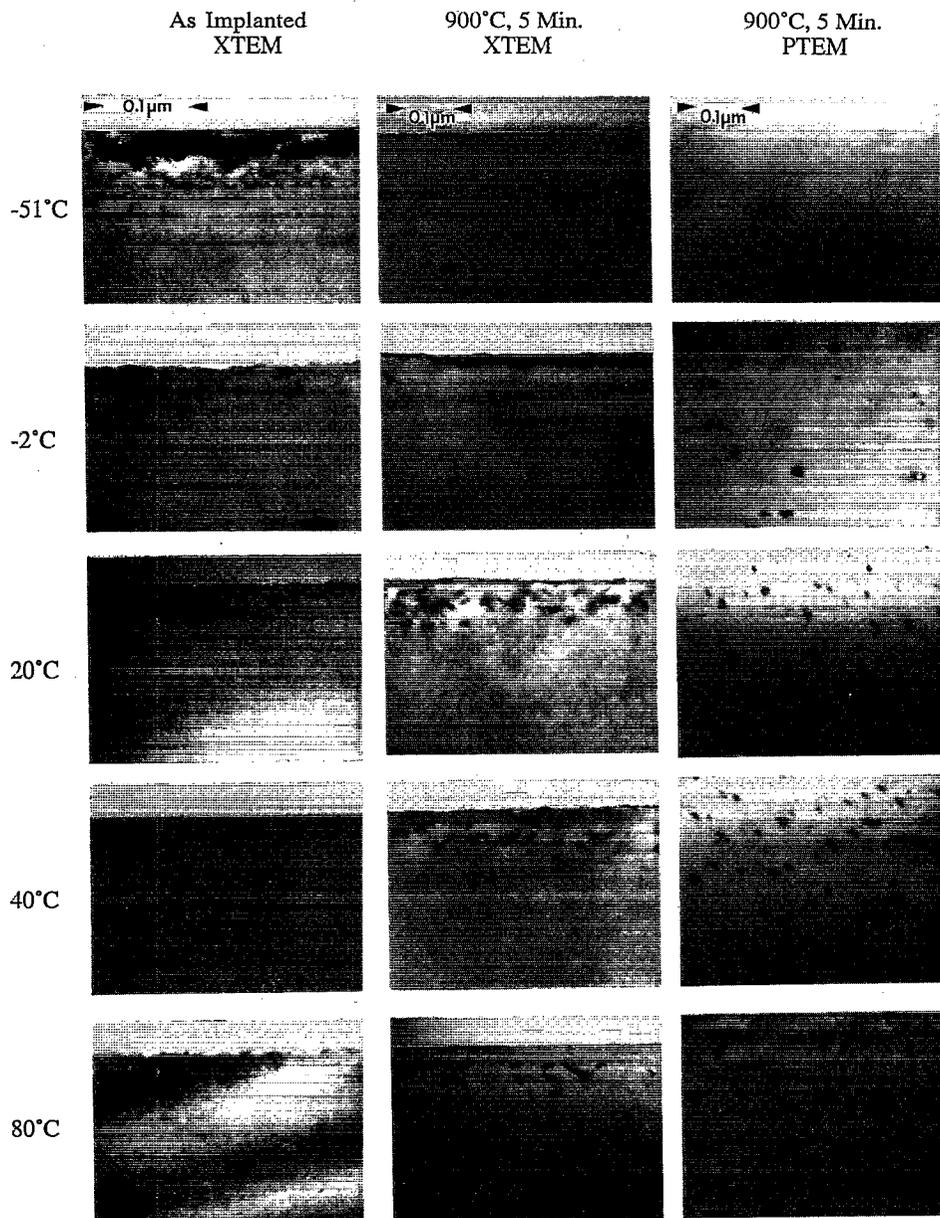
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| | As Implanted XTEM | 900°C, 5 Min. XTEM | 900°C, 5 Min. PTEM |

FIG. 3. Cross-sectional and plan-view TEM micrographs of as-implanted and annealed samples implanted at temperatures from −51 to 40 °C. Note the difference in scale of the as-implanted and annealed cross-sectional micrographs.

olocation loops, with the density and depth of the loops increasing with increasing implant temperature, as seen in Figs. 2 and 3. Type I loops do not form in the −51 °C implanted sample because it is amorphous. Type II (end of range) dislocation loops are also not present in this sample, consistent with previous observations that type II loops are not stable in GaAs.[10] After 30 min at 900 °C, the loops had annealed out of all samples.[7] Since extrinsic dislocation loops will dissolve in the presence of excess vacancies, this continues our earlier observations[7] which showed that both the enhanced diffusion and reduction in dislocation loop density in the lower temperature, partially amorphized implants (−2 and 20 °C) can be explained on the basis of a larger concentration of excess vacancies produced during implantation.

B. Simulation

To evaluate the changes in vacancy concentration required to affect Si diffusion by the amounts shown in Fig. 1, computer simulations using SUPREM-IV.GS,[11] a multi-purpose GaAs process modeling program and TRIM89,[12] a Monte Carlo ion implantation simulator, were performed. The TRIM simulations were used primarily to determine the depth range in which excess vacancies and interstitials are produced during Si implantation. The surface binding energy, displacement energy, and lattice binding energy were taken from the default values used in TRIM92 and set to 3.88, 15, and 1.0 eV, respectively. A TRIM simulation of 100 000 Si ions implanted at 40 keV into GaAs at 7° off axis was made. After adding the ion and Ga interstitial distributions (since most of the Si

is believed to occupy Ga sites), the excess vacancy and interstitial profiles were calculated by subtracting the total point defect profiles from one another. This results in a Ga vacancy rich surface layer to a depth of 200 Å, followed by a buried interstitial rich layer. In the SUPREM simulation, both the excess Ga vacancy and interstitial profiles were read into the simulator, along with the as-implanted Si profile from SIMS. The following parameters, based on previous studies of dopant diffusion in GaAs,[13] were used in the simulation: $C_V^* = 1 \times 10^{15}$ cm^{-3}; $C_I^* = 1 \times 10^{14}$ cm^{-3}; Kr.0 (interstitial-vacancy recombination rate)$=2.0 \times 10^{-15}$ cm^{-3}/s; $D_0(\text{Ga}_{\text{Vac}})=3.5 \times 10^{-12}$ cm^2/s; $D_0(\text{Ga}_{\text{int}})=1.0 \times 10^{-11}$ cm^2/s; $D(\text{silicon})=6.12 \times 10^{-18}$ $(n/n_i)^2$ cm^2/s. The diffusivity of silicon was chosen to correspond to the implanted value used in SUPREM-IV.GS at 900 °C,[11,14] but with an electron concentration squared dependence. This diffusivity is sufficiently small that no Si redistribution would occur during 5 min, 900 °C anneals in the absence of vacancy injection. All other parameters were left at their default values. The SIMS profile for each implant temperature was fit by adjusting the excess vacancy distribution until the simulated and experimental dopant profiles overlayed one another, as seen in Fig. 1. The effective vacancy "doses" needed to fit the −2, 20, and 40 °C annealed profiles were 2.3, 2.0, and 1.7×10^{14} cm^{-2}, respectively. The decrease in diffusivity in going from a −2 to a 40 °C implant is therefore caused by a 35% decrease in vacancies. The ~6×10^{13} cm^{-2} increase in vacancies at −2 °C as compared to 40 °C is the same as the number needed to dissolve the interstitial loops to the extent observed (see Fig. 2), lending quantitative evidence to the conclusion that the same source of vacancies affects both the diffusion and the change in loop density.

C. Diffusion mechanism

It was recently postulated that the reason for the increase in Si diffusion at low implant energies is an increased surface vacancy concentration due to an increased sputtering yield for shallow implants.[15] That explanation appears to be consistent with the results reported here and suggests that consideration of sputtering yield may be important for explaining these results. For semiconductor targets, several studies have shown that the sputtering yield increases significantly when the wafer temperature is lowered through the crystalline to amorphous transition.[16-18] For off-axis implants of Ge into Ge, Holmén found the sputtering yield to decrease from 10 to 6.5 in a span of 40 °C.[17] Changes for on-axis implants were even more dramatic and abrupt. Bhattacharyya calculated the sputtering yield for Ar implanted GaAs to be 6, presumably for an amorphous target, but did not monitor the variation with temperature.[19] The shapes of the sputtering curves in these earlier studies are reminiscent of the variation in RBS yield with temperature for high dose Si implants ($\geqslant 6 \times 10^{14}$ cm^{-2}) into Ge and GaAs reported by Haynes and Holland.[6] The sputtering yield in the crystalline phase was also found to depend on the crystallographic orientation of the wafer and exhibit a nonisotropic ejection pattern.[16-18] Thus the yield change is directly associated with the crystalline to amorphous transition. This behavior has been ex-

plained on the basis of channeling in crystals; i.e., ions and recoils which can obtain channeling trajectories in crystalline targets are less likely to suffer momentum reversing collisions. The effect appears to be greater for Ge (and presumably GaAs) than for Si because ion channeling increases with atomic number and lattice spacing of the substrate.

The RBS damage fractions and TEM micrographs of the as-implanted samples (Figs. 2 and 3) indicate that GaAs undergoes an amorphous to crystalline transition in the temperature range studied for these particular implant conditions. By analogy to Ge then, the sputtering yield should decrease significantly as the temperature is increased through this transition, leading to lower surface vacancy concentrations. The 35% decrease in Ga vacancy dose needed to match the diffusion data can therefore be effected by a change in sputtering yield from $S=4.6$ to $S=3.4$ as the implant temperature rises from −2 to 40 °C (since the change in Ga vacancies represents only half of the sputtering yield). This amount of decrease is well within the range shown in the literature for semiconductor crystals at the amorphous/crystalline transition temperature.[16-18]

More channeling at higher implant temperatures would also allow more recoil atoms to penetrate deeper into the wafer, increasing the depth of excess interstitials available to form dislocation loops. The XTEM micrographs of the annealed implants in Fig. 3, where loops are found at depths over three times R_p in the 40 and 80 °C implants, support this mechanism. The sample which is implanted at −51 °C and becomes amorphous is an exception to these trends. Even though the sputtering yield is also high in this sample, excess "vacancies" are absorbed during epitaxial regrowth of the amorphous layer and are not available to affect dopant diffusion. The threefold increase in diffusion between anneal times of 5 and 30 min (see Ref. 2) appears to be related to the dissolution of the loops during this time period. The extrinsic loops are indicative of a crystal rich in interstitials, and their dissolution may allow the point defects and diffusion coefficients to return to their equilibrium values. Full understanding of this phenomenon awaits the development of models for the dislocation kinetics.

IV. SUMMARY

In conclusion, the amount of Si redistribution is found to decrease with increasing implant temperature between −2 °C and 40 °C. Concomitantly, the area bound by extrinsic, type I dislocation loops increases. RBS and TEM measurements show that the wafer undergoes an amorphous to crystalline transformation in the same temperature range. Computer simulations indicate that a 35% change in surface vacancies can account for the observed changes in both Si diffusion and loop morphology. A model has been proposed to account for these variations through changes in sputter yield at the amorphous/crystalline transition. Sputtering is higher in the low temperature, amorphous phase, such that the concentration of near surface vacancies increases, enhancing the diffusion of Si and reducing the trapped interstitial concentration. Thus in this case, the changes in loop morphology are not responsible for the variation in Si diffusion, but rather are indicative of changes in the vacancy con-

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centration that also affects Si diffusion. These results reinforce the fact that careful choice and control of implant conditions are essential for obtaining reproducible and reliable GaAs devices. In particular, low energy Si implants should be made at elevated temperatures to limit dopant redistribution.

ACKNOWLEDGMENTS

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