Effect of surface proximity on end-of-range loop dissolution in silicon

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The effect of surface proximity on the dissolution of end-of-range dislocation loops in silicon was investigated by transmission electron microscopy (TEM). A layer of dislocation loops was formed at a depth of 2600 Å by annealing a Si wafer amorphized by a $10^{15}\,\mathrm{cm}^{-2}$, 120 keV, and a $10^{15}\,\mathrm{cm}^{-2}$, 30 keV dual Si^+ implant for 30 min at 850 °C. The wafer was diced into 1 cm×1 cm pieces and polished by a chemical–mechanical polishing technique to decrease the loop depth to 1800 and 1000 Å. The samples were then furnace annealed at 900 and 1000 °C in N_2 gas. Quantitative TEM analysis revealed that the density of small loops decreases as the loop band is brought closer to the surface. The flux of interstitials to the surface varied inversely with loop depth, indicating that the loop dissolution is diffusion limited. Assuming that the loops maintain a supersaturation of interstitials (C_{IL}) around them, and by integrating the measured interstitial flux from the loop layer to the surface, the relative supersaturation of interstitials near the loop layer (C_{IL}/C_I^*) was extracted 900 and 1000 °C. [S0003-6951(99)02611-X]

Ion implantation is the preferred method of introducing dopants into silicon for the manufacture of integrated circuits (ICs). Frequently, amorphization is used to prevent channeling of light elements. However, this results in the formation of end-of-range (EOR) dislocation loops below the amorphous/crystalline (a/c) interface after the regrowth of the amorphous layer during a high-temperature anneal. The dislocation loops affect the dopant distribution by capturing or releasing point defects during a subsequent thermal cycle. The growth of dislocation loops has been determined to be governed by a bulk diffusion mechanism, whereas the loop coarsening process, which is the redistribution of point defects within the loop band, follows Ostwald ripening.[1] The enhancement of dopant diffusivity due to the excess interstitials caused by the implantation process results in transient-enhanced diffusion (TED). Recent studies have shown that the distance between the silicon surface and the ion-implant profile plays a key role in the evolution of point and extended defects. Reduction of the transient-enhanced diffusion has been observed both when the surface is brought closer by variable etching[2] and when the implant profile is made deeper due to higher implant energy.[3] In order to better understand and model TED, a greater level of fundamental knowledge about the evolution of loops and the role of the surface in controlling their behavior is necessary.

We have studied the effect of surface proximity on the evolution end-of-range dislocation loops in silicon. A 150 mm ⟨100⟩ Czochralski (CZ) -grown n-type (8–30 Ω cm) Si wafer was implanted with $10^{15}\,\mathrm{cm}^{-2}$, 120 keV and $10^{15}\,\mathrm{cm}^{-2}$, 30 keV Si^+ on an Eaton NV/GSD 200E implanter to produce a continuous surface amorphous layer. Postimplantation annealing was performed in a furnace with flowing N_2 gas (99.999% purity) at 850 °C for 30 min. Cross-sectional transmission electron microscopy (XTEM) revealed that a band of EOR loops approximately 300 Å wide were centered at a depth of 2600 Å. The wafer was then diced into 1 cm×1 cm pieces. A chemical–mechanical polishing (CMP) procedure[4] that removes measured amounts of silicon and leaves the surface smooth was used on the pieces to bring the loop band closer to the surface. The depths were verified by XTEM. The three loop samples were then subjected to a second anneal for either 30 and 120 min at 900 °C or 15 and 30 min at 1000 °C. These times and temperatures were chosen based on prior studies in the growth and coarsening mechanisms of dislocation loops.[1] The control sample did not undergo any further anneals. The procedure for counting interstitials in loops from plan view transmission electron microscopy (PTEM) images and a detailed account of the counting error encountered has been reported.[5]

For the PTEM micrographs shown in Figs. 1(a)–1(d), it was found that the area density of the loops was $1\times10^{11}\,\mathrm{cm}^{-2}$ for the 2600 Å loop depth and $5\times10^{10}\,\mathrm{cm}^{-2}$ for the 1000 Å loop depth sample. Figures 2(a)–2(c) show that the size distribution for the 1000 °C, 30 min anneal gets skewed toward the larger sizes as the loops get closer to the surface. The density of the loops of diameters less than 400 Å decreases from 16×10^9 to $4\times10^9\,\mathrm{cm}^{-2}$, going from a loop depth of 2600 Å to a depth of 1000 Å. The loop mean diameter increased as the loop band was brought closer the silicon surface.

The number of interstitials bound by the dislocation loops in the loop control sample was found to be 4.5×10^{14} atoms. The number of interstitials lost from the loops during the anneal was determined by using the control sample as a reference and subtracting the number of interstitials trapped in loops at a subsequent time step from the reference. The

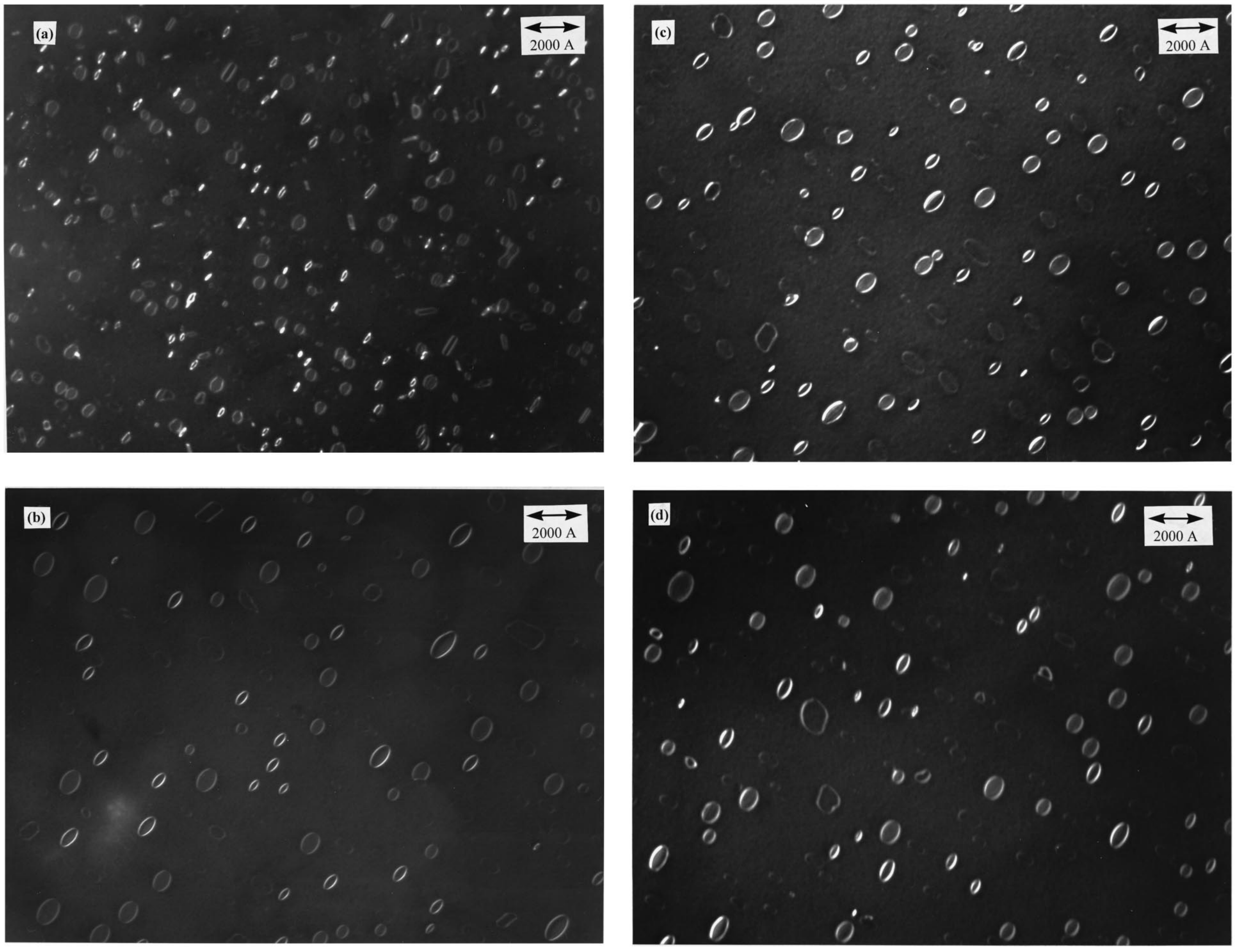

FIG. 1. PTEM images of the samples of (a) the loop control and loop samples with loop depth of (b) 2600 Å, (c) 1800 Å, and (d) 1000 Å after the 1000 °C, 15 min anneal.

interstitials bound by loops as a function of time with respect to the control are shown in Figs. 3(a)–3(b) for the 900 and 1000 °C anneals, respectively. At 900 °C the loop sample with the band centered at 1000 Å lost 2×10^{14} interstitials in the first 30 min of annealing as compared to 0.75×10^{14} interstitials lost from loops in the 2600 Å sample. The curves flatten out with increasing anneal time to 120 min, indicating that the rate of loss declines with time. Similar trends are observed in the 1000 °C anneal [Fig. 3(b)] sample. The interstitial flux is determined by the slope of a straight line fit between the control and the sample annealed for 30 min at 900 °C and a straight line fit between the control and the sample annealed for 15 min at 1000 °C. These numbers were extracted from the above plots as a function of the loop depth.

The loop dissolution is analyzed by assuming a diffusion-limited model. The loop band, at a distance d from the surface, has a interstitial concentration of C_{IL} in the loop boundary, which is the concentration of interstitials in the periphery of the loop layer. The equilibrium is denoted by C_I^*. The Si surface, which is assumed to be a perfect sink,[2,6] maintains the interstitial concentration at the surface at C_I^*. The interstitial concentration in the vicinity of the loops, defined as C_{IL}, is pinned at some value near the loop band. The loops dissolve at higher temperatures to maintain C_{IL}, generating a flux to the surface. With a high enough thermal budget, the interstitial profile from the loops to the surface is a straight line, i.e., it is diffusion limited.

With these assumptions, the interstitial flux equation to the surface is defined as

$$\frac{dn_I}{dt}=\frac{D_I C_I^*}{d}\left(\frac{C_{IL}}{C_I^*}-1\right), \tag{1}$$

where dn_I/dt is the interstitial flux to the surface and D_I is the diffusivity of the interstitials. The dn_I/dt values are determined from the loop dissolution rates described above. Experimentally determined values for $D_I C_I^*$ are in good relative agreement with each other compared to either D_I or C_I^* in which there are great variations.

Using the $D_I C_I^*$ values from the literature,[7,8] it is possible to extract C_{IL}/C_I^* from the rate of loss of interstitials from the loops. Figure 3 shows that the rate loss changes in time. This is to be expected, because the loop distribution is also changing in time. C_{IL} is a function of the loop radius, and therefore, changes in time as the loops dissolve and ripen. Consequently, the best place to investigate the surface effect C_{IL}/C_I^* is at the shortest time, since the loop distribution starts the same for all depths. As the loops evolve in time, we can no longer assume that C_{IL} is the same for all depths. Since we cannot directly measure the rate loss, we have to measure the number of interstitials at some later

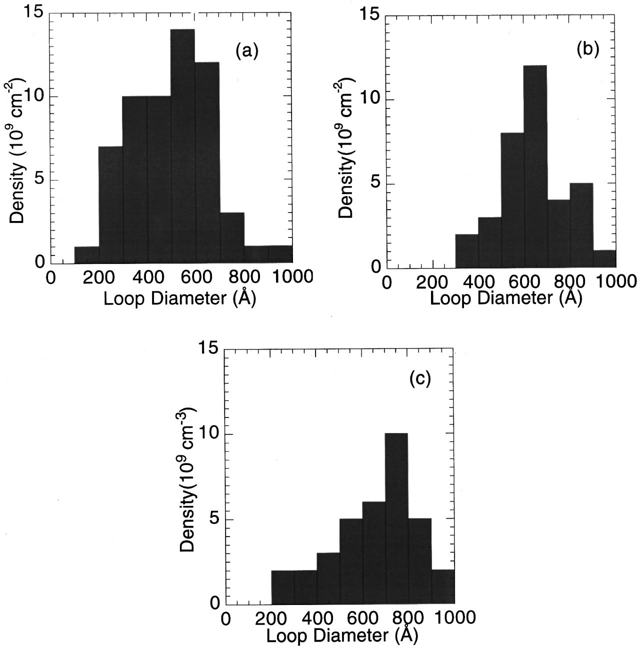

FIG. 2. Loop size distribution at 1000 °C, 30 min for (a) 2600 Å, (b) 1800 Å, and (c) 1000 Å loop depth samples.

point in time, and this introduces an error into comparing the different depths to one another. If this error is small and the surface controls dissolution, we would expect to see a good match in the computed values of C_{IL}/C_I^*.

The flux values can then be inserted into Eq. (1) to extract the C_{IL}/C_I^* values. Table I shows a spreadsheet of the

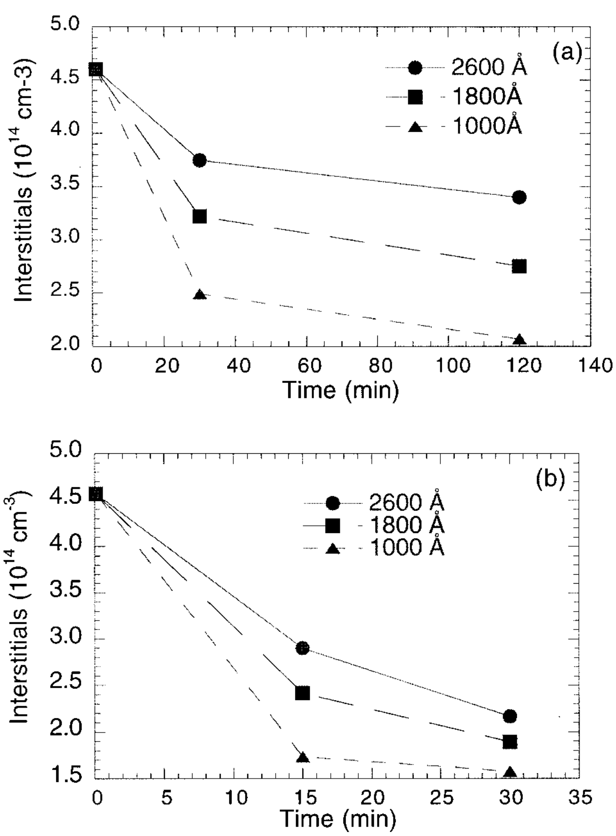

FIG. 3. Plot of loss of interstitials with time at (a) 900 °C and (b) 1000 °C for the three loop depths.

TABLE I. A spreadsheet showing the extracted flux and the interstitial supersaturation values.

Depth (A)	Temperature (K)	$D_I C_I^*$	dn/dt	C_{IL}/C_I^*
2600	1173	7.43×10^4	4.71×10^{10}	17.46
1800	1173	7.43×10^4	5.02×10^{10}	17.45
1000	1173	7.43×10^4	1.22×10^{11}	17.40
2600	1273	3.19×10^6	1.73×10^{11}	2.48
1800	1273	3.19×10^6	2.38×10^{11}	2.34
1000	1273	3.19×10^6	3.22×10^{11}	2.00

extracted flux and the interstitial supersaturation values. The C_{IL}/C_I^* was found to be ~17 at 900 °C and is fairly constant with loop depth, as expected. At 1000 °C, the C_{IL}/C_I^* value drops to ~2. This result compares well with previously used values in the literature.[9] It was found that the flux varies inversely with the loop depth for both the annealing temperatures. This result indicates that the dissolution of dislocation loops is diffusion limited to the surface. It also indicates that C_{IL} is not changing significantly in the loops over the initial time period.

In conclusion, it was found that the proximity to the silicon surface significantly affected the dissolution kinetics of dislocation loops. The flux of interstitials to the surface was measured using quantitative TEM analysis and was found to be varying inversely with loop depth, indicating that the loop dissolution is diffusion limited to the silicon surface. By integrating the measured interstitial flux from the loop layer to the surface, the relative supersaturation of interstitials near the loop layer (C_{IL}/C_I^*) was extracted. This work demonstrates that the loop dissolution is diffusion limited to the surface, since identical loop layers were annealed with the only difference being the amount of surface polishing. Since the dissolution rate has a nearly exact inverse depth dependence, the surface is the controlling sink.

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[1] J. Liu, M. E. Law, and K. S. Jones, Solid-State Electron. **38**, 1305 (1995).
[2] D. R. Lim, C. S. Rafferty, and F. P. Klemens, Appl. Phys. Lett. **67**, 2302 (1995).
[3] A. Sultan, S. Banerjee, S. List, and M. Rodder, Appl. Phys. Lett. **69**, 2228 (1996).
[4] S. B. Herner, B. P. Gila, K. S. Jones, H. J. Gossman, J. M. Poate, and H. S. Luftman, J. Vac. Sci. Technol. B **14**, 3593 (1996).
[5] S. Bharatan, J. Desroches, and K. S. Jones, in *Transmission Electron Microscopy Characterization of Lattice Damage* (Ion Beam, Austin, TX, 1997).
[6] M. J. v. Dort, W. van. der. Wel, J. W. Slotboom, N. E. B. Cowern, M. P. G. Knuvers, H. Lifka, and P. C. Zalm, Tech. Dig. Int. Electron Devices Meet. , 865 (1994).
[7] M. Tang, L. Colombo, J. Zhu, and T. D. d. l. Rubia, Mater. Res. Soc. Symp. Proc. **396**, 33 (1996).
[8] M.-J. Cartula, T. D. d. l. Rubia, L. A. Marques, and G. H. Gilmer, Phys. Rev. B **54**, 16683 (1996).
[9] C. Bonafos, M. Omri, B. de Mauduit, G. BenAssayag, A. Claverie, D. Alquier, A. Martinez, and D. Mathiot, J. Appl. Phys. **82**, 2855 (1997).