The effect of preamorphization energy on ultrashallow junction formation following ultrahigh-temperature annealing of ion-implanted silicon

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High-power arc lamp design has enabled ultrahigh-temperature (UHT) annealing as an alternative to conventional rapid thermal processing (RTP) for ultrashallow junction formation. The time duration of the UHT annealing technique is significantly reduced from those obtained through conventional RTP. This difference in time may offer the ability to maintain a highly activated ultrashallow junction without being subjected to transient enhanced diffusion (TED), which is typically observed during postimplant thermal processing. In this study, two 200-mm (100) *n*-type Czochralski-grown Si wafers were preamorphized with either a 48- or a 5-keV Ge^+ implant to 5×10^{14} cm^2, and subsequently implanted with 3-keV BF_2^+ molecular ions to 6×10^{14} cm^2. The wafers were sectioned and annealed under various conditions in order to investigate the effects of the UHT annealing technique on the resulting junction characteristics. The main point of the paper is to show that the UHT annealing technique is capable of producing a highly activated *p*-type source/drain extension without being subjected to TED only when the preamorphization implant is sufficiently deep.
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INTRODUCTION

Ion implantation is commonly used in complementary metal-oxide-semiconductor (CMOS) technology to dope the source/drain extension (SDE) region of the device.[1] This process is known to create a large amount of interstitial-vacancy (Frenkel) pairs caused by the nuclear collisions among the primary ions and recoiled atoms with the host atoms of the substrate. Many of these Frenkel pairs recombine during relaxation of the collision cascade produced by the implanted ion, after which the primary damage generated by the incident ion can be considered stable.[2,3] The probability of the recombination of a Frenkel pair is dependent upon the separation distance of the interstitial and vacancy, temperature, and the concentration of point defect traps. For nonamorphizing implants, the stable damage is primarily small defect clusters, dopant-defect complexes, and some isolated Frenkel pairs. It is well known that continuous amorphous layers can be formed by ion implantation, and that these layers are capable of preventing ion channeling associated with the implantation of low-mass species (e.g., B). These layers extend from the substrate surface down to a depth dependent on the implant conditions. When considering amorphous Si (α-Si) it can be said that the lattice maintains some short-range order, although it is significantly disordered and consists of atoms with unsatisfied bonds that exhibit large tetrahedral bond-angle distortions.[4] The threshold damage density for the formation of an amorphous layer is often taken to be 10% of the Si lattice density.[5] It was shown that damage accumulation saturates after an amorphous state is reached.[2] It is well known that α-Si has a melting temperature and an atomic density of approximately (225 ± 50) °C and (1.8 ± 0.1)% below that of crystalline Si (c-Si), respectively.[6–8] In addition, it was shown that α-Si consists of a covalently bonded continuous random network (CRN) that can exist as either an as-implanted or a structurally relaxed state.[9–14] The structurally relaxed α-Si differs from the as-implanted case in that the number of large-angle bond distortions and defect complexes produced during the preamorphization implant are reduced, typically by a low-temperature relaxation anneal (e.g., 500 °C for 60 min).[15] Regardless of the structural state of the α-Si, a large population of excess interstitials are transmitted through the amorphous layer and remain below the original amorphous/crystalline (α/c) interface until postimplant thermal processing.

Postimplant thermal processing is required to induce solid phase epitaxial regrowth (SPER) of the implantation-induced amorphous layer, which repairs the lattice damage accumulated during the implantation process as well as activates the implanted dopants by establishing them on substitutional sites where they are able to contribute their holes (electrons) to the valence (conduction) band. During SPER of an amorphous layer, the excess interstitials coalesce into small defect clusters.[16] During the subsequent thermal processing these small defect clusters, which are located just below the original α/c interface [termed the end-of-range (EOR) region], evolve into either {311} defects or dislocation loops. The {311} defect is an extrinsic row of interstitials

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lying on the {311} habit plane, elongated in the ⟨110⟩ direction. Two different types of dislocation loops have been observed: the so-called perfect prismatic loops with a Burgers vector $b=a/2\langle 110\rangle$ and faulted Frank loops with a Burgers vector $b=a/3\langle 111\rangle$.[16] Dislocation loops are more stable than {311} defects.[17] During postimplant thermal annealing, these defects release interstitials and these interstitials give rise to transient enhanced diffusion (TED), which significantly increases the diffusion behavior of dopants, such as B and P, which diffuse primarily or in part by an interstitial(cy) mechanism.[18] It was shown that the amount of TED observed during an anneal decreases when the implant damage is annealed out at a higher temperature.[1] This observation influenced the development of single-wafer thermal processes capable of producing a high-temperature ambient with ramp rates on the order of 50–200 °C/s, and fast switching times in order to insulate the dopant from a high degree of TED.[19]

Rapid thermal processing (RTP) has proven to be successful in producing junctions with the performance characteristics necessary for the continued scaling of CMOS technology to date. Its ability to satisfy these requirements is associated with improved equipment capability in the form of spike annealing, which decreases the effective thermal budget, allowing for higher annealing temperatures to improve activation and reduce the amount of diffusion of the dopants during the thermal process. A spike anneal is characterized as a short thermal-anneal cycle that can be achieved by increasing the ramp-up and ramp-down rates and by minimizing the dwell time at the temperature of interest. The inability of this technique to produce junctions with the performance characteristics required by future technology nodes is in the cycle time of the thermal process, which results in an unacceptable amount of dopant diffusion. The minimum cycle times in conventional RTP techniques are limited by the maximum power delivered to the wafer (which determines the ramp-up rate) and the minimum response time of the relatively large thermal mass incandescent tungsten lamps (which determines both the soak time and the ramp-down rate). Without being able to minimize the soak time and the ramp-down rate, increasing the ramp-up rate above 100 °C/s results in a negligible improvement in terms of forming a highly activated ultrashallow junction.[19] This illustrates the need to investigate advanced annealing technologies that may be able to produce highly activated junctions without being subjected to TED.

High-power arc lamp design has enabled ultrahigh-temperature (UHT) annealing as an alternative to conventional RTP for ultrashallow junction formation.[20] This technique heats the wafer to an intermediate temperature (e.g., 800 °C) before discharging a capacitor bank into flash lamps, which heat the device side of the wafer to a relatively high temperature (e.g., 1200 °C) for a few milliseconds.[21–23] This time duration is significantly reduced from those obtained with conventional RTP, which are on the order of 1–2 s within 50 °C of the peak temperature. This difference in annealing time may offer the ability to maintain a highly activated ultrashallow junction without being subjected to TED, which is typically observed during postimplant thermal processing. In this paper, we investigate the possibility of the UHT annealing technique to activate a junction at a relatively high temperature (e.g., 1300 °C) without being subjected to TED.

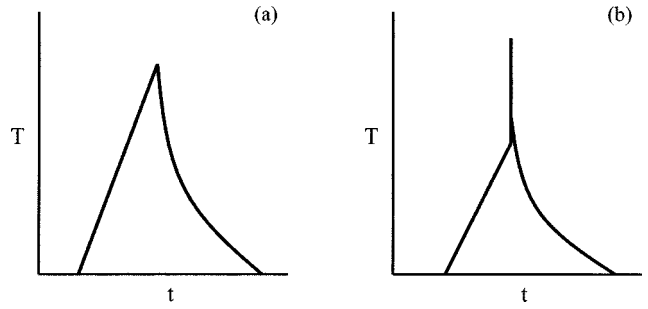

FIG. 1. Representative temperature-time ($T-t$) profiles of the (a) iRTP and (b) fRTP anneal processes. The iRTP anneal ramps directly to a peak temperature and cools back down by thermal convection. The fRTP anneal ramps to an intermediate temperature, where a high-temperature thermal cycle is superimposed by discharging a capacitor bank into flash lamps. Thermal conduction through the bulk of the substrate cools the wafer quickly after the high-temperature cycle, and thermal convection is responsible for cooling the wafer down to room temperature.

EXPERIMENTAL DESIGN

Two 200-mm 3–5 Ω cm (100) *n*-type Czochralski (CZ)-grown Si wafers were preamorphized with either a 48- or a 5-keV Ge^+ implant to 5×10^{14} cm^2, and subsequently implanted with 3-keV BF_2^+ molecular ions to 6×10^{14} cm^2. The implants were carried out in the drift mode and performed at room temperature with the ion beam normal to the surface plane using an Applied Materials Leap-II system. The implant parameters were monitored to ensure that they remained within predetermined limits. The wafers were then sectioned and annealed at Vortek Industries to investigate the effects of the UHT annealing technique on the resulting junction characteristics. Representative temperature-time (*T*-*t*) profiles of the two UHT annealing techniques are shown in Fig. 1. The impulse anneal (iRTP™) is produced by continuous-wave mode arc lamp irradiation of the front surface of the wafer and is responsible for producing the bulk wafer temperature, known as the intermediate temperature, at which the flash anneal (fRTP™) is to be introduced. The fRTP anneal is produced by discharging a capacitor bank into flash lamps, which increase the temperature of the surface of interest while increasing the bulk wafer temperature to not more than 50 °C of the intermediate temperature, allowing for conductive heat loss through the substrate. The iRTP anneal provides a means to better understand the advantages gained by the fRTP anneal. All of the anneals were carried out in a N_2 ambient with less than 10 ppm O_2. The iRTP and fRTP anneal temperatures were determined by a radiometer, which determined the wafer emissivity through a reflectance calculation that expresses the temperature of the system. In this experiment, iRTP anneals were performed over the range of 760–1100 °C using a ramp-up rate of 400 °C/s, and a ramp-down rate which was estimated to be approximately 150 °C/s at 900 °C. The ramp-down rate was determined by an instantaneous derivative of the radiation-cooling curve for a gray body with an emissivity and thickness comparable to

the Si substrate. It should be noted that the ramp-down rate for conventional RTP is limited to 50–80 °C/s due to radiative cooling of the substrate to the ambient.[19] The ramp-down rate is greater than that obtained through conventional techniques due to the use of an absorbing chamber technology, which reduces radiation return to the substrate, providing an improved cooling rate.[24] The fRTP anneals were performed over the range of 1200–1350 °C using ramp-up and ramp-down rates on the order of 10^6 °C/s.

Dynamic secondary-ion-mass spectrometry (SIMS) was used to quantify dopant concentration as a function of depth. The $^{10}B^+$ and $^{11}B^+$ counts were obtained on a Cameca IMS-6*f* analytical tool using an O_2^+ primary beam with a nominal beam current of 50–70 nA and a net impact energy of 800 eV directed 50° from the sample normal. The depth profile was established by continuously rastering a 200 $\times 200$ μm^2 area, and collected from a centered circular area 30–60 μm in diameter under an isobaric O_2 ambient, which provided an adequate condition for the complete oxidation of the Si surface during analysis. The system was configured so as to maintain a sputtering rate of 0.08–0.1 nm/s. Variable angle spectroscopic ellipsometry (VASE) was used to determine the thickness of the implantation-induced amorphous layers. The VASE measurements were performed on a J. A. Woollam Co., Inc. multiwavelength ellipsometer with the 75-W Xe light source tilted 20° from the surface plane. The system was calibrated by fitting a known oxide thickness from a control Si substrate, and each subsequent measurement assumed a 2-nm native oxide above the continuous amorphous layer in order to more accurately measure the amorphous layer thickness. Cross-sectional transmission electron microscopy (XTEM) was used to verify the thickness of the amorphous layers measured by VASE. The XTEM samples were thinned by 5-kV Ar^+-ion milling, with the plasma sources tilted 12° from the surface plane. All XTEM images were captured on a JEOL 200 CX TEM operating at 200 kV under a bright field imaging condition with the objective aperture centered over the transmitted beam. A Prometrics RS-20 four-point probe was used to measure the sheet resistance (R_s) for each anneal condition. The sample geometric correction factor is negligible for the wafer sections, which have surface areas greater than those below which edge effects reduce measurement accuracy.

RESULTS

The 48- and 5-keV preamorphization implants to 5×10^{14} cm^2 produced continuous amorphous layers extending 76 and 12 nm below the substrate surface, respectively, as determined by VASE and verified through XTEM (not shown).

Figures 2(a) and 2(b) show the SIMS results for each of the iRTP anneals used in this study for the 48- and 5-keV preamorphization implants, respectively. Each profile shows an increase in junction depth x_j when compared to the as-implanted profile. The x_j is defined as the depth of the profile at a dopant concentration of 1×10^{18} cm^3. Figure 2(a) shows that the 760 and 800 °C iRTP anneals display similar profiles. A SIMS profile for a 585 °C furnace anneal for 45 min

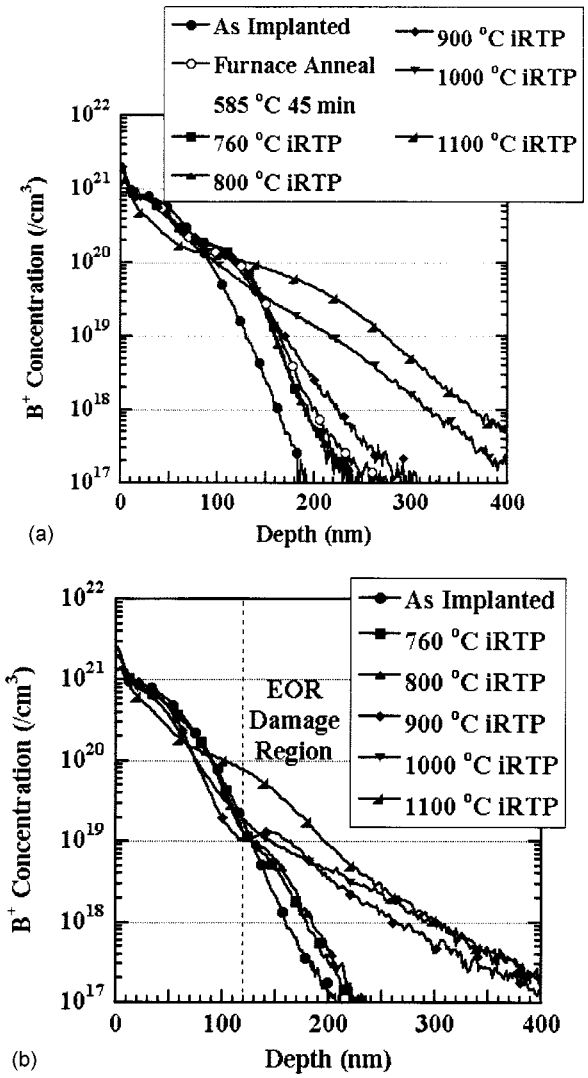

FIG. 2. Concentration profiles showing the B^+ concentration as a function of depth for the 3-keV BF_2^+ implant to 6×10^{14} cm^2 after each iRTP anneal temperature used in this study for the (a) 48- and (b) 5-keV Ge^+ preamorphization implants to 5×10^{14} cm^2. The symbols are for identification purposes only.

is included with the data in Fig. 2(a), and shows very similar diffusion behavior when compared to the 760 and 800 °C iRTP anneals. Figure 2(b) shows that the 760 and 800 °C iRTP anneals produce a slight amount of diffusion when compared to the as-implanted profile. It should be noted that the profiles are comparable to the as-implanted profile above a concentration of 1×10^{19} cm^3. It can be said that the diffusion observed for the 760 and 800 °C iRTP anneals in Fig. 2(b) occurs in *c*-Si, since the motion occurs below the original α/c interface produced by the 5-keV preamorphization implant.

Figure 2 shows that the diffusion behavior for the 900 °C iRTP anneal is much larger for the 5-keV preamorphization implant when compared to the 48-keV preamorphization implant. Figure 2(b) shows that the 900 °C iRTP anneal is sufficient to produce a peak approximately 14 nm below the substrate surface. Since the corresponding plan-view TEM (PTEM) results (not shown) revealed that no observable defects formed for the 5-keV preamorphization im-

plant, it is presumed that this peak forms because of the high local concentration of excess interstitials and B atoms in that region which forms B-interstitial clusters (BICs) during postimplant UHT annealing.

Figure 2(a) shows that the 48-keV preamorphization implant results in increased diffusion behavior for the 1000 and 1100 °C iRTP anneals when compared to the results for the 5-keV preamorphization implant in Fig. 2(b).

Figure 2(a) shows that the iRTP anneals produce profiles with plateau concentrations on the order of (1.4–1.8) $\times 10^{20}$ cm^3 for the 48-keV preamorphization implant. The plateau concentration is defined as the concentration at which the anneal produces an inflection point. These profiles show inflection points between 7 and 8 nm below the substrate surface. These inflection points correspond to the concentration levels below which B is diffusing and presumed to be active and above which inactive B cluster formation or precipitation occurs and the B remains immobile.[25,26] It should be noted that the 1100 °C iRTP anneal dissociated some of the initially inactive dopant near the Si surface, independent of the preamorphization implant energy.

Figures 3(a) and 3(b) show the SIMS profiles for a collective subset of intermediate temperatures with a 1200 °C fRTP anneal for the 48- and 5-keV preamorphization implants, respectively. As can be seen in Fig. 3(a), the 760 and 800 °C intermediate anneals produce similar profiles after the 1200 °C fRTP anneal for the 48-keV preamorphization implant. The slight diffusion that occurs during the fRTP anneal shows that most of the overall diffusion occurs during rampup to the intermediate temperature. It should be noted that the diffusion behavior for each of the profiles is much less than would be expected from a conventional RTP anneal, presumably because of the short amount of time spent at a relatively high temperature. Figure 3(b) shows that the 760 and 800 °C intermediate anneals produce an increase in B diffusion behavior with the 1200 °C fRTP anneal for the 5-keV preamorphization implant. The 900 °C intermediate temperature results in a profile with an exponentially decreasing tail after the 1200 °C fRTP anneal for the 5-keV preamorphization implant.

Figures 4(a) and 4(b) show the SIMS results for the 1350 °C fRTP anneal for the 48- and 5-keV preamorphization implants, respectively. As can be seen in Fig. 4(a), the 760 °C intermediate anneal results in a slightly shallower profile with the introduction of the 1350 °C fRTP anneal when compared to the 800 °C intermediate anneal, which was not observed following the 1200 °C fRTP anneal shown in Fig. 3(a). Also, these profiles are deeper than those produced by the 1200 °C fRTP anneal, showing that the diffusion characteristics are dependent on the peak fRTP anneal temperature. As can be seen in Fig. 4(b), the 1350 °C fRTP anneal results in similar profiles independent of the intermediate anneal temperature for the 5-keV preamorphization implant. Additional SIMS results (not shown) reveal that similar profiles are also obtained when using a 1300 °C fRTP anneal.

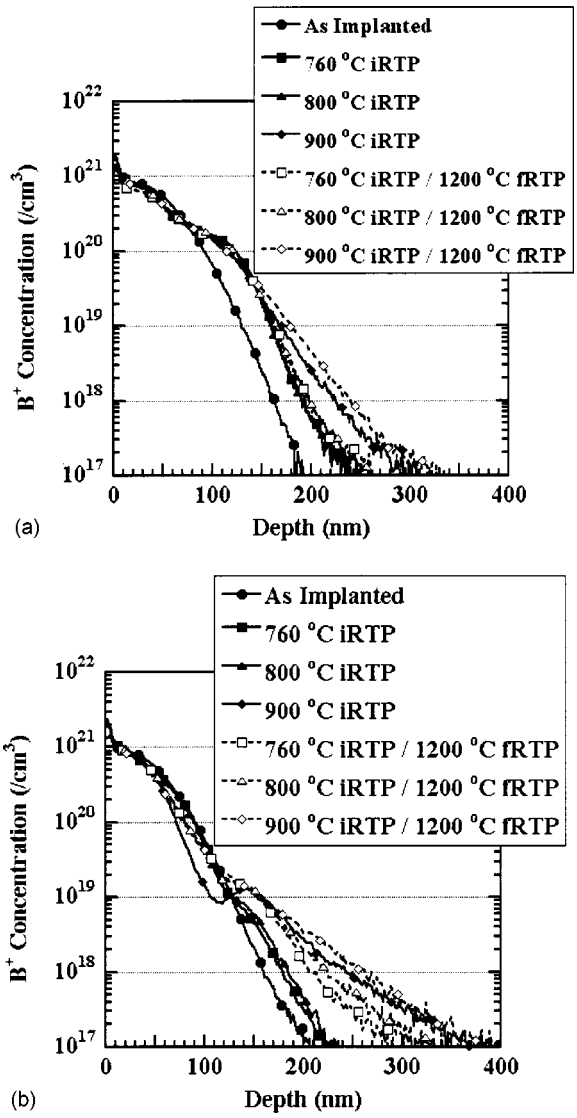

FIG. 3. Concentration profiles showing the B^+ concentration as a function of depth for the 3-keV BF_2^+ implant to 6×10^{14} cm^2 before and after a 1200 °C fRTP for the (a) 48- and (b) 5-keV Ge^+ preamorphization implants to 5×10^{14} cm^2. The symbols are for identification purposes only.

DISCUSSION

The SIMS results for the 760 and 800 °C intermediate temperatures in Fig. 3(a) showed that, for a 1200 °C fRTP anneal, most of the diffusion occurred during ramp up to the intermediate temperature for the 48-keV preamorphization implant. It was shown that B from both B^+ and BF_2^+ implants into preamorphized Si displayed a similar diffusion enhancement during SPER of an implantation-induced amorphous layer at 550 °C.[27] Since B thermal diffusion in *c*-Si is negligible at 550 °C, this diffusion enhancement was attributed to TED (possibly due to the large amount of damage produced by the 20-keV Si^+ preamorphization implant to 5×10^{14} cm^2). However, the fact that the same diffusion profile was obtained over the temperature range of 585–800 °C in Fig. 2(a) suggests that the diffusion enhancement is not TED. Instead, it is proposed here that the diffusion enhancement observed in Fig. 2(a) is caused by B diffusion in α-Si before the complete recrystallization of the implantation-induced amorphous layer (i.e., not TED).

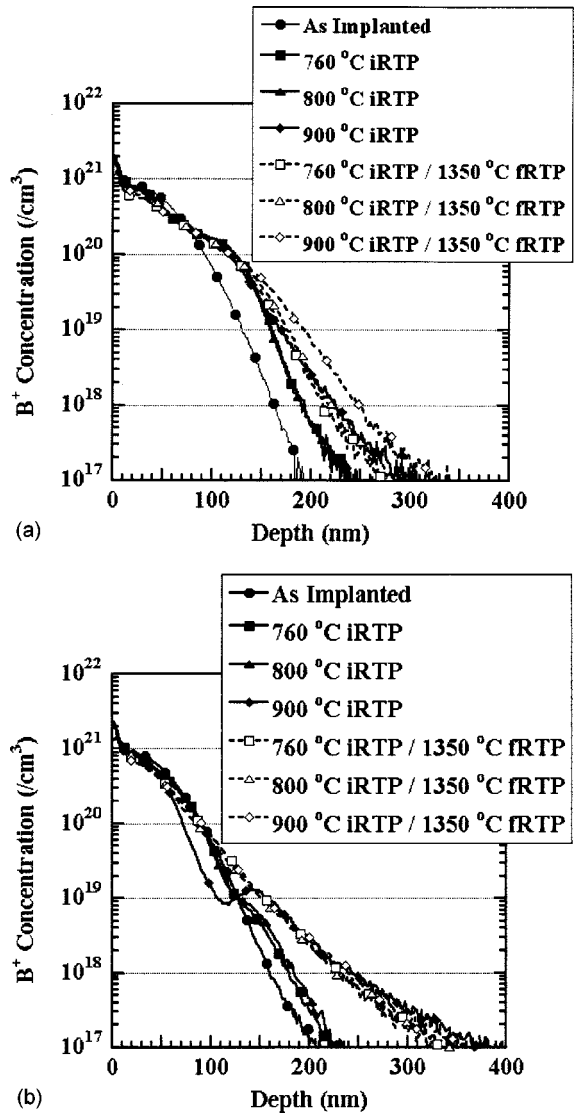

FIG. 4. Concentration profiles showing the B^+ concentration as a function of depth for the 3-keV BF_2^+ implant to 6×10^{14} cm^2 before and after a 1350 °C fRTP for the (a) 48- and (b) 5-keV Ge^+ preamorphization implants to 5×10^{14} cm^2. The symbols are for identification purposes only.

It was shown that B diffusivity in α-Si at 600 °C is more than five orders of magnitude greater than that in *c*-Si.[28] This was done by growing three narrow B profiles with a peak concentration of 1.3×10^{20} cm^3 at depths of 170, 338, and 508 nm with respect to the substrate surface. These three B profiles were then implanted at −196 °C with 600-keV Si^+ to 5×10^{15} cm^2 and subsequently implanted with 70-keV Si^+ to 5×10^{14} cm^2 to produce a continuous amorphous layer extending 900 nm below the substrate surface. The amorphous layer was then recrystallized at 600 °C and continuously monitored by time-resolved reflectivity (TRR). The data show that the three B profiles are slightly broadened by the two Si^+ preamorphization implants, and that the three B profiles are further broadened during the SPER of the implantation-induced amorphous layer. The broadening of the three profiles increases with decreasing depth from the substrate surface (i.e., the profiles that spend the most time within the α-Si show the most broadening during SPER of the amorphous layer). This result is inconsistent with TED, which would cause the deepest B profile to broaden the most. This result is also inconsistent with the suggestion that dopant segregation across the advancing α/c interface caused the increase in diffusion behavior.[29] If the diffusion occurred because of mass transfer across the α/c interface, then it would be independent of the amount of time the B spends in α-Si, which was not the case in Ref. 28.[29] The results in that study estimate the B diffusivity in α-Si to be approximately $(2.6\pm0.5)\times10^{-16}$ cm^2/s at 600 °C, which matches very well with the calculated (i.e., $2\sqrt{Dt}$) amount of diffusion expected from the 585 °C furnace anneal in Fig. 2(a) (assuming a regrowth velocity of approximately 30 nm/min).[30] Figure 2(b) showed no B diffusion during SPER of the implantation-induced amorphous layer, presumably because of the high local concentration of excess interstitials produced by the 5-keV preamorphization implant (which couple with the B atoms and form immobile clusters, preventing diffusion in the amorphous phase). It should be noted that the diffusion coefficient of Ge in α-Si was reported to be very low and is not expected to have a significant impact on the results in Fig. 2.[31]

The profiles after the 760 and 800 °C iRTP anneals in Fig. 2(a) showed approximately 3 nm of diffusion up to a concentration of 1.8×10^{20} cm^3, above which inactive B cluster formation or precipitation occurred and B remained immobile during SPER of the amorphous layer produced by the 48-keV preamorphization implant. Similar profiles were observed by Jin *et al.*, who showed that this characteristic is independent of B^+ or BF_2^+ implantation after a 550 °C furnace anneal for 40 min.[27] Since additional XTEM results (not shown) revealed that the 76-nm continuous amorphous layer produced by the 48-keV preamorphization implant completely recrystallized during the 760 °C iRTP anneal, it can be said that the 760 and 800 °C iRTP anneals result in similar dopant profiles due to the fact that B remains in α-Si at the same amount of time before the recrystallization of the amorphous layer is complete. This shows that the 760 and 800 °C iRTP anneals are insufficient to evolve the excess interstitials to the point where TED begins to affect the overall diffusion profile. The observation of similar dopant profiles for the 760 and 800 °C iRTP anneals suggests that there is a temperature range in which the iRTP anneal will result in equivalent dopant profiles without being subjected to TED.

Figure 5 shows that the 900 °C iRTP anneal, increased the x_j from 19.3 to 22.5 nm when compared to the 800 °C iRTP anneal for the 48-keV preamorphization implant. Florida object-oriented process simulator (FLOOPS) simulations estimate that approximately 3 min at 900 °C are required to produce the 3.2 nm increase in x_j for the 900 °C iRTP anneal. Since the entire anneal cycle (i.e., ramping up to 900 °C and cooling down to room temperature) was complete on the order of 8–10 s, the increase in diffusion behavior is attributed to TED. The corresponding PTEM results (not shown) revealed that the 760, 800, and 900 °C iRTP anneals produce defect structures consisting of a high density of defect clusters. This suggest that either a submicroscopic interstitial cluster dissolution and evolution or a nonconservative defect coarsening process of the EOR damage is re-

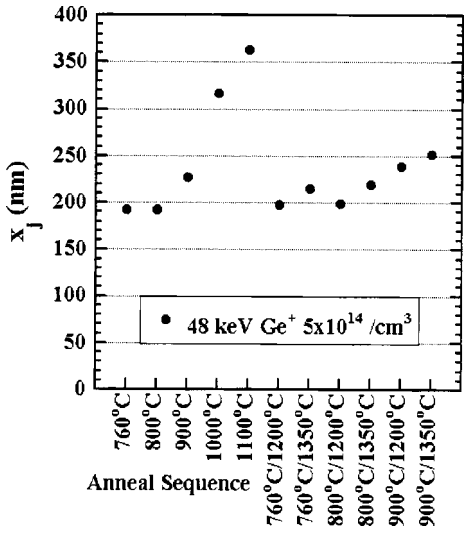

FIG. 5. Graph of x_j as a function of the anneal sequence for the 48-keV Ge^+ preamorphization implant to 5×10^{14} cm^2. Note that all the samples that received either a 1200 or a 1350 °C fRTP anneal have shallower x_j compared to the samples that received the 1000 or 1100 °C iRTP anneal.

sponsible for the diffusion enhancement observed for the 900 °C iRTP anneal in Fig. 2(a).

It was shown that the 900 °C iRTP anneal in Fig. 2(a) showed less of a diffusion enhancement than in Fig. 2(b). This difference is presumably caused by the effect of interstitial release from the EOR damage region. It was shown that the interstitial flux from the EOR damage is approximately an order of magnitude greater into the substrate than toward the surface for overlapping 112-keV and 30-keV Si^+ implants to 1×10^{15} cm^2 performed at (20 ± 1) °C.[32] The decrease in the interstitial flux toward the surface was attributed to the EOR damage acting as interstitial traps, which prevent a significant fraction of the interstitials from diffusing toward the substrate surface. Jones *et al.* correlated the EOR dislocation loop density with the amount of interstitial backflow toward the surface, which increased with decreasing implant temperature (presumably due to the fact that less EOR damage is available to prevent the interstitials from diffusing toward the substrate surface).[33] The difference in the interstitial flux for near room-temperature preamorphization implants offers an explanation for observing increased diffusion enhancement below and the lack of diffusion behavior above the original α/c interface produced by the 5-keV preamorphization implant. It is presumed that the BICs that form for the 5-keV preamorphization implant behave in a similar way to EOR damage in that they are capable of obstructing interstitial backflow toward the surface.

Figure 5 shows that the 900, 1000, and 1100 °C iRTP anneals increased the x_j by 3.2, 12.4, and 16.8 nm, respectively, compared to the 800 °C iRTP anneal for the 48-keV preamorphization implant. These results show that the largest difference in B diffusion behavior is observed for the 1000 °C iRTP anneal. The increase in diffusion behavior for the 1000 °C iRTP anneal is most likely due to a significant fraction of the interstitial flux toward the surface, which is capable of reaching the B profile during the 1000 °C iRTP anneal but is less pronounced for the 900 °C iRTP anneal. Such a significant pulse of TED was shown to occur for the 40-keV Si^+ implants to both 2×10^{13} and 5×10^{13} cm^2 during the first 15 *s* of annealing at 700 °C.[34] This pulse of TED was shown to be in excess of the enhancement caused by {311} defect dissolution, suggesting a different source of interstitials.[34] It is presumed that a similar mechanism is causing the diffusion enhancement for the 1000 °C iRTP anneal in Fig. 2(a) for the 48-keV preamorphization implant, because the corresponding PTEM results (not shown) revealed that {311} dissolution is incomplete following the 1000 °C iRTP anneal. Figure 2 showed that the 1000 and 1100 °C iRTP anneals increased the x_j much less for the 5-keV preamorphization implant when compared to the 48-keV preamorphization implant, presumably because once the interstitials pass the B profile they no longer affect its diffusion behavior.

Figure 3(a) showed that the 760 and 800 °C intermediate temperatures resulted in similar profiles following the 1200 °C fRTP anneal, and that the 900 °C intermediate temperature resulted in an increased x_j due to the diffusion that occurred during ramp up to the intermediate temperature for the 48-keV preamorphization implant. Additional FLOOPS simulations estimate that approximately 3 ms at 1200 °C are required to produce the observed 0.6 nm increase in x_j for the 760 and 800 °C intermediate temperatures. Although the *T-t* profiles for the 1200 °C fRTP anneals are unavailable, it is reasonable to say that the observed diffusion behavior is caused by equilibrium diffusion and not TED (since the fRTP takes approximately 5 ms to complete). This is a remarkable result, considering that the junction was annealed at a peak temperature of 1200 °C. Although these time scales are similar to those used during the fRTP anneal, it is not known whether interstitial recombination within the bulk or a lack of thermal energy prevented significant diffusion during the anneal. It is reasonable to assume that the time duration of the fRTP anneal is too short to allow enough interstitials to diffuse toward the surface to cause a significant diffusion enhancement. Similar comments can be made for the diffusion behavior observed after the 1350 °C fRTP anneal for the 48-keV preamorphization implant shown in Fig. 4(a). The fact that the 900 °C intermediate temperature resulted to no additional diffusion enhancement after the 1200 °C fRTP anneal in Fig. 3(b) suggests that the interstitial flux into the substrate is complete during ramp up to the 900 °C intermediate temperature. This is supported by the SIMS results in Fig. 4(b), which showed that the 1350 °C fRTP anneal resulted in similar profiles independent of the intermediate anneal temperature for the 5-keV preamorphization implant.

It was put forward that the plateau concentration that manifests during UHT annealing defines the concentration level below which B is active. This can be tested by comparing the measured R_s values to those obtained through a theoretical calculation that compensates for the inactive fraction by truncating the concentrations above the plateau concentration. The measured and calculated R_s values for the 48-keV preamorphization implant as well as the measured R_s values for the 5-keV preamorphization implant are shown in Fig. 6. The calculated data for the 5-keV preamorphization implant were not included due to the inability in accurately

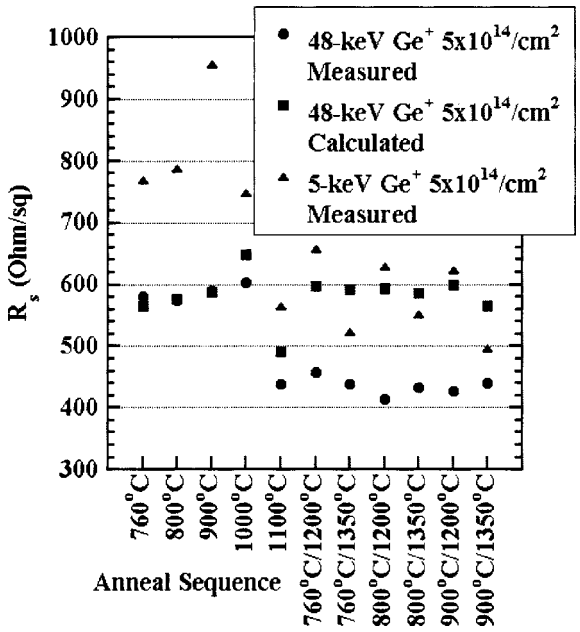

FIG. 6. Graph of the measured (●) and calculated (▲) R_s values obtained for the 48-keV Ge^+ pre-amorphization implant to 5×10^{14} cm^2 and the measured (_) values obtained for the 5-keV Ge^+ preamorphization implant to 5×10^{14} cm^2.

determining the appropriate plateau concentration. The calculated values were determined by using the following empirical mobility equation by Caughy and Thomas for Si:

$$\mu(x) = (\mu_a/\{1 + [n(x)/n_r]^{\alpha}\}) + \mu_b, \quad (1)$$

where $\mu(x)$ and $n(x)$ and are the mobility and carrier concentration as a function of depth, respectively, and μ_a, μ_b, n_r, and α are constants which depend on the carriers of interest.[35] The resulting $\mu(x)$ values were converted into sheet resistance by

$$R_s = 1/\{\Sigma_1[\Delta x_{i-1}\mu(x_i)n(x_i)q]\}, \quad (2)$$

where Δx is the difference in depth between two carrier concentration values obtained from the SIMS profile, and q is the charge of a free electron. As can be seen in Fig. 6, the 48-keV preamorphization implant results in lower R_s values compared to the 5-keV preamorphization implant for each annealing condition used in this study. For the 48-keV preamorphization implant, the measured and calculated R_s values match well for the iRTP anneals. This shows that, for an iRTP anneal, most of the activation occurs during ramp up to the annealing temperature (presumably caused by solute trapping during SPER of the implantation-induced amorphous layer). The fRTP data show that the high-temperature anneal significantly improves the R_s. The disagreement between the measured and calculated fRTP results for the 48-keV preamorphization implant shows that the active B concentrations are greater than those used in the calculation. One possible explanation for the improved R_s could be that the high-temperature anneal is sufficient to dissociate some of the initially clustered B atoms, which are only able to contribute to the active carrier concentration after such a high-temperature anneal. Additional work is required to better understand the difference among the calculated results and measured data.

CONCLUSIONS

High-power arc lamp design has enabled UHT annealing as an alternative to conventional RTP for ultrashallow junction formation. This technique heats the wafer to an intermediate temperature (e.g., 800 °C) before discharging a capacitor bank into flash lamps, which heat the device side of the wafer to a relatively high temperature (e.g., 1200 °C) for a few milliseconds. This time duration is significantly reduced from those obtained with conventional RTP, which are on the order of 1–2 s within 50 °C of the peak temperature. In this paper, we investigated the possibility of the UHT annealing technique forming a highly activated ultrashallow junction without being subjected to TED. It is shown that, of the 3.6 nm of diffusion that occurs during a 1200 °C UHT anneal for a 48-keV preamorphization implant, 3.0 nm is caused by B diffusion in α-Si before the complete recrystallization of the implantation-induced amorphous layer. The additional 0.6 nm of diffusion that occurred during the 1200 °C fRTP anneal is very close to what would be expected under equilibrium conditions (i.e., 1200 °C anneal for 3 ms). Although 3.8 nm of diffusion occurred for the 5-keV preamorphization implant during the same anneal, the diffusion that occurred in *c*-Si and is presumably caused by TED due to the close proximity between the excess interstitials and B atoms. Both preamorphization conditions show approximately 200 Ω/sq improvement in activation during a 1200 °C fRTP anneal (compared to the sample that was only annealed to the intermediate temperature); this improvement in R_s may be caused by the breaking up of initially clustered B atoms, but needs to be better understood. Dopant activation is degraded for the 5-keV preamorphization implant, presumably because the high local concentration of excess interstitials and B atoms results in inactive BIC formation during postimplant UHT annealing. This shows that a highly activated ultrashallow *p*-type junction can be formed without being subjected to TED only when the excess interstitials are sufficiently separated from the B atoms implanted near the substrate surface.

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