Application of flash-assist rapid thermal processing subsequent to low-temperature furnace anneals

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The substantial reductions in anneal times, such as in flash-assist rapid thermal processing (fRTP), place considerably more emphasis on the initial condition of the wafer, which may assume a greater role in the dictating diffusion product (Dt). Investigations have been conducted on the effect of low-temperature preanneals prior to fRTP on the extended defect nucleation and evolution and on boron activation. Czochralski grown *n*-type silicon wafers are preamorphized with 8 Ge^+ ions at a constant dose of 1×10^{15} cm^{-2} and then implanted with 1 keV, 1×10^{15} cm^{-2} B. Low-temperature furnace anneals are performed at 500 °C for 30 min and the wafers subsequently subjected to flash-assist RTP anneals in the range 1000–1300 °C. Four-point probe measurements indicate that the low-temperature anneal results in higher sheet resistance values. Plan-view transmission electron microscopy, secondary-ion-mass spectrometry, and Hall-effect measurements revealed no substantial differences in defect structure, junction depth, or mobility. However, the carrier density was found to be higher for those wafers which were preannealed. © *2006 American Vacuum Society.* [DOI: 10.1116/1.2140003]

I. INTRODUCTION

An essential requirement for the continued scaling of complementary metal-oxide semiconductor (CMOS) technology is to attain high levels of dopant activation while maintaining shallow layers and simultaneously increasing junction abruptness. Flash-assist rapid thermal processing (fRTP) operates in the time regime between laser thermal processing (LTP) and rapid thermal annealing (RTA), allowing anneal ramp rates on the order of 10^6 °C s^{-1}, thus making it extremely attractive as an annealing technique. The particularly high ramp and cooling rates allow for the attainment of very high anneal temperatures in exceedingly short times, thus resulting in reduced diffusions. Solid phase epitaxial regrowth (SPER) is also very attractive as it is capable of activating dopant levels that exceed equilibrium solid solubility levels in silicon. The low thermal budget applied to the lattice offers many advantages including minimal diffusion and therefore good junction depth control. However, one disadvantage of the process is the residual damage upon recrystallization of the amorphous layer. The following work will investigate the effects of combining these two processes on dopant activation, diffusion, and defect evolution.

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II. EXPERIMENT

This study utilized Czochralski grown, *n*-type silicon (100) wafers which were preamorphized with an 8 keV, 1×10^{15} cm^{-2} Ge^+ implant and subsequently implanted with 1×10^{15} cm^{-2} B^+ at an energy of 1 keV. Implants were performed at a standard tilt of 7° and twist of 27°. Low-temperature furnace anneals were then carried out on the whole wafers in an ASM International A400 furnace at 500 °C for a duration of 30 min. The low-temperature anneal time was selected to ensure regrowth of the amorphous layer produced. The wafers were then subjected to fRTP at Vortek Technologies. The flash anneal temperature profile entailed a ramp up to a 700 °C intermediate temperature (iRTP) at a rate of 150 °C s^{-1}, where the dwell time was 0 s. The temperature was then rapidly increased to flash temperatures of 1100 and 1300 °C at a rate $\sim10^6$ °C s^{-1}. The experimental control wafers were only subjected to the flash anneal for temperatures of 1000, 1100, 1200, and 1300 °C.

Extended defect analyses were performed via plan-view transmission electron microscopy (PTEM) on a JOEL 200 CX, operating at an accelerating voltage of 200 keV. PTEM samples were prepared by standard HF/HNO_3 backside etching methods and were imaged at g_{220} weak beam dark field (WBDF) conditions. The quantification technique of Bharatan *et al.*[1] was employed in the defect density analyses. Cross-sectional TEM (XTEM) samples were prepared utilizing a focused ion beam and the method was used to confirm the regrowth of the amorphous layers, which were imaged

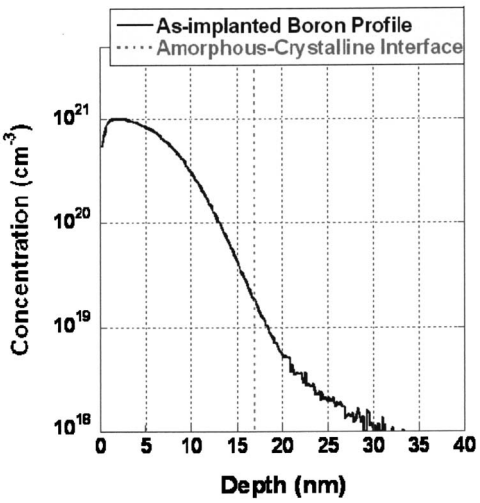

FIG. 1. Position of the as-implanted 1 keV, 1×10^{15} cm^{-2} B profile relative to the 17 nm amorphous layer produced by an 8 keV, 1×10^{15} cm^{-2} Ge PAI in (100) Si.

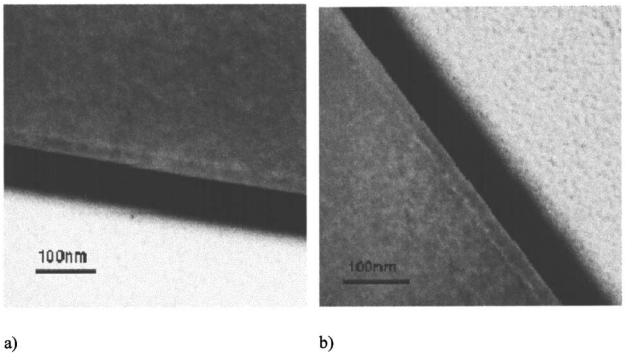

FIG. 2. XTEM images taken at g_{110} bright field conditions of the regrown amorphous layers after (a) 500 °C 30 min furnace anneal and (b) 700 °C intermediate temperature RTP.

under g_{110} bright field conditions. Dopant concentration-depth profiles were assessed by secondary-ion-mass spectroscopy (SIMS) using an adept 1010 Dynamic SIMS System by Physical Electronics. A 25 nA, 1 kV oxygen beam with a 10% gating and a raster of 250 μm^2 was employed in the data acquisition. Sheet resistances were measured on a 4Dimensions 333A four-point Probe system, while the Hall measurements conducted on a MMR Technologies Van der Pauw Hall System were utilized to determine carrier concentrations and mobilities.

III. RESULTS AND DISCUSSION

The concentration-depth profile for the as-implanted B into the Ge preamorphized silicon layer is indicated in Fig. 1. It can be seen that the 8 keV Ge PAI produced an amorphous layer of ~16 nm which was confirmed by XTEM (image not shown). It is also evident that the B implant produced a peak concentration of $\sim1\times10^{21}$ cm^{-3} with a projected range of ~3 nm and a junction depth, measured at a concentration of 1×10^{18} cm^{-3}, of 30 nm. Application of the low-temperature furnace anneals at 500 °C resulted in complete recrystallization of the amorphous layer by SPER. In the experimental control, however, SPER of the amorphous layer was achieved during the ramp up to the 700 °C intermediate temperature, prior to application of the high-temperature flash anneal. XTEM images of the regrown layers are shown in Fig. 2, in which the end of range (EOR) damage can be seen at a depth of 20 nm below the surface.

Sheet resistance measurements were carried out to determine the effect of increasing the flash temperature above the intermediate temperature and also to establish whether the application of the low-temperature furnace anneals resulted in any noticeable differences. Figure 3 is plot of the measured sheet resistance as a function of flash temperature. Clearly, the sheet resistance falls of as the flash temperature is increased above the intermediate temperature for the two cases investigated. In the experimental control, temperatures of 1000 and 1100 °C did not effect any gains in sheet resistance over the 700 °C iRTP anneal, with values ~550 Ω/□. However, as the flash temperature was increased to 1200 and 1300 °C, the sheet resistance rapidly fell off to values of ~460 and 287 Ω/□, respectively. A similar trend was observed for samples which were subjected to the low-temperature anneals at 500 °C. Since XTEM analyses confirmed the regrowth of the amorphized layers after the low-temperature preanneal and during the ramp up to the intermediate temperature in the experimental control, it can be inferred that the gains in sheet resistance observed above 1200 °C were not due to increased activation resulting from SPER.

Another obvious feature of the plot is the higher sheet resistances obtained on application of the low-temperature preanneal. Values of ~740, 620, and 330 Ω/□ were attained

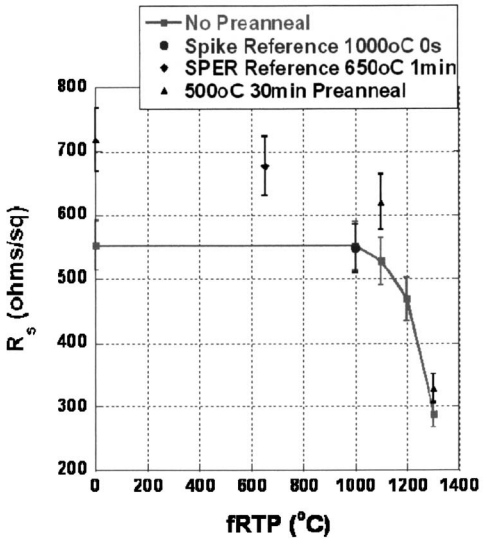

FIG. 3. Sheet resistance, R_s vs flash temperature, fRTP of (100) Si with an 8 keV, 1×10^{15} cm^{-2} Ge PAI containing 1 keV 1×10^{15} cm^{-2} B. Highlights the effects of a 500 °C 30 min furnace anneal prior to a flash anneal with a constant intermediate temperature of 700 °C and flash temperatures ranging 1000–1300 °C.

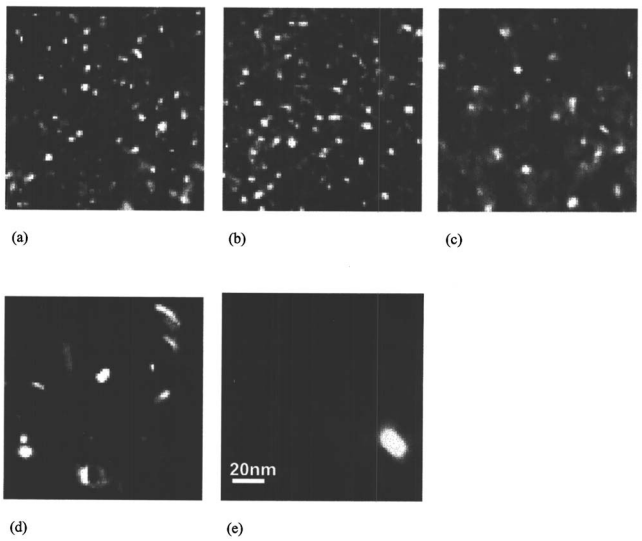

FIG. 4. PTEM WBDF images of the EOR damage in (100) Si containing an 8 keV, 1×10^{15} cm^{-2} Ge PAI and 1 keV, 1×10^{15} cm^{-2} B taken at g_{220} two beam diffraction conditions. The samples were flash annealed at (a) 700 °C iRTP; (b) 700 °C iRTP, 1000 °C fRTP; (c) 700 °C iRTP, 1100 °C fRTP; (d) 700 °C iRTP, 1200 °C fRTP; and (e) 700 °C iRTP, 1300 °C fRTP.

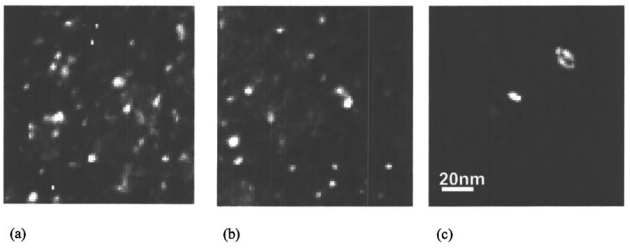

FIG. 5. PTEM WBDF images of the EOR damage in (100) Si containing an 8 keV, 1×10^{15} cm^{-2} Ge PAI and 1 keV, 1×10^{15} cm^{-2} B taken at g_{220} two beam diffraction conditions. The samples were preannealed at 500 °C for 30 min in a furnace and subsequently flash annealed at (a) 700 °C iRTP; (b) 700 °C iRTP, 1100 °C fRTP; and (c) 700 °C iRTP, 1300 °C fRTP.

for the preannealed wafers after application of the 700 °C intermediate temperature and 1100 and 1300 °C flash temperatures, respectively. Thus the low-temperature anneals effected increases of approximately 34% for the 700 and 1100 °C, and 14% for the 1300 °C flash temperatures.

It is known that lattice impurities such as extended defects could act as scattering sites that reduce carrier mobility and hence increase the sheet resistance values.[2] PTEM was therefore conducted to determine whether the microstructural differences were, in part, responsible for the differences in sheet resistance observed. Figure 4 indicates the PTEM images of the extended defects in the flash annealed control samples. Dotlike interstitial clusters populated the microstructure after the 700 °C intermediate temperature anneal. On application of the 1000 °C flash temperature, few differences could be discerned in the extended defects. However, as the flash temperature was increased to 1100 °C, the defect density clearly decreased and the defects appeared as small loops. At 1200 °C, the defect evolution was more apparent as 311-type defects and larger dislocation loops of smaller density were present in the microstructure. This is consistent with a nonconservative Ostwald-type ripening behavior in which the larger defects grow at the expense of the smaller ones. Additional coarsening and defect dissolution occurred as the flash temperature was raised to 1300 °C, at which very few dislocation loops were seen. Visibly, the application of high-temperature flash-assist RTP was capable of evolving the EOR defects into stable dislocation loops, while simultaneously dissolving the defects. This is advantageous from a leakage as well as mobility standpoint and may account for some improvement in the measured sheet resistance between 1100 and 1300 °C, as a reduction in the number of extended defects decreases the probability of scattering events.

Examination of the EOR damage in the preannealed samples indicated that the additional low-temperature thermal step did not effect any noticeable microstructural change. The defect morphology and the evolution for both low-temperature anneals investigated, appeared to follow a similar pathway to the experimental control, evolving from dotlike interstitial clusters at the 700 °C intermediate temperature anneal to stable dislocation loops observed after the 1300 °C flash. The WBDF images of the EOR damage are illustrated in Fig. 5. Defect counts confirm no significant difference in both the defect density and the trapped interstitial population, between the experimental control and the preannealed samples, as shown in Fig. 6. These similarities in the microstructure thus eliminated EOR lattice imperfections as a possible cause for the increased sheet resistance observed on application of the low-temperature anneals.

SIMS analyses were therefore performed to establish whether the differences in the sheet resistance were the result of variations in the layer thickness. Figure 7 shows the diffused profiles for the flash annealed samples in the experimental control. It is evident that application of the 700 °C intermediate temperature resulted in some noticeable diffusion, for concentrations between 1×10^{19} and 2×10^{18} cm^{-3}. This region coincides with the EOR damage layer and may therefore be indicative of the initial stages of boron gettering to the EOR.[3] At 700 °C the solid solubility of boron in crystalline silicon has been estimated at 2×10^{19} cm^{-3}.[4] However, the SIMS analyses demonstrated that a boron solubility of 1×10^{19} cm^{-3} was achieved on application of the 700 °C intermediate temperature. Above this concentration the boron peak appeared to be immobile, which is consistent with the formation of boron interstitial clusters (BICs). The high interstitial concentrations generated by the ion implantation process have been demonstrated to result in the clustering of boron atoms at concentrations far below its solid solubility.[5] Thus BIC formation could account for the lower solid solubility observed in the diffusion profiles.

Clearly the application of the flash anneal resulted in further diffusion of the boron profiles. As the flash temperature was increased from 1000 to 1300 °C there was a concomitant increase in the diffusion. In particular, the boron pile up in the EOR seemed to increase for flash temperatures ranging 1000–1200 °C. However, at 1300 °C the pile up was no

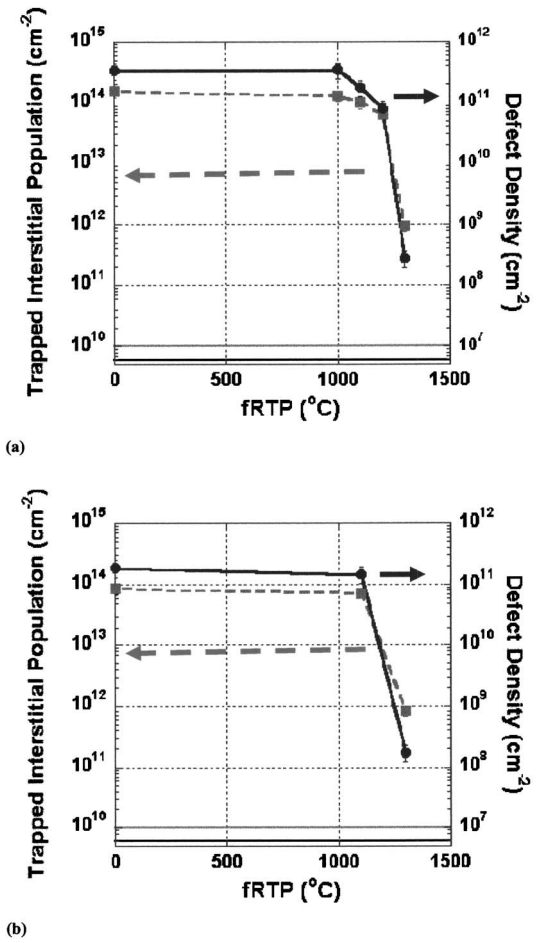

FIG. 6. Defect density and trapped interstitial population vs flash temperature for (100) Si containing an 8 keV, 1×10^{15} cm^{-2} Ge PAI and 1 keV, 1×10^{15} cm^{-2} B. (a) Samples flash annealed between 1000 and 1300 °C, fRTP from a constant iRTP of 700 °C (b) Samples preannealed at 500 °C for 30 min in a furnace prior to application of the flash RTP.

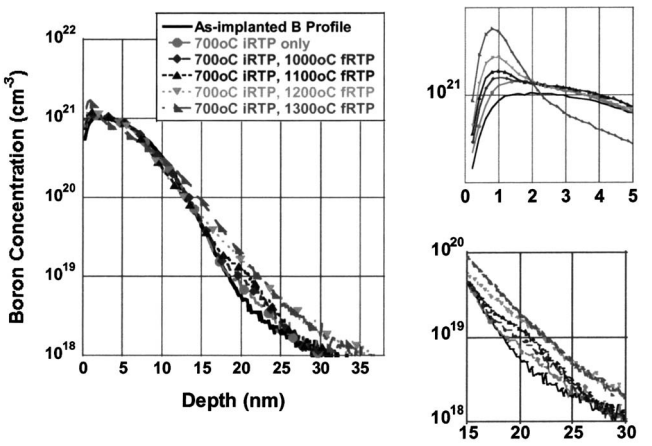

FIG. 7. Boron concentration-depth profiles for a 1 keV, 1×10^{15} cm^{-2} B implant in Si (100) preamophized with 8 keV, 1×10^{15} cm^{-2} Ge PAI. Flash anneals were performed from a constant of 700 °C intermediate temperature for flash temperatures ranging 1000–1300 °C.

longer visible. This behavior correlates very well with the PTEM analyses which confirmed the existence of the EOR damage and it's dissolution with increased flash temperature. Examination of the diffusion profile tails indicated that there was no significant junction motion during the 1000 and 1100 °C flash anneals. The junction depths at these temperatures coincided with that of the as-implanted profile at 30 nm, measured at a concentration of 1×10^{18} cm^{-3}. However, as the flash temperature was increased to 1200 and 1300 °C the tail of the profiles appeared to diffuse to ~35 nm. This increased motion was most likely due in part to the interstitial release from the EOR, since the PTEM analyses indicated the increased defect dissolution at these temperatures. The fact that the junction depth at 1200 and 1300 °C flash temperatures coincided is peculiar, since there was considerable difference in the defect density and trapped interstitial population detected at these temperatures. The estimated number of trapped interstitials fell drastically between the 1200 and 1300 °C anneals, from a value of ~7×10^{14}– ~9×11^{14} cm^{-3}, respectively. One would therefore have expected these interstitials to contribute to additional diffusion of the profile tail. This was clearly not the case.

Careful scrutiny of the near surface region of the boron profiles revealed pile up of boron within the first 1.5 nm, for temperatures ranging 1100–1300 °C. This boron pile up was largest for the highest flash temperature. There have been many reports in the literature that boron can exhibit an uphill diffusion[6,7] and in some cases the boron pile up has been observed to be in the vicinity of the surface or an interface.[8] Such effects have been suggested to result from the implantation-induced gradients in interstitial concentration due to localized interstitial clustering or related effects.[9] However, process simulators have been unable to reproduce surface or interface pileup effects based on this picture.[8] Clearly from this data set, the number of released interstitials from the EOR damage dissolution, between the 1200 and 1300 °C flash anneals, in particular, was insufficient to account for the pileup observed at the surface. Another mechanism must therefore be responsible for this behavior. Recently, Dev *et al.*[10] demonstrated that the band bending at the $Si-SiO_2$ interface is comparable in magnitude to the near-surface band bending induced by electrically charged defects on atomically clean silicon surfaces. Their experiments demonstrated that this band bending existed for a wide range of times and temperatures of interest in conventional ion implantation technology. Jung *et al.*[11] utilized FLOOPS-based numerical simulations,[12] to investigate the effects that this bending can have on dopant profiles and demonstrated that the $Si-SiO_2$ interface bending provides a mechanism to explain the pileup of electrically active boron. These boron atoms were believed to be liberated from clusters during annealing. Examination of the concentration peak of the 1300 °C flash annealed sample, revealed a large portion of the initially immobile peak moved in the direction of the surface, suggestive of possible boron cluster dissolution, in accordance with the theories of Jung *et al.* This possible cluster dissolution and boron reactivation coupled with the

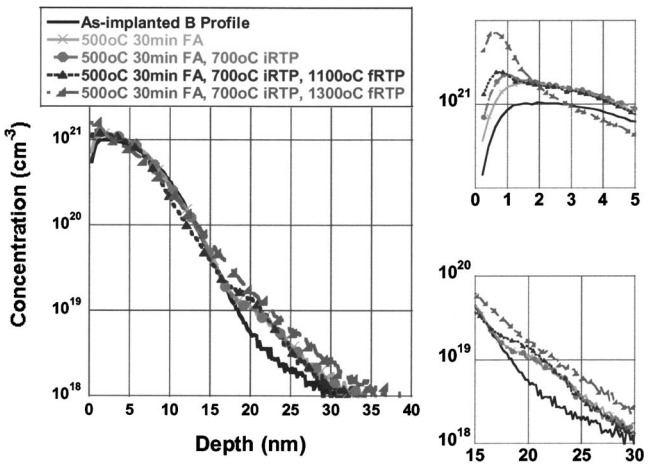

FIG. 8. Boron concentration-depth profiles for a 1 keV, 1×10^{15} cm^{-2} B implant in Si (100) preamophized with 8 keV, 1×10^{15} cm^{-2} Ge PAI. The samples were preannealed in a furnace at 500 °C for 30 min prior to flash annealing. Flash anneals were performed from a constant of 700 °C intermediate temperature for flash temperatures ranging 1000–1300 °C.

significant diffusion observed may contribute to the appreciably lower sheet resistance values obtained for the 1300 °C flash annealed wafer.

SIMS analyses for the samples which were subjected to the low-temperature preanneal are illustrated in Fig. 8. Inspection of the concentration profile indicated many similarities in diffusion behavior to the experimental control. In general, an increase in the flash temperature resulted in increased diffusion and therefore junction depth, as one would expect. Also, the boron pileup at the surface was evident and was highest for 1300 °C flash anneal. However, further examination of the diffused profiles during the low temperature 500 °C 30 min anneal revealed substantially more diffusion than during the 700 °C intermediate temperature in the experimental control. This is demonstrated in Fig. 8, in which it can be seen that the profile diffused between concentrations of $\sim1.5\times10^{19}$ and 1×10^{18} cm^{-3}, which were below the original amorphous layer, in the crystalline region. This region was synonymous with the EOR damage and hence the boron pileup may be attributed with gettering to EOR,[3] as seen in the control. The peak of the profile, above concentrations of $\sim1.5\times10^{19}$ cm^{-3}, appeared immobile, which suggests that there was either very little or no diffusion in the amorphous layer, during recrystallization. This is not inconceivable since the amorphous layer was very shallow and should have taken approximately 5 min to regrow, based on an Arrhenius-type relation with an activation energy of 2.59 eV,[13] leaving approximately 25 min for diffusion of the mobile region of the profile. Previous reports of boron diffusion in the amorphous phase utilized deeper preamorphizing implants[14] and/or fluorine,[15] which is known to slow down the recrystallization rate, to allow enough time for boron to diffuse in the amorphous layer. In this case the time spent in the amorphous phase may have been too short for any appreciable boron diffusion. Furthermore, subjection of a 700 °C intermediate temperature to the preannealed sample resulted in no additional diffusion. This was quite evident since these diffused profiles coincided, implying that the additional thermal budget was insufficient to advance the diffusion.

In the case of the 1100 °C flash anneal, despite the fact that the preannealed sample exhibited some diffusion during the low-temperature stage; the diffused profile was remarkably similar to the experimental control. Likewise, the 500 °C low-temperature anneal did not effect any substantial change to the 1300 °C flashed profile. One would have expected the sample that had the "head start" on diffusion to have diffused more, which was not so. Thus one could reasonably conclude that the differences observed in the sheet resistance were not due to differences in layer thickness.

Initial Hall measurements have been conducted which indicate no substantial change in mobility within the experimental error, on increasing the flash temperature. Also, the mobility attained for the samples which were preannealed were very similar to those of the experimental control. These seem to suggest that the differences in sheet resistance between the samples which were subjected to the low-temperature preanneal and the control samples may be due to differences in the carrier density. An important element of the experiment is the anneal step during which the recrystallization of the amorphous region occurred. During the low-temperature preanneal the amorphous layer was totally regrown prior to the application of the flash. In the case of the control samples recrystallization occurred during the 700 °C intermediate anneal, before the flash was applied to the wafer. Thus the higher sheet resistance values attained for the preannealed samples may be related to the recrystallization temperature.[16–18] If higher activation levels can be achieved at higher recrystallization temperatures, then the samples which were recrystallized during the 500 °C 30 min anneal should have a lower activation than those which were crystallized during the 700 °C intermediate temperature. This would explain why application of the flash anneal to the preannealed wafers did not effect sheet resistance values which were comparable to the control. However, this also suggests that the use of a high-temperature flash anneal after total recrystallization of an amorphous layer does not necessarily effect improvements in activation. If this is the case, in the experimental control in which all the samples were recrystallized at 700 °C, one would expect the activation to be the same for flash temperatures between 1000 and 1300 °C. The Hall measurements indicate differently; the activation is constant for flash temperatures 1000–1200 °C and much higher for the 1300 °C flash anneal. Therefore the reductions in sheet resistance observed as the flash temperature was raised from 1000 to 1200 °C, may be due to an increase in the layer thickness at 1200 °C. Since the layer depth at 1300 °C coincided with that of the 1200 °C, the substantially lower sheet resistance obtained could be accounted for by possible boron cluster dissolution, with a resultant diffusion of boron toward, and pile up at the interface of electrically active boron, alluded to by Jung *et al.*[11] The same would apply for the preannealed samples which demonstrated similar behavior.

IV. CONCLUSION

Flash-assist RTP has been demonstrated to evolve the residual EOR damage associated with amorphized silicon, with minimum junction diffusion, while still attaining highly active layers. This is extremely advantageous from both a leakage and junction depth perspective. The effect of employing this technique with low temperature SPER, which is known to result in a metastable activation of dopants to levels above equilibrium solid solubility, has been investigated. The findings in this work demonstrate the low-temperature process effects increases in sheet resistance, which have been attributed to reductions in carrier density associated with lower activation levels achieved at the low recrystallization temperature.

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