

# Dissolution of extended defects in strained silicon

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The experimental and theoretical analyses performed in this work provide an insight into the impact of external stress on extended defects that form in silicon after ion implantation. It is shown experimentally that the embedded SiGe source/drain regions help to dissolve the extended defects in the adjacent silicon. The reduced amount of free and clustered interstitials is known to reduce junction leakage and increase dopant activation. These benefits are expected to improve further for the subsequent technology generations, due to the shrinking distance between the source and drain SiGe regions. A quantitative model of defect evolution in silicon with embedded SiGe is proposed. The model can be applied to optimize the combination of stress engineering, implant conditions, and thermal budget for the best device performance.

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## I. INTRODUCTION

Stress engineering is becoming an industry-wide practice to enhance the device performance. This work addresses some of the unexplored side effects of stress engineering. Specifically, the formation, evolution, and dissolution of the implant-induced dislocation loops and {311} defects are driven by minimization of free energy. The elevated levels of free energy around the defects reflect mechanical stress in the disturbed silicon lattice.<sup>1</sup>

Upon ion implantation, each of the implant-induced silicon self-interstitials creates compressive stress around it. When several interstitials combine together to form a small interstitial cluster, they still create compressive stress in the adjacent silicon lattice, but it is lower than the total stress generated by the same number of separate interstitials. Small interstitial clusters exhibit Ostwald ripening, evolving into larger {311} oriented rod-like defects, and then into even larger plate-like {111} dislocation loops. During this defect evolution, each interstitial creates smaller and smaller stress as the size of extended defect increases. The Ostwald ripening leads to eventual dissolution of the extended defects, which further reduces compressive stress in the silicon lattice.

Given such a profound role of stress in defect formation, it is expected that external stress generated as a result of stress engineering will affect evolution of the extended defects. *Ab initio* analysis of {311} dissolution under external stress has shown dramatic impact of the typical stress levels on defect dissolution time.<sup>2</sup>

## II. EXPERIMENT

In this work, we use an experimental setup similar to the one reported in Ref. 3. The Si wafers with embedded 100 nm thick Si<sub>0.8</sub>Ge<sub>0.2</sub> layers of varying widths are implanted with  $3 \times 10^{15} \text{ cm}^{-2}$  As<sup>+</sup> at 40 keV and annealed either at 800 or 900 °C. The plan-view transmission electron microscope (PTEM) measurements were used to analyze the defect evolution in silicon and Si<sub>0.8</sub>Ge<sub>0.2</sub>. Weak beam dark field g220 imaging conditions were used in which the g vector is parallel to the Si<sub>0.8</sub>Ge<sub>0.2</sub>/Si interface. Thus the misfit dislocations parallel to the interface are not visible and only those misfit dislocations in the SiGe perpendicular to the interface are visible.

Figure 1 shows a typical PTM image of dislocation loops in the vicinity of the strained Si<sub>0.8</sub>Ge<sub>0.2</sub> layer. In this case, the Si<sub>0.8</sub>Ge<sub>0.2</sub> layer is narrow (about 200 nm), whereas the silicon width in between the Si<sub>0.8</sub>Ge<sub>0.2</sub> layers is large (over 1 μm). A defect-free denuded zone is visible within several tens of nanometers from the Si<sub>0.8</sub>Ge<sub>0.2</sub> layer. Beyond this denuded zone, silicon is littered with dislocation loops of up to 50 nm in diameter. These dislocation loops form as a result of ripening of the interstitial defects that are induced by the arsenic implant. Inside the Si<sub>0.8</sub>Ge<sub>0.2</sub> layer, a network of misfit dislocations is formed. Both the observed density of misfit dislocations as well as the micro-Raman stress measurements for similar structures performed in Ref. 3 indicate that the amount of stress relaxation due to dislocations is under 10%. Over 90% of the lattice mismatch stress is retained, making it possible to use embedded SiGe source/drain to improve p-type metal-oxide-semiconductor field effect transistor (pMOSFET) performance. The misfit dislocations were only observed after the arsenic implant and annealing, and not observed right after SiGe epitaxy.

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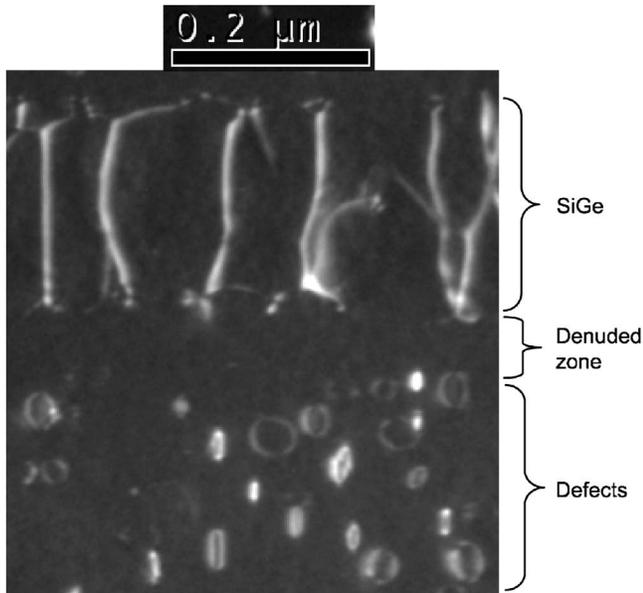


FIG. 1. PTM image of the wafer annealed for 10 s at 900 °C.

Figure 2 shows a top view TEM image of a narrow (170 nm wide) silicon stripe surrounded by the wide  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layers. To complement the previous PTM images, Fig. 3 shows several alternating narrow silicon and  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layers.

All four images exhibit similar defect patterns, with stress relaxation dislocations in  $\text{Si}_{0.8}\text{Ge}_{0.2}$ , implant-induced dislocation loops in silicon, and a denuded zone in silicon next to  $\text{Si}_{0.8}\text{Ge}_{0.2}$ . When two denuded zones overlap in the 100 nm wide silicon stripe as can be seen on the left in Fig. 3, most of the dislocation loops disappear. The size and density of

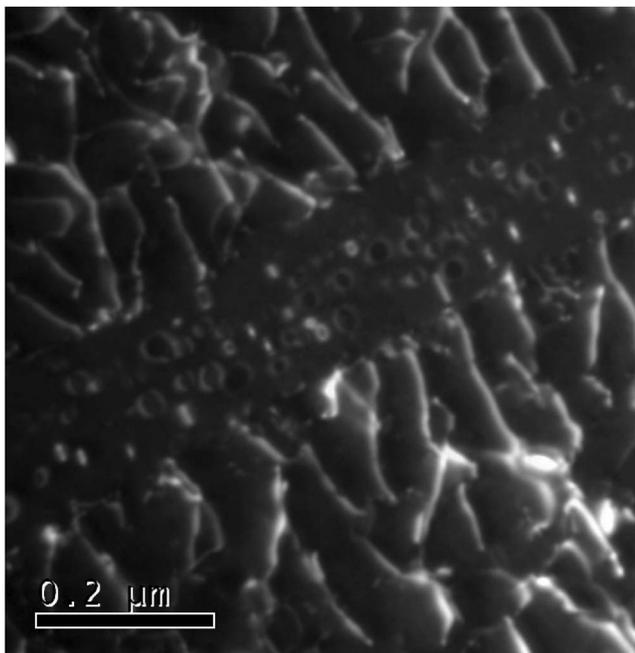


FIG. 2. PTM image of the wafer annealed for 200 min at 800 °C.

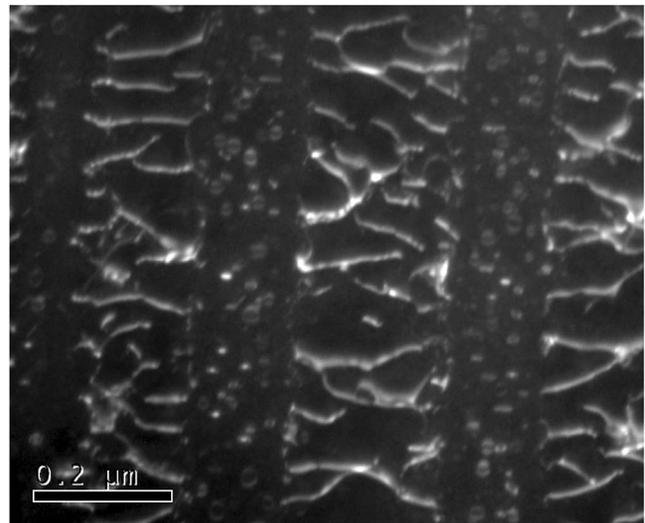


FIG. 3. PTM image of the wafer annealed for 25 min at 800 °C.

the dislocation loops away from denuded zone is similar to those observed in control stress-free areas of the silicon wafer.

### III. ANALYSIS

The defect formation, evolution, and dissolution have been studied using the kinetic Monte Carlo (KMC) process simulator.<sup>4,5</sup> Figure 4 shows stress distribution within  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layer as well as in the adjacent silicon. Stress is generated by the lattice mismatch and is not affected by the temperature ramps. Therefore, the defect evolution that happens at elevated temperatures experiences the same stress. It can be seen from Fig. 4(a) that the  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layer and some of the adjacent silicon are under compressive stress (i.e., positive hydrostatic pressure, shown as light gray). However, silicon in the immediate vicinity of the Si/SiGe interface is under tensile stress (i.e., negative hydrostatic pressure, shown as dark gray).

Figure 4(b) demonstrates pressure distributions in the lateral direction across the Si/SiGe interface. The  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layer is compressed both at the surface and in the bulk. Along the surface, silicon is also compressed, which is why the embedded SiGe source/drain regions are used to induce compressive stress into the  $p$ MOSFET channel that is located on the silicon surface. The compressive channel stress enhances the hole mobility which improves the  $p$ MOSFET performance. In the bulk, 50 nm below the surface, silicon region immediately adjacent to the interface is under tension, eventually turning into compression away from the interface. This stress behavior in the bulk does not affect the transistor performance, but this is where the implant-induced extended defects form, making it important for this study.

Different widths of the silicon and  $\text{Si}_{0.8}\text{Ge}_{0.2}$  layers change the absolute level of stress, but exhibit the same qualitative stress pattern in terms of locations of the compressive and tensile areas. For the structures with wide  $\text{Si}_{0.8}\text{Ge}_{0.2}$  and narrow silicon layers, compressive stress ex-

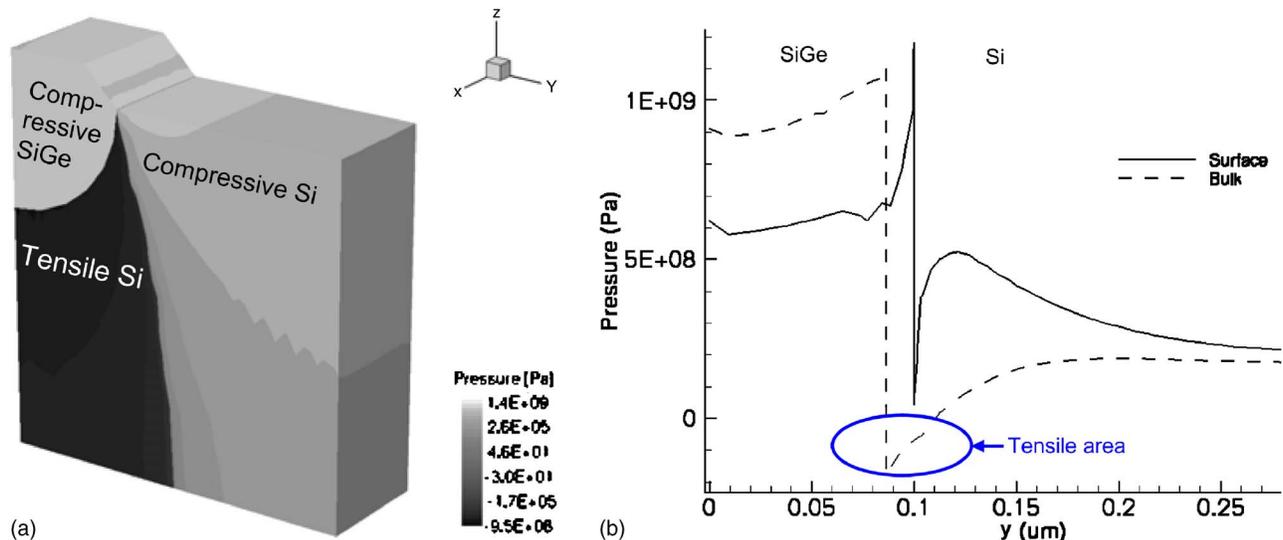


FIG. 4. Distribution of hydrostatic pressure in SiGe layer and adjacent silicon. Three-dimensional distribution (a) and distribution along the surface and at a 50 nm depth (b).

ceeds 1 GPa at the silicon surface and approaches 500 MPa in the bulk at a typical depth of extended defect formation.

All simulations in this work were done assuming standard impact of stress on diffusivities and equilibrium concentrations of the point defects.<sup>5</sup> However, turning off these effects did not noticeably change simulation results, which means that the experiments performed in this work are driven by the properties of extended defects rather than point defects.

Following intuition and *ab initio* results obtained in Ref. 2, we assumed that the extended defects have stress-dependent binding energy  $E_b = E_b^{\text{relaxed}} \exp(-P\Delta V/kT)$ , which is higher under tension and lower under compression with the activation volume of  $\Delta V = +0.02 \text{ nm}^3$ . Here,  $E_b^{\text{relaxed}}$  is the defect binding energy in a silicon lattice without the external stress and  $P$  is hydrostatic pressure. This stress dependence applies to all interstitial clusters, including small interstitial clusters,  $\{311\}$ s, and dislocation loops using the same activation volume. Simulated results, depicted in Fig. 5 exhibit extended defect behavior that is opposite to the one observed in PTEMs. Specifically, extended defect density somewhat increases in the vicinity of Si/SiGe interface, contradicting the measurements.

This might lead one to an idea that the reversed stress dependence of the defect binding energy should reverse the

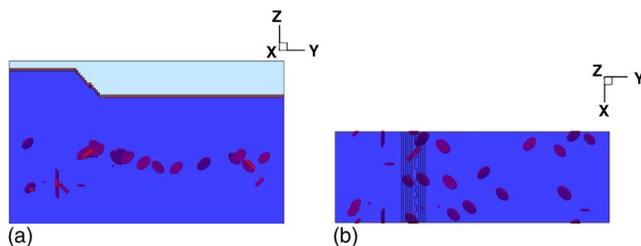


FIG. 5. Simulated distribution of extended defects assuming that defect formation energy is favorable inside tensile lattice and unfavorable inside compressive lattice. Side view (a) and top view (b).

defect pattern and therefore describe the experiments. Simulated results under this assumption with the negative activation volume of  $\Delta V = -0.02 \text{ nm}^3$  are shown in Fig. 6. The defect distribution still does not match the PTEMs.

After seeing both possible stress dependent models fail, we turned the stress dependency off and assumed that the Si/SiGe interface is trapping interstitials, effectively acting as a recombination center. A typical defect distribution simulated under this assumption is shown in Fig. 7. This time, there is a clear denuded zone formed next to the Si/SiGe interface in agreement with the measurements.

The model that successfully describes the experimentally observed defect patterns contradicts *ab initio* results reported in Ref. 2. Additional experimental and theoretical study will be instrumental in resolving the apparent contradiction. Our results do not necessarily rule out stress dependence of the defect binding energy. Instead, they mean that the possible stress dependence is so weak that it does not noticeably affect the defect Ostwald ripening kinetics and in our experimental setting is eclipsed by the stronger effect of interstitial trapping at the Si/SiGe interface.

Figure 8 shows the impact of trapping efficiency of the Si/SiGe interface on the width of the denuded zone. These results indicate that it is not necessary to have a perfect in-

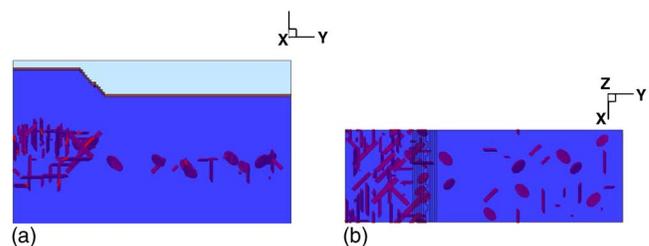


FIG. 6. Simulated distribution of extended defects assuming that defect formation energy is favorable inside compressed lattice and unfavorable inside tensile lattice. Side view (a) and top view (b).

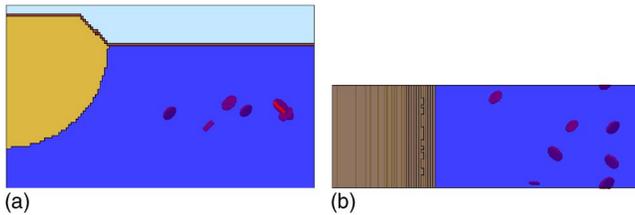


FIG. 7. Simulated distribution of extended defects assuming that defect formation energy is stress independent and that the Si/SiGe interface traps interstitials. Side view (a) and top view (b).

terstitial sink at the Si/SiGe interface to form a distinct defect-free denuded zone. Whenever interstitials have trapping probability of 1% or higher, a 50 nm wide denuded zone is observed.

This observation might shed some light on the trapping mechanism involved here. Specifically, Listebarger *et al.* report experimental evidence of dislocations acting as an interstitial sink.<sup>6</sup> Let us assume that a misfit dislocation has 100% probability of trapping the interstitials with a capture radius of 0.387 nm. Then the typical dislocation density observed in this work translates into traps covering about  $1\% \pm 0.5\%$  of the interface area. This number is close to the minimum necessary trap density estimated using KMC calculations, which makes this mechanism a likely explanation of the apparent interstitial trapping.

Practical implications of our findings can be summarized as follows. Further transistor scaling inevitably pushes a variety of interstitial trapping interfaces such as the Si/SiGe interface closer to each other. The closer proximity of interstitial trapping interfaces to the implant-induced damage helps to dissolve the damage and associated extended defects faster. This brings about several positive trends that accompany transistor scaling. First, reduced interstitial concentration improves dopant activation as there are fewer interstitials to form a variety of boron-interstitial clusters and phosphorus-interstitial clusters. Second, the dopants experience less transient-enhanced diffusion which makes it easier to form shallow junctions. Third, a lower thermal budget can be used to anneal the implant-induced damage and keep the junction leakage under control.

#### IV. CONCLUSIONS

The experimental and theoretical analyses performed in this work provide an insight into the impact of external stress

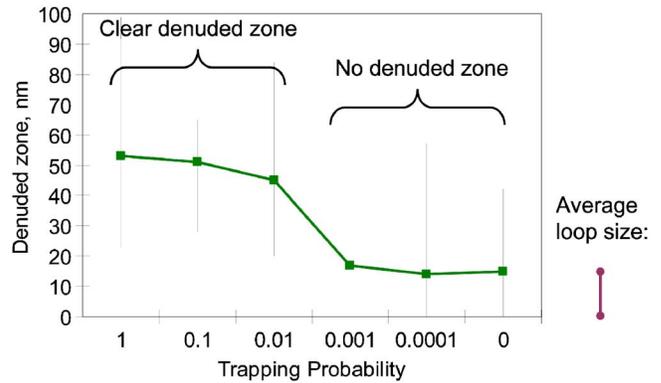


FIG. 8. Simulated width of denuded zone as a function of the interstitial trapping efficiency of the Si/SiGe interface. The trapping probability means the probability for an interstitial to get trapped when it encounters the Si/SiGe interface. The vertical bars show the data ranges obtained in 5 randomized KMC simulations per each probability. The thick line shows average width of the denuded zone.

on extended defects that form in silicon after ion implantation. It is shown experimentally that the embedded SiGe source/drain regions help to dissolve the extended defects in the adjacent silicon. The reduced amount of free and clustered interstitials is known to reduce junction leakage and increase dopant activation. These benefits are expected to improve further for the subsequent technology generations, due to the shrinking distance between the source and drain SiGe regions. A quantitative model of defect evolution in silicon with embedded SiGe is proposed. The model can be applied to optimize the combination of stress engineering, implant conditions, and thermal budget for the best device performance.

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