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Modeling Solid Phase Epitaxial Growth for Patterned Ge Substrates

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Modeling the two-dimensional (2D) solid phase epitaxial growth (SPEG) of amorphized Ge has become important due to the renewed interest in Ge as an alternative material to Si in complementary metal-oxide-semiconductor (CMOS) devices. In this work, a 2D SPEG model that uses level set techniques as implemented in the Florida object oriented process simulator (FLOOPS) to propagate regrowth fronts with variable crystallographic orientation patterned material is presented. Apart from the inherent orientation dependence of the SPEG velocity, it is established that nitride-induced stress can affect mask edge defect formation for patterned samples. Data acquired from transmission electron microscopy (TEM) experiments matches well with simulations, thus providing a stable model for simulating 2D regrowth and mask edge defect formation in Ge. In comparison to Si, mask edge defect formation is less apparent in Ge due to a more isotropic orientation dependence for Ge SPEG.
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Solid phase epitaxial growth (SPEG) is a common method of achieving high dopant activation for ultra shallow junctions in Ge.[1–3] SPEG describes the crystallization of an amorphous layer that adopts the crystallographic orientation of the substrate and typically takes place in the source and drain regions of CMOS devices. As silicon nears the end of its roadmap, Ge is an attractive alternative material due to its higher free carrier mobility and dopant activation. One dimensional (1D) SPEG has been well documented for Ge,[4–8] but little work has been done on 2D SPEG in Ge substrates.

The velocity of the amorphous-crystalline (α-c) interface for Ge is known to be thermally activated with an activation energy of 2.17 eV.[7,8] The velocity obeys the Arrhenius-type relationship given by

$$v = v_0 \exp\left(\frac{-\Delta G}{kT}\right) \quad [1]$$

where v_0 is a temperature independent prefactor, $\Delta G = 2.17$ eV is the activation energy, $k = 8.62 \times 10^{-5}$ eV/K is Boltzmann's constant, and T is the absolute temperature.[9–11] Additionally, SPEG is affected by the crystallographic orientation at the α-c interface, dopant impurities, and applied stress.[5,12–15]

Unlike one dimensional (1D) SPEG for blanket implants, the source and drain regions are typically patterned, which results in curved α-c interfaces. This is essentially a three dimensional (3D) process, but in the case of one of the dimensions of the structure being very long, it can be simplified to a two dimensional (2D) process. In this study, a line pattern was chosen where the length (dimension into the page for all the figures) is very long (hundreds of microns), which is a good assumption for many devices.

The crystallographic orientation dependence is important to consider for 2D SPEG. The normalized regrowth velocity as a function of crystallographic orientation $f(\theta)$ for Ge has been measured by TEM from [001] to [011].[16] The SPEG velocity as a function of θ can be expressed as

$$v(\theta) = v_{[001]} \cdot f(\theta) \quad [2]$$

where $v_{[001]}$ is the value of v along the [001] and $f(\theta)$ is temperature independent and can be fit using a fourth order polynomial fit. For Ge, the [001] regrowth velocity is 16 times faster than the slowest regrowth direction of [111] and 1.4 times faster than the [011] direction.

The SPEG velocity of the [001] and [011] directions are much faster than that of the [111]. This causes the vertical and lateral epitaxial fronts to meet when a masked implant recrystallizes. The [111] front becomes pinched off, resulting in what is known as a mask edge defect.[17–19] These defects are highly sensitive to stress, and tend to be more pronounced when formed under compressive stress.[20] From a modeling perspective, it is important to be able to predict the formation of mask edge defects as they can affect the short channel mobility and drive current of devices.[21,22]

The goal of this work is to study and simulate the 2D SPEG process for Ge in order to gain an understanding of how Ge crystallizes and the mask edge defects that form during this process. This work will also attempt to compare the multidirectional SPEG process of Ge with that of Si.

Experimental

For this work, 110 nm of Si_3N_4 was deposited on a Ge (001) wafer using a plasma enhanced chemical vapor deposition (PECVD) tool at 300°C. The wafer was then spin coated with 250 nm of PMMA resist and baked at 170°C for 30 min. E-beam lithography was used to create line regions on the wafer aligned along [011] directions. Reactive ion etching (RIE) consisting of a 1 min SF_6 treatment was used to expose ~300 nm regions of Si_3N_4 separated by ~350 nm. The Si_3N_4 was purposely under-etched by ~10 nm to prevent damage to the Ge surface.

One set of patterned samples was implanted at 90 keV with a dose of 5×10^{14} Ge^+/cm^2, which produced an amorphous layer 75 nm deep with a pinned α-*c* interface under the mask edge, as seen in the cross-sectional transmission electron microscopy (XTEM) image in Fig. 2a. The α-*c* interface in this case contains concave curvature.

Another set of samples was implanted at 300 keV with a dose of 5×10^{14} Ge^+/cm^2, which produced an amorphous layer 160 nm under the mask and 235 nm in the exposed areas as seen in the XTEM image in Fig. 4a. In this case, the α-*c* interface is not in contact with the surface and is therefore not subjected to any surface pinning. The α-*c* interface in this case contains both concave and convex curvature.

The samples were annealed in a tube furnace at 330°C in N_2 atmosphere for times of 44–335 min. Anneal times were chosen to see different points during the regrowth process when the regrowth evolution showed important changes. A set of the samples with interfacial pinning had the Si_3N_4 removed prior to annealing via a 5 minute etch in hydrofluoric acid, as seen in Fig. 3a. This was done to observe the effect of patterned Si_3N_4 on the α-*c* interface evolution. It was determined from previous work that the presence of the Si_3N_4 only affected the regrowth of pinned α-*c* interfaces for Si substrates.[23] An FEI DB235 focused ion beam (FIB) was used to prepare XTEM samples and a JEOL 2010F was used to image the 2D SPEG process. The

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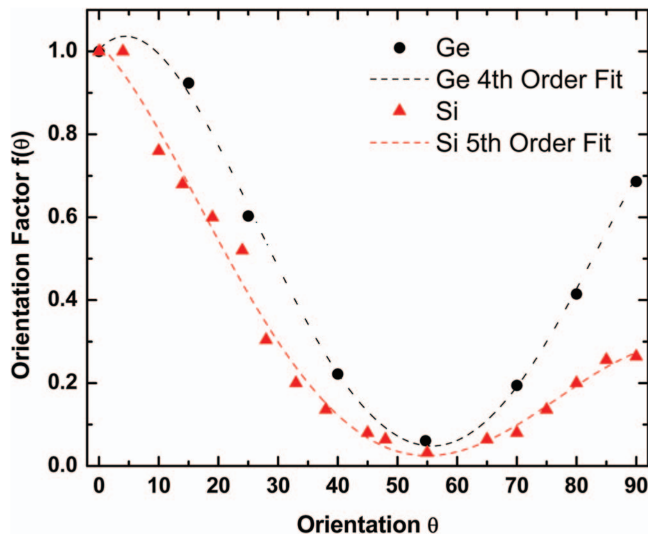

Figure 1. The Ge and Si orientation dependence on SPEG velocities normalized to the [001] direction (0°). A 4th order fit was given to the Ge data,[16] while a 5th order fit was given to the Si data.[23] The [111] and [011] directions exist at 54.7° and 90°, respectively.

2D SPEG process was modeled using level set techniques and implemented in FLOOPS.[24] Level set simulations were used to track the evolution of the propagating interface, where the interface of interest is the α-*c* interface.[25]

Results and Discussion

Fig. 1 shows the normalized SPEG velocities as a function of orientation for Ge in addition to normalized Si values from the literature. The data has been normalized to the [001] direction, which was measured to be 1 nm/min for Ge at 330°C using XTEM. The orientation angle is measured from the [001] direction so that 90° corresponds to the [011] direction. Given the dataset, the fourth order is the least order polynomial that yields a reasonable fit for the Ge data, while a fifth order fit was previously employed for Si.[23] The polynomial for substrate orientation used in this work is given by:

$$f(\theta) = (A_1 \cdot \theta^4) + (A_2 \cdot \theta^3) + (A_3 \cdot \theta^2) + (A_4 \cdot \theta) + A_5 \qquad [3]$$

where $A_1 = -1.47 \times 10^{-7}$, $A_2 = 3.22 \times 10^{-5}$, $A_3 = -1.92 \times 10^{-3}$, $A_4 = 1.51 \times 10^{2}$, $A_5 = 1.01$, and θ is the angle in degrees. $f(\theta)$ is valid between 0 and 90 degrees, which was sufficient for modeling the 2D SPEG from the [001] to [110] directions. Since $f(\theta)$ is unitless, the units of $A_1 - A_5$ are degrees^{-1}. Also, since the orientation dependence is independent of temperature,[26] the regrowth shapes simulated in this experiment would also be independent of temperature.

For the FLOOPS simulations of the patterned Ge structures, Eq. 2 was modified to be linearly dependent on interfacial curvature via[23,27]

$$\upsilon(\theta) = \upsilon_{[001]} f(\theta)(1 + A\kappa) \qquad [4]$$

where A is the curvature factor with units of length and $\kappa = 1/r$ where r is the radius of curvature at the mask edge ($r \sim 80$ nm). For the pinned interface nitride capped samples, $A = 8 \times 10^{-8}$ cm was used, while $A = 3 \times 10^{-7}$ cm was used for the etched samples with a pinned interface. The unpinned interface samples were simulated with a curvature factor of $A = 1 \times 10^{-6}$ cm. Eq. 4 was used for level set simulations of the 2D SPEG process at 330°C for the samples shown in Fig. 2–4.

Fig. 2 shows XTEM images of the annealing sequence at 330°C for pinned interface structures with nitride present during the anneal. After 44 minutes, the α-c interface becomes a right angle (Fig. 2b) and after 135 minutes, mask-edge defects form (Fig. 2c). The mask edge defects remain stable after complete crystallization at 335 minutes (not shown). Similar mask edge defects were observed in Si and were determined to be dislocations aligned along [011]-type directions.[28]

Fig. 3 shows XTEM images of the annealing sequence at 330°C for pinned interface structure with the nitride etched prior to the anneal. After 44 minutes, the α-c interface becomes obtuse (Fig. 3b) and eventually crystallizes up to the surface defect free (Fig. 3d). This result indicates that the presence of the nitride causes a change in the α-c interface shape, resulting in mask edge defect formation. Wafer curvature measurements (not presented) revealed that the nitride contained 55 MPa of tensile stress after deposition, which increased to tensile stresses as high as 80 MPa at 330°C. The increase in film stress was likely due to densification of the film, but nevertheless, this suggests that the film would have imparted a compressive stress on the substrate under the mask during the anneal. Due to the low amorphization threshold for Ge,[29] the lateral straggle of the ions caused the α-c interface and subsequent defects to stretch under the mask. This is somewhat different from defect formation in Si substrates, where the defects reside at the mask edge and not under the mask.[17–19] The formation of compressive stress under the mask edge facilitates the formation of mask edge defects by forming an acute angle in the α-c interface.[20,28] Interestingly, the removal of the nitride film relieved enough stress to eliminate mask edge defect formation in the patterned Ge.

While mask edge defects have been known to cause device leakage,[30] recent work on Si substrates has shown that mask edge defects can actually be beneficial if positioned correctly along the edges of the channel.[21,22,31] Due to the vacancy-type nature of the mask edge defects,[22] the regions surrounding the defect are put in a state of tension. This technique is referred to as stress memorization technology (SMT), in that once the mask is removed, the stress from the defect remains in the substrate. Although no TEM investigation was performed to determine the nature of the Ge mask edge defects, it is probable that they are intrinsic, as they are in Si. This would imply that the creation of mask edge defects would be beneficial for nMOS devices for Ge.

Morarka et al. have suggested that the role of the applied stress on Si SPEG evolution may be accounted for by simply changing the curvature factor.[13] They found that simulations with larger curvature factors matched reasonably well with experiments under tensile stress, and simulations with smaller curvature factors matched reasonably well with experiments under compressive stress. This work has shown that unstressed (stressed) Ge SPEG can be simulated with a curvature factor of $A = 3 \times 10^{-7}$ cm ($A = 8 \times 10^{-8}$ cm), which further supports that the nitride caused a compressive stress in the substrate.

Fig. 4 shows XTEM images of patterned Ge SPEG with an unpinned α-c interface. Unlike the structures with concave interfaces ($\kappa < 0$) shown in Fig. 2-3, the as implanted structure shown in Fig. 4a produced an α-c interface with both concave ($\kappa < 0$) and convex ($\kappa > 0$) α-c interfaces. A negative κ value results in smaller SPEG velocities for concave interfaces according to Eq. 4. In fact, this is exactly what is observed experimentally since the interface curvature decreases over time. This implies that interfaces with positive κ grow faster than interfaces with negative κ. Throughout the annealing sequence, the FLOOPS simulations matched well with the XTEM images. This shows that Eq. 4 can be used to simulate both concave and convex interfaces for Ge.

Fig. 4d shows a near-completely recrystallized structure free of mask edge defects. This could be due to the fact that the initial α-c interface in the unpinned case had less curvature than the pinned case, suggesting that the formation of mask edge defects is also highly dependent on the initial interfacial curvature. This is also why a different curvature factor needed to be used. The defect-free nature of this sample could also be due to the absence of stress near the initial α-c interface. Simulations have shown that the stress from the nitride is concentrated within the first 100 nm of the surface,[28] which could explain why the deep implant in this case recrystallized free of defects.

It is interesting to note that analogous structures in Si formed mask edge defects much more readily.[12,18,19,23,28,32] This stems from a different SPEG dependence on substrate orientation, notably the

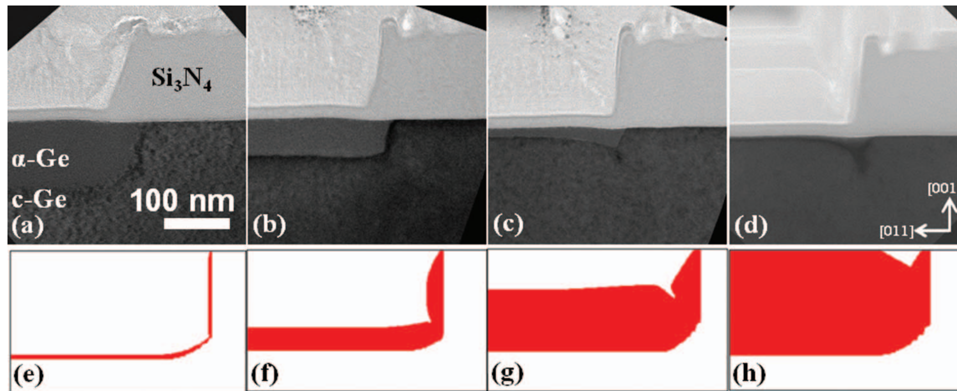

Figure 2. Cross sectional TEM images of nitride stressed patterned Ge implanted with 90 keV 5 × 10^{14} Ge^+/cm^2 and annealed at 330°C for (a) 0, (b) 44, (c) 135, and (d) 235 minutes. The corresponding FLOOPS simulations are shown below in (e) through (h) using a curvature factor of $A = 8 \times 10^{-8}$ cm. A mask edge defect is produced in the stressed case.

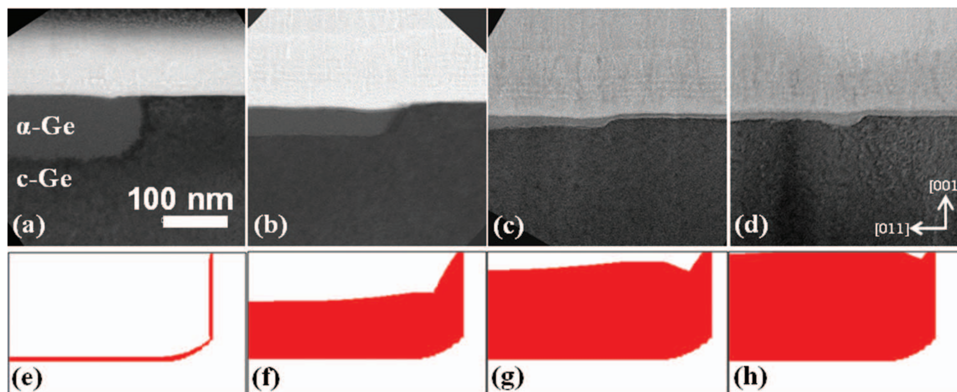

Figure 3. Cross sectional TEM images of unstressed patterned Ge implanted with 90 keV 5 × 10^{14} Ge^+/cm^2 and annealed at 330°C for (a) 0, (b) 44, (c) 135, and (d) 235 minutes. The corresponding FLOOPS simulations are shown below in (e) through (h) using a curvature factor of $A = 3 \times 10^{-7}$ cm. No mask edge defect is produced in the unstressed case.

higher normalized velocities for Ge compared with Si (as seen in Fig. 1). The more isotropic SPEG orientation dependence for Ge leads to a more uniform and defect free regrowth up to the surface. This can be visualized with the FLOOPS simulations for identical Si and Ge structures shown in Fig. 5. The curvature factor for the simulations was kept constant at 8 × 10^{-8} cm for both structures, so the only difference was the substrate orientation factor for Si and Ge and the simulation anneal temperature (330°C and 500°C for Ge and Si, respectively). The orientation factor used for Si in this comparison has been previously presented by Morarka and is graphed in Fig. 1.[23] It is evident from the simulations that α/c interface in Ge is less pinched than its Si counterpart. This means that Ge would be less prone to mask edge defect formation. While this may be inconvenient for utilizing stress memorization technology in nMOS Ge devices, it may be advantageous for the use of Ge in pMOS devices since mask edge defects would be undesirable in this case. From this comparison, it is clear that the orientation factor plays an important role in mask edge defect formation. Since Ge has a more isotropic orientation

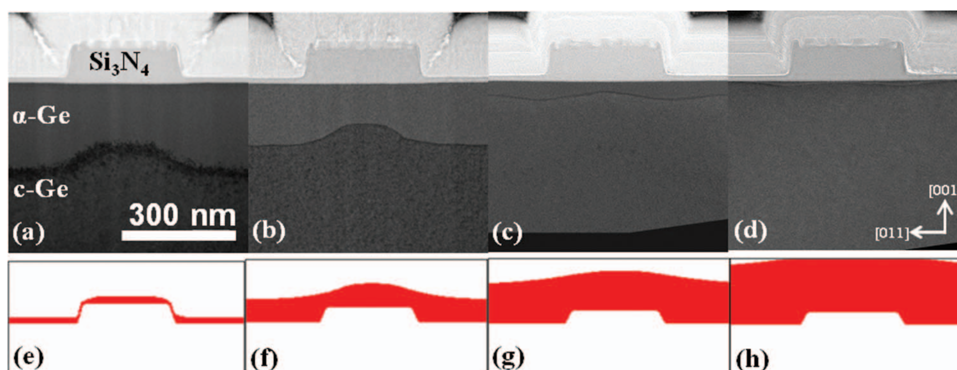

Figure 4. Cross sectional TEM images of patterned Ge implanted with 300 keV 5 × 10^{14} Ge^+/cm^2 and annealed at 330°C for (a) 0, (b) 44, (c) 235, and (d) 335 minutes. The corresponding FLOOPS simulations are shown below in (e) through (h) using a curvature factor of $A = 1 \times 10^{-6}$ cm. No mask edge defect is produced in the unpinned case.

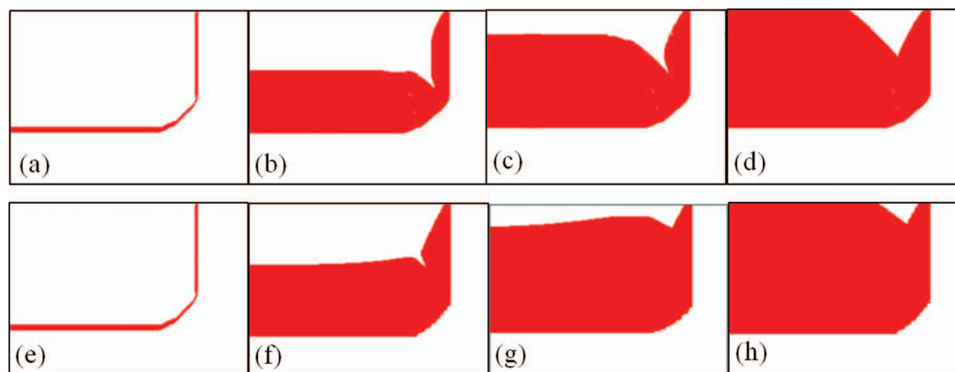

Figure 5. FLOOPS simulations for pinned interface structures for Si at 500°C (a)–(d) and Ge at 330°C (e)–(h). The curvature factor was kept constant for both structures at 8×10^{-8} cm as well as the α/c initial interface.

dependence on SPEG, the structure recrystallizes with less mask edge defects.

Conclusions

The 2D SPEG process for Ge was studied using TEM and modeled using level set techniques. Stress from a nitride cap was found to influence the α-c interface shape upon SPEG. The unstressed patterned Ge SPEG was virtually free of mask edge defects, while the stressed patterned Ge formed a mask edge defect upon SPEG. In addition, α-c interfaces with lower curvatures were found to recrystallize defect free as well. The ability to control defect formation through stress and α-c interface curvature shows promise for use of Ge in device structures. FLOOPS simulations were accurate in predicting the evolution of the α-c interface and the curvature factor was modified to account for the stress of the nitride and the initial curvature of the α-c interface. Ge FLOOPS simulations were compared with Si, which revealed that multidirectional SPEG is less defective for Ge.

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References

1. B. R. Yates, B. L. Darby, N. G. Rudawski, K. S. Jones, D. H. Petersen, O. Hansen, R. Lin, P. F. Nielsen, and A. Kontos, *Materials Letters*, **65**, 3540 (2011).
2. A. Satta, E. Simoen, T. Clarysse, T. Janssens, A. Benedetti, B. De Jaeger, M. Meuris, and W. Vandervorst, *Appl. Phys. Lett.*, **87**, 172109 (2005).
3. Y.-L. Chao, S. Prussin, J. C. S. Woo, and R. Scholz, *Appl. Phys. Lett.*, **87**, 142102 (2005).
4. B. L. Darby, B. R. Yates, N. G. Rudawski, K. S. Jones, and A. Kontos, *Nucl. Instrum. Methods Phys. Res. B*, **269**, 20 (2011).
5. B. C. Johnson, P. Gortmaker, and J. C. McCallum, *Phys. Rev. B*, **77**, 12 (2008).
6. L. Csepregi, R. P. Kullen, J. W. Mayer, and T. W. Sigmon, *Solid State Commun.*, **21**, 1019 (1977).
7. G. Q. Lu, E. Nygren, and M. J. Aziz, *J. Appl. Phys.*, **70**, 5323 (1991).
8. G. Q. Lu, E. Nygren, M. J. Aziz, D. Turnbull, and C. W. White, *Appl. Phys. Lett.*, **56**, 137 (1990).
9. G. L. Olson and J. A. Roth, *Materials Science Reports*, **3**, 1 (1988).
10. J. A. Roth, G. L. Olson, D. C. Jacobson, and J. M. Poate, *Appl. Phys. Lett.*, **57**, 1340 (1990).
11. J. M. Poate, S. Coffa, D. C. Jacobson, A. Polman, J. A. Roth, G. L. Olson, S. Roorda, W. Sinke, J. S. Custer, M. O. Thompson, F. Spaepen, and E. Donovan, *Nucl. Instrum. Methods Phys. Res. B*, **55**, 533 (1991).
12. S. Morarka, N. G. Rudawski, M. E. Law, K. S. Jones, and R. G. Elliman, *J. Vac. Sci. Technol. B*, **28**, C1F1 (2010).
13. S. Morarka, S. Jin, N. G. Rudawski, K. S. Jones, M. E. Law, and R. G. Elliman, *J. Vac. Sci. Technol. B*, **29**, 041210 (2011).
14. B. C. Johnson and J. C. McCallum, *Phys. Rev. B*, **76** (2007).
15. I. Suni, G. Goltz, M. A. Nicolet, and S. S. Lau, *Thin Solid Films*, **93**, 171 (1982).
16. B. L. Darby, B. R. Yates, I. Martin-Bragado, J. L. Gomez-Selles, R. G. Elliman, and K. S. Jones, *J. Appl. Phys.*, **113**, 033505 (2013).
17. H. Cerva and K.-H. Kusters, *J. Appl. Phys.*, **66**, 4723 (1989).
18. K. L. Saenger, K. E. Fogel, J. A. Ott, D. K. Sadana, and H. Yin, *J. Appl. Phys.*, **101**, 104908 (2007).
19. K. L. Saenger, K. E. Fogel, J. A. Ott, C. Y. Sung, D. K. Sadana, and H. Yin, *J. Appl. Phys.*, **101**, 084912 (2007).
20. C. R. Olson, E. Kuryliw, B. E. Jones, and K. S. Jones, *J. Vac. Sci. Technol. B*, **24**, 446 (2006).
21. E. W. Cory, M. C. Stephen, D. Hemant, G. Oleg, and Y. L. Mark, 34 (2011).
22. L. Kwan-Yong, L. Hyunjung, R. Choongryul, S. Kang-Ill, K. Uihui, K. Seokhoon, C. Jongwan, O. Kyungseok, J. Hee-Kyung, S. Chulgi, K. Tae-Ouk, C. Jinyeong, L. Seunghun, S. Yangsoo, Y. Hong Sik, P. Junghyun, L. Kwanheum, K. Wookje, L. Eunha, S. Sang-Pil, K. Chung Geun, K. Sang Bom, C. Siyoung, and C. Chilhee, in *Electron Devices Meeting (IEDM), 2010 IEEE International*, p. 10.1.1 (2010).
23. S. Morarka, N. G. Rudawski, M. E. Law, K. S. Jones, and R. G. Elliman, *J. Appl. Phys.*, **105**, 053701 (2009).
24. M. E. Law and S. M. Cea, *Computational Materials Science*, **12**, 289 (1998).
25. J. A. Sethian, *J. Comput. Phys.*, **169**, 503 (2001).
26. L. Csepregi, E. F. Kennedy, J. W. Mayer, and T. W. Sigmon, *J. Appl. Phys.*, **49**, 3906 (1978).
27. B. Drosd and J. Washburn, *J. Appl. Phys.*, **51**, 4106 (1980).
28. N. G. Rudawski, K. S. Jones, S. Morarka, M. E. Law, and R. G. Elliman, *J. Appl. Phys.*, **105**, 081101 (2009).
29. S. Koffel, P. Scheiblin, A. Claverie, and G. Benassayag, *J. Appl. Phys.*, **105**, 013528 (2009).
30. S. Onishi, A. Ayukawa, K. Tanaka, and K. Sakiyama, *J. Electrochem. Soc.*, **138**, 1439 (1991).
31. M. Takei, H. Hashiguchi, T. Yamaguchi, D. Kosemura, K. Nagata, and A. Ogura, *Technical report of IEICE. SDM*, **111**, 43 (2011).
32. K. L. Saenger, J. P. d. Souza, K. E. Fogel, J. A. Ott, C. Y. Sung, D. K. Sadana, and H. Yin, *J. Appl. Phys.*, **101**, 024908 (2007).