# On Implant-Based Multiple Gate Oxide Schemes for System-on-Chip Integration

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***Abstract*—Integrating the entire system on a chip (SOC) is one of the main challenges for many researchers all over the world. One of the major breakthroughs toward achieving this goal has been the ability to manufacture multiple gate oxides for different requirements on the same chip. The most attractive of the techniques currently in the literature is the implantation of nitrogen in silicon, which can be used to achieve the goal of multiple gate oxide thickness. The rate of oxidation depends on the amount of nitrogen incorporated at the silicon/silicon oxide interface. By modulating the amount of nitrogen incorporated at the interface, the rate of oxidation and hence the oxide thickness can be moderated. This paper reviews the diffusion, oxidation, and device issues pertaining to the use of nitrogen implants in silicon and also compares it to other implant-based techniques related to the achievement of multiple oxide thickness across the chip for SOC integration.**

***Index Terms*—Fluorine, gate oxides, multiple gate oxides, nitrogen implantation, oxides, system-on-chip (SOC) integration technology platform.**

## I. Introduction

MOORE'S law has driven much of the semiconductor PC revolution for the past twenty years. However, in today's integrated wireless communications environment, system-on-chip (SOC) solutions are becoming increasingly important for cost reduction [1], [2]. For the purposes of this paper, SOC solutions refer to integrating different processes onto the same chip. For example, this could mean the integration of digital, analog, power management, I/O, passives, radio, FLASH, RAM and driver circuitry modules that have different power supply voltages (ranging between about 1.2 to 10 V) on the same die in the same chip. The successful implementation of SOC will require innovation in both circuit design and fabrication technology. However, from a process technology standpoint, it can be seen that in order to provide process design flexibility each of the modules can require different gate oxide thicknesses. Such schemes have been proposed for the 90-nm node and beyond [3].

SOC integrates digital and analog circuits on the same chip. This is a challenging task for technology platform development since the requirements for digital and analog devices are different and sometimes conflicting. [2]

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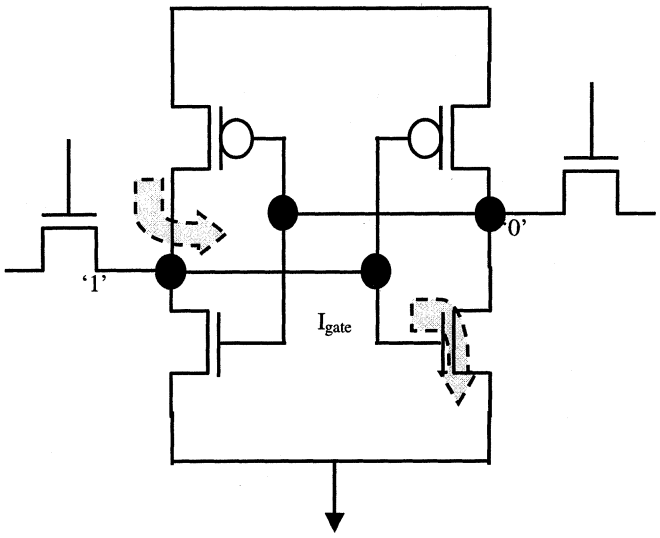


Fig. 1. This figure illustrates how high gate currents can increase the standby power of high-density embedded SRAM cells. From [4].

### A. Logic Technology Concerns

While the internal circuitry of a microprocessor runs at reduced voltage levels of about 1.5 V or less, the I/O modules of a chip that connect to the pads run at higher voltages (and therefore need thicker oxides) to match printed circuit board (PCB) requirements.

In an embedded SRAM cell, high gate currents increase the standby power, thereby ruining battery life [4]. This is illustrated in Fig. 1, reproduced from [4, Fig. 1]. There have been reports in the literature of triple-gate digital technologies where a thin gate oxide is grown for the core logic and pass transistors, a slightly thicker oxide for the low-power CMOS areas, and an even thicker gate oxide for the I/O modules [5].

### B. Analog Technology Concerns

The requirements for analog technologies are quite different from their digital counterparts. Digital technology has been successful with continuous scaling of supply voltages (and therefore gate oxides) of transistors to improve power consumption requirements. In very simple terms, the power dissipated follows the relation $CV_{dd}{}^2f$. Therefore, for a given clock frequency, the lower the supply voltage $V_{dd}$, the lower the power dissipated. However, in analog technologies, the prime concern is minimal signal distortion with maximum power delivered to the external load—for example, a loudspeaker. This in turn means that the signal swing has to be as close to

the $V_{dd}$ rails as possible. The more the signal swing, the higher the power delivered to the external load. As the power supply voltages and gate oxide thicknesses are reduced with transistor scaling, the output-signal swing for a given SNR or total harmonic distortion also becomes less. This in turn reduces the power that can be delivered to the external load. It can also be shown that, in analog circuits, decreasing the supply voltage $V_{dd}$ in fact increases power dissipation [6].

Another example of how analog requirements are different from their digital cousins is the case of the cascode amplifier that probably is one of the most common analog circuit configurations. In a cascode amplifier, each successive $V_T$ drop reduces the amount of "headroom" or the voltage signal space available for the other transistors in the circuit. If we consider line driver circuits, then the need for higher voltages and hence thicker gate oxides is self-explanatory.

The above examples help illustrate that integration of gate oxides of multiple thickness is of utmost importance in an SOC technology platform that envisions integrating digital, analog, and/or power circuitry on the same chip in a low-cost CMOS process.

In order to achieve the cost reduction benefit from SOC, the ability to grow multiple gate oxide thicknesses has to come at no/very minimal increase in mask levels. A few different techniques have been proposed. One of the techniques possible is to use a repeat mask and etch process to grow the required gate oxide thickness. These processes typically use oxynitridation methods by flowing $N_2O$, NO, or $NO_2$ gases. There are excellent reviews on the subject of oxynitridation from gas phase chemistries [7]–[12]. The main drawback with this process is that many thermal steps are involved, since each time the gate oxide of a particular thickness has to be grown. This in turn increases the number of process steps involved which defeats the purpose of dramatic cost reduction that SOC was intended to produce. Further, this process could also lead to an increase in the defect density due to repeated resist removal and etching. While currently some members of the semiconductor community may use a scheme similar to the one described above due to its maturity, this scheme may become infeasible as integration complexity increases. This issue looks farther ahead on the challenges of integrating the entire system on a chip, and hence other techniques that are technologically attractive have to be investigated.

An alternate scheme, which is the central focus of this paper, is based on the implantation of nitrogen into silicon. The final oxide thickness grown depends on the dose of the nitrogen implanted into silicon [13]–[26]. Therefore, by controlling the dose of the nitrogen implant, the thickness of the oxide across the silicon wafer can be varied. There are other nitrogen implant-based techniques into polysilicon material and metal gates that can also be used to achieve different threshold voltages [27]–[31]. This scheme (nitrogen implantation) does not lead to any increase in mask levels above that of the process mentioned above. The added advantage of the nitrogen implant process is that it does not require any additional thermal steps, as once the required doses of nitrogen are implanted, a single thermal step should be enough to achieve the different gate oxide thickness across the wafer, thereby making it a modular process. Although the application of nitrogen implants to ultralarge-scale integration (ULSI) to produce multi-$V_T$ devices for SOC applications is the main focus of this paper, it may be instructive to note that the application of nitrogen implants in electronic device applications extends beyond multi-$V_T$ devices. For example, nitrogen implants into silicon have been used to control the transient diffusion of boron and arsenic in silicon [32]–[36] and have also been implanted into SOI substrates [37]. Nitrogen implants also suppress the penetration of boron from the polysilicon into the gate and the underlying substrate [29], [38]–[41]. Nitrogen-implanted buried channel silicon carbide devices have shown improved channel mobility [42], [43]. There have also been reports in the literature that the implantation of fluorine can also lead to variation in the gate oxide thickness [44]–[46]. However, fluorine has the opposite effect on oxidation to that of nitrogen in silicon. That is, fluorine implantation enhances the oxidation rate. Therefore, one can think of a scheme where the thinnest oxide in the device receives no fluorine implant and the thickness of the other oxides depend on the dose of the fluorine implant.

The moderation of oxidation subsequent to nitrogen implantation is because of the diffusion of nitrogen subsequent to its implantation. Oxynitridation in general reduces the gate tunneling current while also reducing the equivalent oxide thickness [47], [48]. Equivalent oxide thickness is defined as the thickness of a pure $SiO_2$ layer having the same capacitance as that of the oxynitride. The work in [47] shows that there is an optimization of the nitrogen content at the interface required for integrating digital and analog CMOS. While the above references pertain to NO and remote plasma nitridation (RPN)-based oxide growth methods, one would expect similar requirements for nitrogen implant-based methods also. This is because, upon implantation and anneal, the nitrogen reaches the interface. Therefore, understanding the diffusion behavior of implanted nitrogen in silicon is relevant. Section II of this paper will discuss the physics of the diffusion of nitrogen subsequent to implantation. As explained earlier, the main motivation of implanting nitrogen in silicon is to vary the gate oxide growth. Hence, Section III will couple the understanding of the diffusion behavior of nitrogen implants in silicon with the physics of oxide growth subsequent to nitrogen implantation. Section IV will discuss the device issues pertaining to nitrogen implants in silicon devices. Section V will discuss alternate implant-based techniques to achieve multi-$V_T$ devices. Section VI will discuss the challenges yet to be overcome in nitrogen-implanted silicon. Finally, Section VII will summarize this paper.

## II. Diffusion of Implanted Nitrogen in Silicon

It may be instructive to note that interest in nitrogen implanted into silicon has been around since the early 1960s. One of the first works on the study of nitrogen implants into silicon was performed by Ferber [49] in 1963. In fact, in this study, the authors tried to determine the electrical activation of nitrogen implanted into silicon. Nitrogen was implanted into silicon and then an inversion of the conductivity type with high resistivity was observed. Increasing the anneal temperature up to 500 °C did not change the conductivity discernibly. There has been

some work done in the 1960s and early 1970s on the electrical activation of implanted nitrogen in silicon. [50]–[52]. However, all these studies report shallow donor levels between 0.017 and 0.142 eV. We know now from deep level transient spectroscopy (DLTS) studies that nitrogen occupies deep level states in the bandgap, although there is a spread in the literature on the exact location of the deep levels [53], [54].

Early reports in the literature suggest an Arrhenius relationship to the diffusivity of implanted nitrogen in silicon. [51], [55]. Those studies depended on indirect profiling methods to extract dopant diffusivities. For example, Clark *et al*. [51] studied the effect of nitrogen implanted into p-type silicon and annealed at different temperatures of up to 1200 °C. Based on the junction formation, they obtained an effective diffusivity for implanted nitrogen in silicon and reported it in terms of an Arrhenius relationship. However, we know now that the electrical activation of implanted nitrogen in silicon is very low and hence using junction determination methods to extract diffusivity is a very suspect technique—certainly for impurities like nitrogen with low electrical activation levels. More recently, Hockett [56] reported diffusion profiles of nitrogen implanted into silicon at $1 \times 10^{14}$ $N^+/cm^2$, 200 keV (projected range $\sim 0.25$ $\mu$m) into float zone substrates. He observed a shift of the peak of the profile deeper into the bulk with time and attributed this to implant damage-mediated diffusion. However, this goes contrary to current observations of implanted nitrogen diffusion in silicon, as explained later in this section. In fact, as will be obvious later in this section, nitrogen diffusion does not correspond to an Arrhenius relationship.

More recently, there has been reports on the diffusion of nitrogen into silicon in the presence of other species like boron [32], [36]. These studies looked at the effect of the diffusion of boron subsequent to nitrogen implantation. The work in [36] also showed the microstructure evolution subsequent to nitrogen implantation. While the focus of these studies was to implant nitrogen to mediate the diffusion of boron, they did provide some useful hints on the diffusion of implanted nitrogen also. These studies showed that the diffusion of boron was sometimes suppressed in the presence of nitrogen implants. This meant that the nitrogen was modifying the defect populations in some manner. Given that the diffusion of boron is mediated through interstitials [57], these studies provide a hint that the implantation of nitrogen into the silicon substrate modifies the populations of interstitials in silicon. Therefore, there existed a need for a study where just nitrogen was implanted into the silicon substrate and then annealed at various times and temperatures. Such a study was performed by Adam *et al*. [58] and by Lysaght *et al*. [59]. Both of these studies showed that nitrogen diffused toward the surface upon annealing. In [60], nitrogen was implanted at $5 \times 10^{13}$ $N_2^+$, 40 keV, and 200 keV and annealed at 650 °C and 750 °C for various times. Figs. 2–4 show the profiles. Based on these studies, it can be concluded that the diffusion behavior of nitrogen implanted into silicon is anomalous. Figs. 2–4 show four main characteristics.

1) The motion of the profile is anomalous and cannot be explained by conventional Fick's law [61]. While the peak of the profiles decrease with increasing time, there is no spreading of the profile in the bulk with time as one would expect.

Fig. 2. Diffusion of $5 \times 10^{13}$ $N_2^+$, 40 keV implant at 650 °C. From [58].

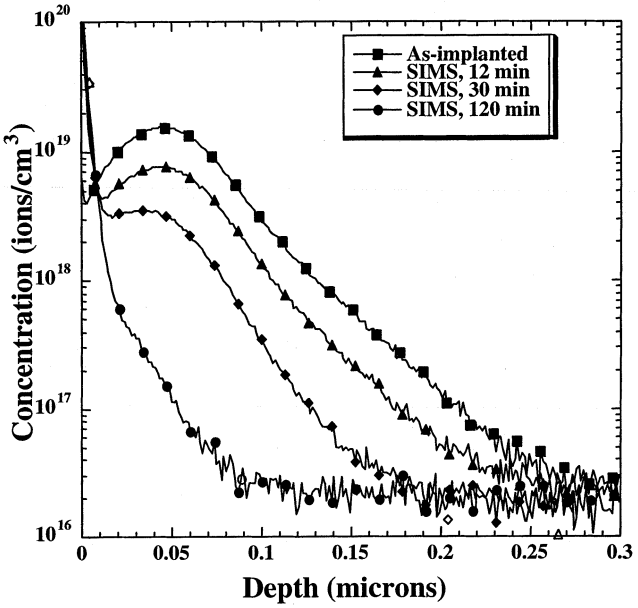


Fig. 3. Diffusion of $5 \times 10^{13}$ $N_2^+$, 40 keV implant at 750 °C. From [58].

2) The motion of the total nitrogen profile toward the surface is much more rapid at 750 °C than at 650 °C. This indicates that there is a high-temperature-dependent barrier to diffusion.
3) The peak of the profiles also shifts toward the surface with time. This indicates that the nitrogen is being released deeper rather than closer toward the surface.
4) The fact the motion of the nitrogen profile toward the surface is similar at 40 keV and 200 keV shows that the motion of the nitrogen profile toward the surface cannot be attributed to electrostatic attraction at the surface.

Further, transmission electron microscopy (TEM) studies on these samples showed that no {311} defects evolved subsequent to nitrogen implantation and annealing. This was also

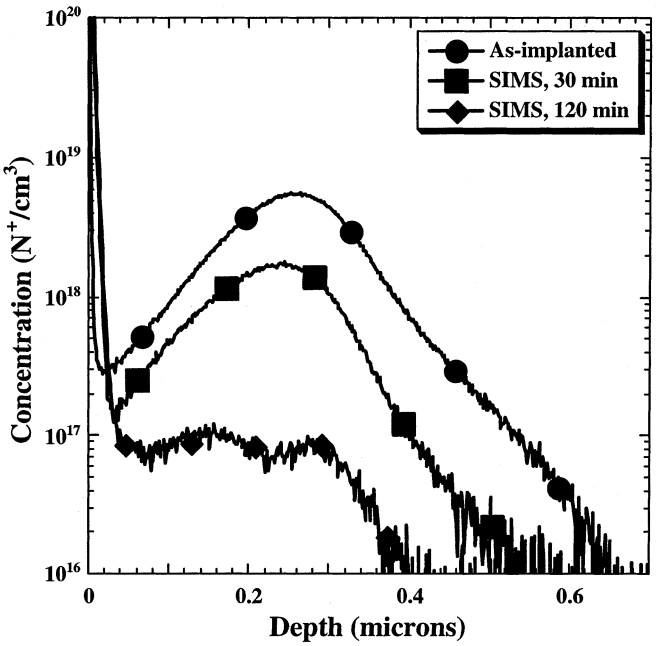


Fig. 4. Diffusion of $5 \times 10^{13}$ $N_2^+$, 200 keV implant at 750 °C From [60].

quite interesting to the processing community because silicon implanted at comparable doses and energies showed many {311} defects [62]. However, with nitrogen, such was not the case. While the anomalous nature of the diffusion behavior of implanted nitrogen in silicon was now established, the physical mechanism by which this occurs was still not explained. A model developed by Adam *et al.* [63]–[65] comprehensively explained the diffusion behavior of implanted nitrogen in silicon. The damage profiles of the implant were obtained from a scaled UT-MARLOWE simulation [66]. The model used a set of reaction rates involving nitrogen vacancy and nitrogen interstitial complexes. The energetics of these complexes was provided by *ab initio* calculations and experimental observation [67]–[69]. The reactions were diffusion limited at lower temperatures and reaction limited at higher temperatures. The crux of the model was that the reaction rates were controlled such that there existed a gradient of nitrogen interstitials toward the surface. The boundary conditions were such that any nitrogen that reaches the surface accumulates at the $Si/SiO_2$ interface. This is supported by experimental X-ray photoelectron spectroscopy observations [13] and is particularly important in the discussion of nitrogen-mediated oxide growth rates as discussed in detail in Section III. Since nitrogen interstitials are the only nitrogen-related mobile species (this was again shown by *ab initio* calculations) in the set of reactions considered, the entire profile has to shift toward the surface with time. Therefore, we currently have a diffusion model that accurately predicts the diffusion behavior of implanted nitrogen in silicon. The model also explained the absence of {311} defects in nitrogen-implanted samples. This was because the nitrogen reactions were stronger than the {311} reactions for the self-interstitials. Therefore, the dose of the {311}'s and the self-interstitials contained in the {311}'s was at about or lower than the detection limits of the TEM. The agreement between the SIMS and the simulations at various times and temperatures is shown in Figs. 5–7.

It must also be mentioned that there is another school of thought that considers molecular nitrogen as the primary diffusing species in nitrogen implanted silicon. Some of the earlier studies by Pavlov *et al.* [55] suggest $N_2$ formation in silicon. However, since they suggest Arrhenius relationships for the diffusivity of nitrogen implanted into silicon, their conclusions are quite contrary to recent experimental findings on the diffusion of implanted nitrogen in silicon. Itoh and Abe [70] also discuss the formation of $N_2$ molecules in the system based on grown-in nitrogen incorporated during crystal growth. They extract their diffusivity based on the theory that when nitrogen is grown-in into the bulk, they form $N_2$ molecules that escape from the system. They also try correlating the escape of nitrogen from the surface to IR spectra. In their paper, the authors do not mention about the presence of a capping material. It is well known that, in the absence of a capping material, the impurities that reach the surface will diffuse out of the system. Therefore, based on the results of Itoh and Abe, we cannot conclude if the diffusing species is $N_2$ or some species involving a single N. In the presence of a capping oxide, as shown by Liu *et al.* [71], nitrogen implantation into silicon retards the oxide growth rate. This is indicative of the fact that, at least under nitrogen implantation conditions, nitrogen does not escape from the system.

Our thoughts on this issue of molecular nitrogen as the primary diffusing species in silicon is that the current experiments by Liu *et al.* [13], [71] do not support the formation of molecular nitrogen as the dominant nitrogen-related species after implantation. In [13] and [71], the authors report that nitrogen implantation moderates the oxidation rate. If nitrogen were present in its molecular form, then, due to the high binding energy ($\sim$6 eV) of molecular nitrogen, one would expect that molecular nitrogen would leave the system rather than being incorporated in some form either at the $Si/SiO_2$ interface or in the oxide. One could possibly argue that maybe molecular nitrogen is incorporated into the oxide due to the high solid solubility of nitrogen in the oxide. However, from oxynitridation studies, it is well known that diffusing nitrogen from an $N_2$ ambient does not lead to nitrogen incorporation in the oxide [72]. This is because, since molecular nitrogen is very tightly bound, it is extremely difficult to break them up and make them bond with oxygen atoms. It is for this reason that a carrier gas like ammonia ($NH_3$) or $NO_2$ is routinely used for oxynitridation from gas ambients [73].

It must also be mentioned that we did do some simulation trials accounting only for $N_2$ and $N_2$ based reactions and were not able to produce agreeable results with SIMS observations. The energetics of the reactions were obtained from Sawada and Kawakami [74]. The reason the simulations did not show the behavior as observed in SIMS was because, in the case of the simulations involving molecular nitrogen, two nitrogen interstitials formed a nitrogen molecule. Therefore, the self-interstitials were consumed more efficiently leading to fewer self-interstitials remaining in the system at longer times. The remaining self-interstitials are not enough to sustain the continued production of nitrogen interstitials and hence molecular nitrogen.

To summarize this discussion on the diffusion of implanted nitrogen in silicon, the diffusion of nitrogen implanted into silicon has been researched quite extensively and a physics-based diffusion model developed. However, since nitrogen is im-

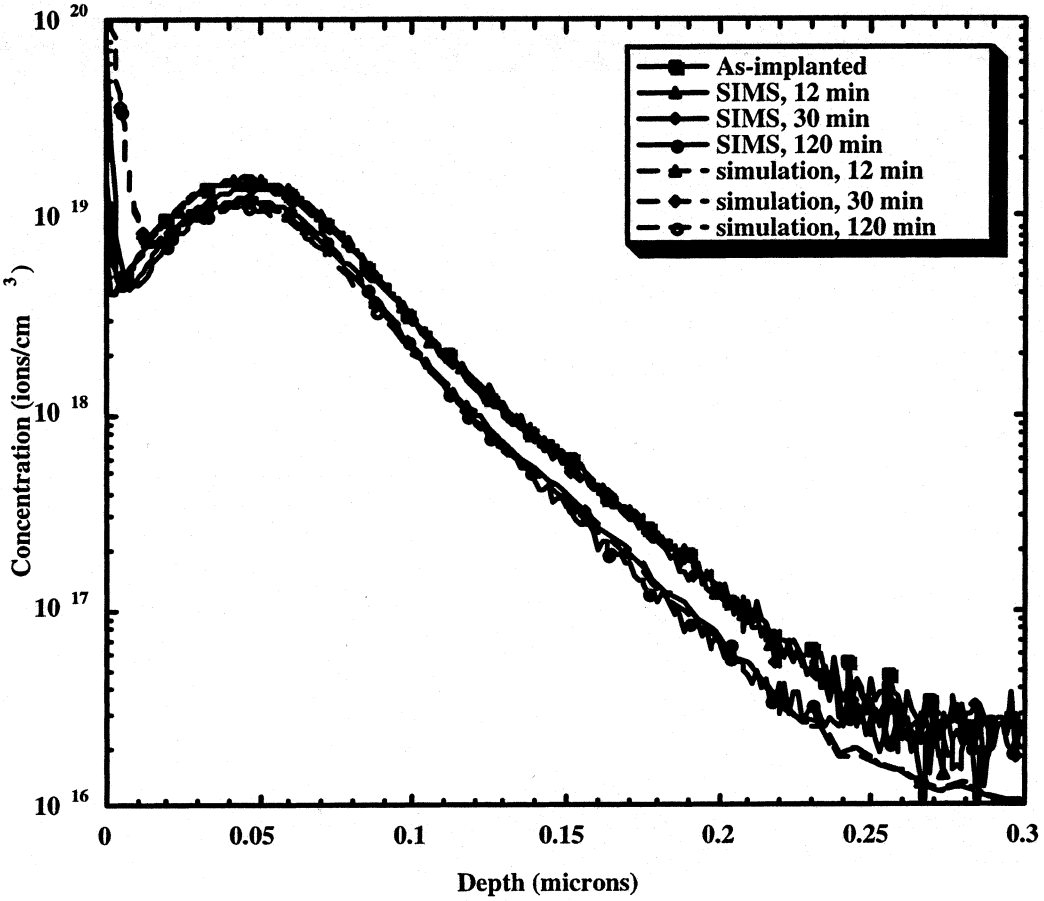


Fig. 5. SIMS versus simulation comparisons at 650 °C for $5 \times 10^{13}$ $N_2^+$, 40 keV. From [65].

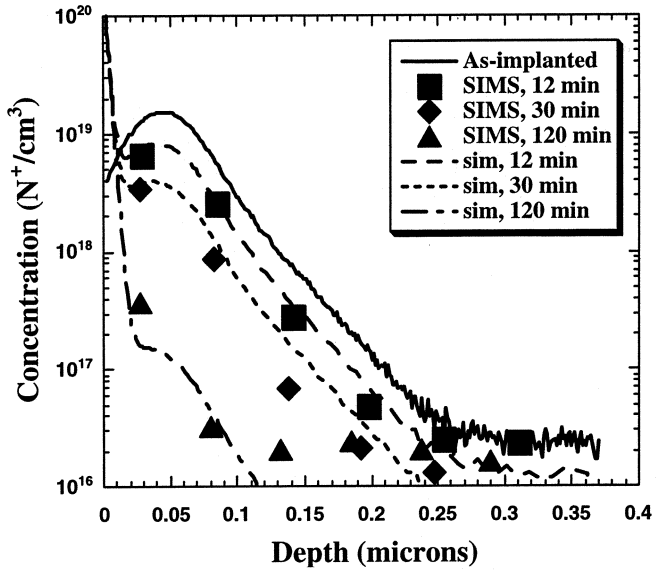


Fig. 6. SIMS versus simulation comparisons at 750 °C for $5 \times 10^{13}$ $N_2^+$, 40 keV. From [65].

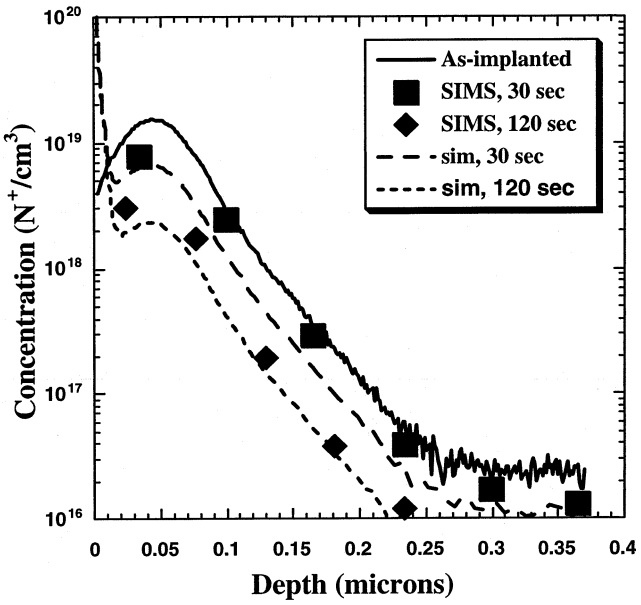


Fig. 7. SIMS Vs simulation comparisons at 850 °C for $5 \times 10^{13}$ $N_2^+$, 40 keV. From [65].

planted into silicon with the main purpose of achieving multiple gate oxides on the same chip, a nitrogen diffusion model by itself is not of much technological value if it cannot be used to predict the oxide growth rates. Therefore, the physics of the moderation of oxide growth rates subsequent to nitrogen implantation will be the focus of the next section.

## III. Oxidation of Nitrogen-Implanted Silicon

There have been reports in the literature that nitrogen implantation into silicon retards gate oxide growth [13]–[26], [75]. This makes nitrogen implantation a particularly attractive tech-

nique for multiple gate oxide technologies because, by varying the dose and energy of the nitrogen implant, the thickness of the gate oxide across the wafer can be varied. Oxidation of silicon can be divided into three categories:

1) fast initial oxidation for very thin oxides ($<\sim$70 Å);
2) linear oxidation rate for thicker oxides ($<\sim$200 Å);
3) parabolic oxidation rate for very thick oxides ($>\sim$200 Å).

Divisions 2) and 3) are more "classic" and will hence be discussed first. Division 1) above will be discussed a little later in this section. Divisions 2) and 3) above correspond to the classic Deal–Grove equation [76]. The mathematical form of their model can be represented by

$$\left[\frac{X^2}{B}\right] + \left[\frac{X}{\left(\frac{B}{A}\right)}\right] = t + \tau. \tag{1}$$

In (1), $X$ represents the oxide thickness and $t$ represents the time. $\tau$ is a parameter that has the units of time and takes into account the initial oxide thickness (native oxide). In (1), $B$ is associated with the quadratic term and is hence called the parabolic rate constant. Similarly, $(B/A)$ is associated with the linear term and is hence called the linear rate constant. When the oxide thickness is small, the linear reaction rate $(B/A)$ term is dominant and, as the thickness increases, the parabolic rate constant term gradually takes over.

In order to understand how the nitrogen retarded gate oxide growth, Adam *et al*. [63], [64] integrated their diffusion model into an oxidation model to predict the gate oxide growth. They based their model on a variation of the Massoud model of rapid oxidation [77], which corresponds to case 1) mentioned above. The Massoud model consists of an Arrhenius relationship for the fast initial oxidation of thin oxides followed by the terms of the classic Deal–Grove equation. This is represented by the equation below:

$$X = X_0 + \int \alpha_0 \exp\left(\frac{-\Delta E}{kT}\right) \exp\left(\frac{-X}{L}\right) dt. \tag{2}$$

In (2), $X_0$ corresponds to the thickness as calculated from the Deal–Grove model characterized by (1) above, $\alpha_0$ and $\Delta E$ represent an Arrhenius relationship that is temperature-dependent and $L$ represents a decay length. $\alpha_0$ has units of $\mathrm{s}^{-1}$. The limits of the integral in (2) are from $t = 0$ to the time under consideration. As can be seen from (2), as the oxide thickness $X$ increases, the effect of the second term in (2) reduces and the Deal–Grove model gradually takes over.

Adam *et al*. [63] moderated the linear growth rate of the Deal–Grove equation as a linear function of the nitrogen that reaches the surface as given by the diffusion model. The ultrafast initial oxidation is moderated as a function of the nitrogen that reaches the surface through a power law. The equations used in their model are given below:

$$\frac{B}{A} \text{ reduction factor: } 1 - \left(\frac{\mathrm{dose}(\mathrm{N_{interface}})}{1 \times 10^{15}}\right) \tag{3}$$

$$\text{Massoud reduction factor: } \left[\frac{b}{\left(b + \left(\frac{\mathrm{dose}(\mathrm{N_{interface}})}{1 \times 10^{15}}\right)\right)}\right]^m. \tag{4}$$

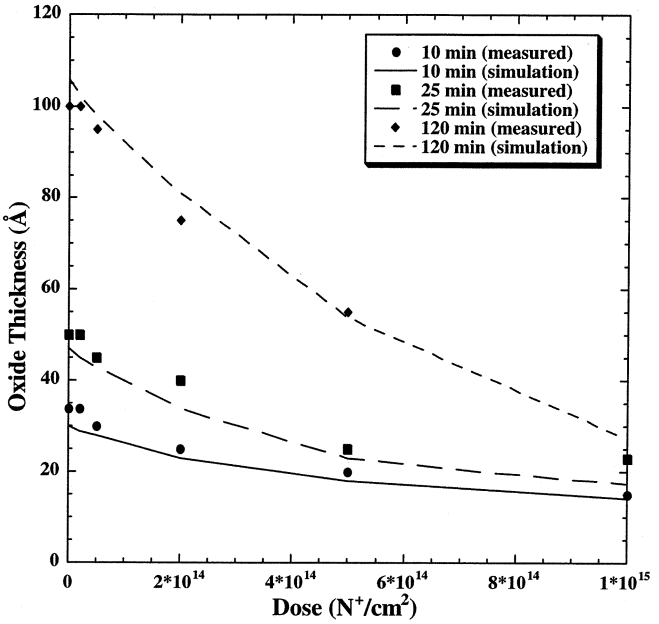


Fig. 8. Comparison of measured and simulated oxide thickness at 800 °C. Data from [13], simulation from [63].

In (3) and (4), $b$ and $m$ are fitting parameters. The factor of $1 \times 10^{15}$ corresponds to the surface site density and $\mathrm{dose}(\mathrm{N_{interface}})$ corresponds to the nitrogen dose incorporated at the interface through the diffusion model described in Section III. From (3) and (4), we can see that as the nitrogen interfacial dose increases, the growth velocity and the surface reaction rate reduce. As described in the diffusion model in Section III, as nitrogen accumulates at the interface, it fills up available lattice sites at the surface. Therefore, the number of available surface sites for the oxidant to attach itself to reduces and hence the oxide thickness decreases. Since the accumulation of nitrogen at the interface is limited to the surface site density $(1 \times 10^{15}/\mathrm{cm}^2)$ in the diffusion model, (3) has a lower limit of zero. Furthermore, (3) scales linearly with $\mathrm{dose}(\mathrm{N_{interface}})$. This adds further strength to the model because, (3) impacts the linear growth regime of the Deal–Grove equation. The best fits were obtained with $b = 0.25$ and $m = 1.8$. As shown in Figs. 8–10, using these two parameters, the authors in [63] and [64] have been able to fit oxide data over a wide range of temperature, from 800 °C to 1050 °C.

Therefore, we now have a reasonable physical understanding of the physics of how nitrogen diffuses in silicon and how it moderates oxide growth. The next issue to consider will be the effect of nitrogen implantation and diffusion on the device characteristics. These issues will be discussed in the section below.

## IV. Device Issues

Liu *et al*. [13] show that the penetration of boron into the silicon substrate from the $\mathrm{p}^+$ polysilicon is retarded in nitrogen-implanted material. This has also been corroborated by other researchers [15], [17], [29], [30], [40], [78], [79]. While the reports in [15] and [78] suggest that this is due to the accumulation of the nitrogen at the oxide interface, Nakayama *et al*. [40] and Chao *et al*. [79] suggest that the suppression of boron penetration into the oxide is due to the reduced diffusivity of boron in

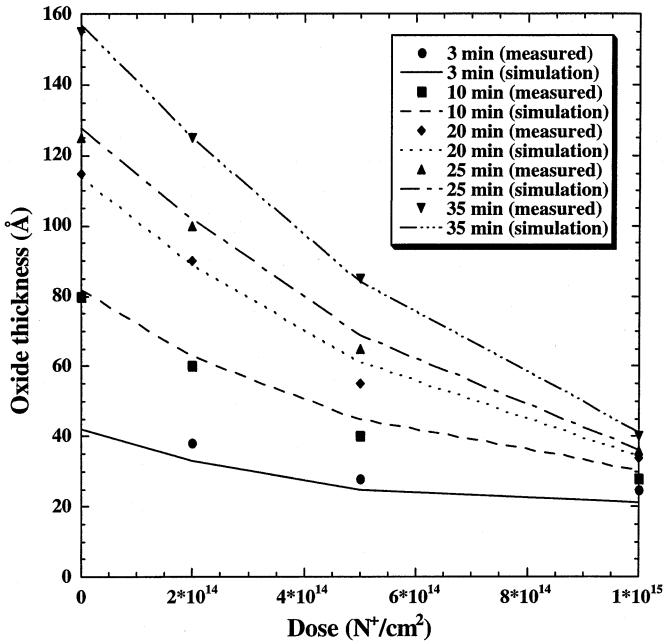


Fig. 9. Comparison of measured and simulated oxide thickness at 900 °C. Some of the data is from [75], the rest of the data from [63], and the simulation is from [63].

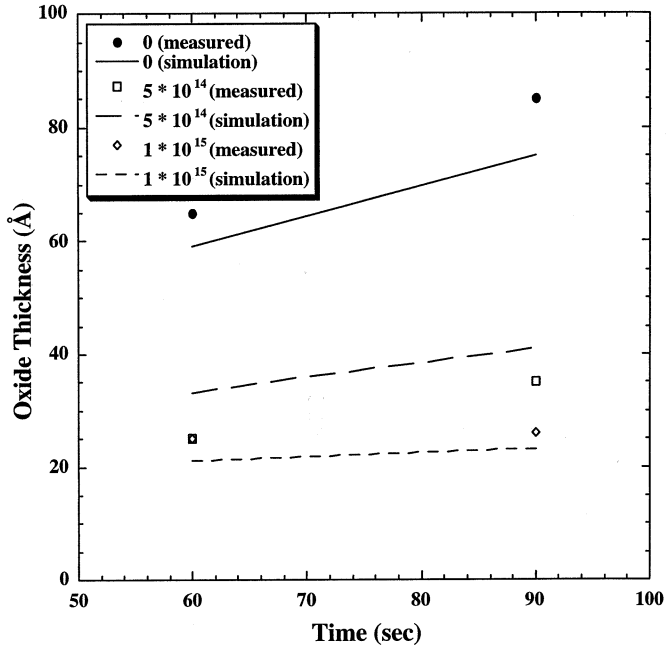


Fig. 10. Comparison of measured and simulated oxide thickness at 1050 °C. Some of the data is from [75], the rest of the data from [63], and the simulation is from [63].

the polysilcion in the presence of a nitrogen implant. Chao *et al.* [79] suggests a possible B-N complex formation in polysilicon. However, this has not yet been confirmed with *ab initio* calculations.

Nam *et al.* [17] also report that the gate current decreases in the case of nitrogen-implanted silicon transistors. The electron wavefunction decay constant within a dielectric is proportional to $\sqrt{m^*\phi_B}$ where $m^*, \phi_{\mathrm{B}}$ are the dielectric effective mass and barrier height, respectively. Nitrided oxides possess a lower tunneling effective mass and barrier height compared to $SiO_2$ giving a reduced decay constant [80]. For an equivalent capacitance, the reduction in decay constant is compensated for by the thicker physical thickness of nitrided films given by the ratio of dielectric constants $\varepsilon_{\mathrm{NO}}/\varepsilon_{\mathrm{OX}}$. This ratio leads to reduced tunnel current for nitrided oxides compared to $SiO_2$ with the same electrical thickness.

In addition to reducing tunnel current, implanted nitrogen has been shown to improve channel hot carrier reliability (stressed with gate and drain biased high). Guarin *et al.* [81], Furukawa *et al.* [82], and Hook *et al.* [83] report that the hot carrier lifetimes in NMOSFETs increase with high doses of implanted nitrogen ($2.5 \times 10^{14}$ $N_2^+$ and above at 10–20 keV). In fact, the paper by Guarin *et al.* [81] reports an increase in the channel hot carrier NMOS lifetimes by as much as 20 times. This is likely due to fewer hydrogen passivated bonds at the interface in the presence of nitrogen. However, the reports of Liu *et al.* [13] and Chen *et al.* [84] indicate a minimal impact of nitrogen on the NMOS hot carrier lifetimes, although their implant dose conditions were much lower. At any rate, nitrogen implanted into silicon certainly does not degrade the NMOS hot carrier lifetimes, and therefore there are no lifetime-related device concerns from nitrogen implants to control the gate oxide thickness.

Liu *et al.* [13] also report that the short channel effects of PMOS transistors was improved while that of NMOS was not affected at $2\times10^{14}$ $N^+/cm^2$. Furukawa *et al.* [82] report that the short channel effects of NMOSFET were improved subsequent to a nitrogen implant into the channel region. Bin Yu *et al.* [78] also report that the $I_{\mathrm{on}} - I_{\mathrm{off}}$ characteristics of both NMOS and PMOS transistors are not degraded at a dose of $5\times10^{15}$ $N^+/cm^2$ at 40 keV through 200 nm of polysilicon and 5.5 nm of gate oxide. Kamgar *et al.* [35] report that the reverse short channel effect (RSCE) is reduced in nitrogen-implanted silicon transistors. However, they attribute this reduction to the decrease in the gate oxide thickness and not due to any inherent property of the nitrogen implant to reduce RSCE. At any rate, nitrogen does not increase the RSCE.

Guarin *et al.* [81], Adam [85], and Han *et al.* [86] report an increase in the interface trap densities $(N_{\mathrm{it}})$ with nitrogen-implanted silicon. The study of Guarin *et al.* [81] used charge pumping techniques to determine the interface charge density on NMOS transistors. Adam [85] used the technique of Corona Oxide Characterization of semiconductor (COCOS) [87] to determine the interface trap density of nitrogen implanted p-type silicon in his study. Han *et al.*, [86] used the shift of the flatband voltage to determine the interface traps on n-substrates. Although the studies used different techniques and different substrate types to determine the interface traps subsequent to nitrogen implantation, they all arrived at the same conclusion, i.e., nitrogen implantation increases the interface trap density. The studies in [81] and [85] quantify the interface trap density subsequent to nitrogen-implanted silicon. The numbers reported are in the $10^{10} - 10^{11}$ traps/$cm^2$ range. This is shown in Fig. 11. The difference in their reported interface densities could be attributed to the difference in the processing conditions. While the study of Guarin *et al.* [81] was performed on MOS transistors, Adam's study [85] used MOS capacitors. Further, Adam's

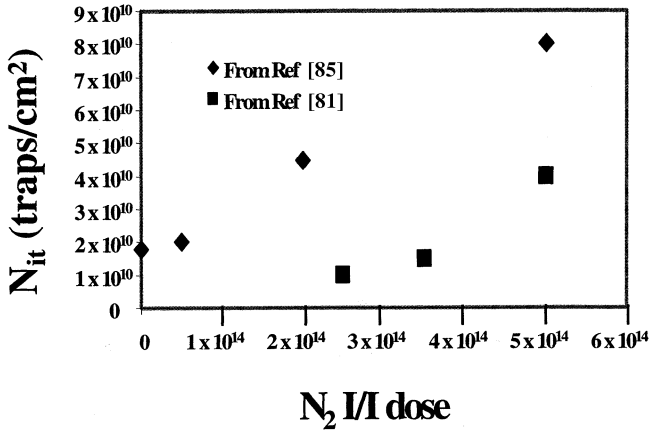


Fig. 11. Interface trap density as a function of the nitrogen ion implant dose. The implant energy was in the 10–20-keV range in [81] and 40 keV in [85]. The data in [84] were measured from MOS capacitors while the data from [81] were measured from 0.45 $\mu$m $L_{\text{design}}$ NMOSFETs. Further, the data from [85] are after an oxide growth at 800 °C for 25 min and a forming gas passivation anneal. The processing conditions for the data from [81] are not reported. Although the processing conditions were not the same in the data from the two references, it shows that nitrogen implantation increases the interface trap density.

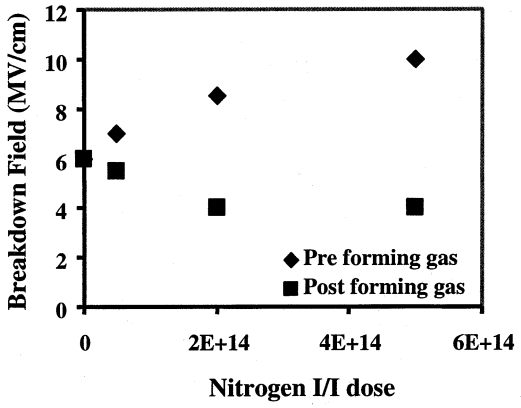


Fig. 12. Breakdown voltage before and after a forming gas anneal of MOS capacitors as a function of nitrogen I/I dose for thermal oxides grown at 800 °C for 25 min. Data are from [85].

study used 800 °C, 10 and 25 min for the gate oxidation, while these data are not reported in the study of Guarin *et al*. [81]. Further, the study of Adam [85] showed that the breakdown fields of the gate oxide dielectric increased with nitrogen implanted dose prior to the forming gas passivation anneal. However, the opposite effect was observed after a forming gas anneal. This is illustrated in Fig. 12. Generally, hydrogen is not believed to introduce bulk traps in silicon. Therefore, in general, the forming gas anneal is not expected to affect the breakdown fields which are controlled predominantly by the bulk traps in the oxide [88]. However, at least in the case of nitrogen-implanted material, that is not the case.

Yasuoka *et al*. [30] show that the effective hole mobility is not degraded at both low and high fields even for a high dose of $4 \times 10^{15}$ N$^+$/cm$^2$ at 10 keV. Liu [13] report that the mobility of the electrons and holes are not particularly degraded by nitrogen implantation into silicon. In general, nitrided films exhibit degraded mobility at low transverse fields and enhanced mobility at high fields [17], [89].

Cheung *et al*. [90] shows that the electron and hole trapping during Fowler–Nordheim injection is suppressed by the incorporation of nitrogen at the gate oxide/Si interface subsequent to nitrogen implantation and oxide growth. This has also been corroborated by other researchers who show that charge to breakdown ($Q_{bd}$) and time to breakdown (TBBD) also increase in the case of nitrogen-implanted silicon [13], [15], [17], [78], [86], [91]. Lin *et al*. [92] report that the $Q_{bd}$ worsens in the case of implanted nitrogen. However, their results are not consistent with those of the other reports in the literature.

Kimizuka *et al*. [93] and Liu *et al*. [94] report that the negative bias temperature instability (NBTI) of pMOSFETs degrades subsequent to nitrogen implantation. The general belief in the industry is that nitridation of the gate oxide—whether through implantation or other methods—degrades NBTI. However, the models to establish NBTI mechanisms are still under development and more work in this area is required to be definitive.

Nitrogen implantation has also been shown to improve the plasma damage immunity for gate oxides even for low doses of $2 \times 10^{13}$ N$^+$ into silicon [90]. Nitrogen-implanted polysilicon resistors have also shown superior temperature coefficient of resistance and voltage coefficient of resistance and reduced resistance mismatch, which are important in comparator design [95]. Nitrogen implantation has also been shown to improve the thermal stability of Cobalt silicide ($CoSi_2$) polycide gate MOS devices [96]. This in turn improves the polysilicon resistance and the series resistance of the source/drain regions. Nitrogen implantation into the source/drain regions on SOI MOSFETs has also shown improvements in drain leakage currents [97].

## V. Alternate Techniques

Thus far, the discussion has concentrated on achieving multiple gate oxide thickness for SOC through nitrogen implants. However, there have also been reports in the literature of achieving multiple gate oxide thickness through fluorine incorporation into the oxide [44]–[46], [98]. These papers report that the introduction of fluorine into the oxide through chemical or implantation methods enhances the oxidation rate. The physics behind the behavior of fluorine in the oxide is not yet well understood. Fluorine is also used in silicon technology to retard the diffusion of boron under some conditions in the fabrication of ultrashallow junctions [99]. However, this paper will focus only on the application of fluorine to produce multiple gate oxides. It has been shown that fluorine incorporation into pure oxides shows improved electrical device characteristics in terms of hot carrier reliability, reduces interface trap density, immunity to ionizing radiation, NBTI, and flatband voltage shifts [100]–[106]. The drawback, however, is that fluorine incorporation into the oxide also enhances the penetration of boron from the p$^+$ poly gate into the oxide and the underlying silicon substrate [107].

In the context of multiple gate oxide thickness, the fact that fluorine enhances the oxidation rate could mean the possibility of a scheme where the thinnest oxide does not receive a fluorine implant while the thickness of the other oxides is moderated by the fluorine implant. The main disadvantage with this process is that the thinnest oxide is a pure oxide and therefore most susceptible to device degradation due to tunneling, dopant

penetration from the polysilicon, etc. One possible argument to overcome this limitation is to use a nitrided oxide process and then introduce fluorine into the thicker oxides to moderate oxide growth. A recent paper by Hook *et al*. [83] discusses the electrical characteristics of fluorine implanted into nitrided ($N_2O$) oxides. They report an improvement in hot carrier immunity, flicker noise, and NBTI with fluorine-implanted polysilicon. However, the introduction of fluorine introduces much larger $V_T$ shifts for the NMOS than the PMOS. They also show that the introduction of fluorine increases the interface trap density in the upper half of the bandgap, thereby affecting the NMOS devices. The focus of Hook's work was on the effect of fluorine on the electrical properties of nitrided oxides and not the applicability of fluorine implants to moderate oxide thickness per se. However, one can try to gain some insight from their results on the suitability for using fluorine implants to moderate oxide thickness. In [83], the authors report a retained dose in the oxide of about 5%–15% for the doses investigated. At an implant dose of $2.5 \times 10^{14}/\text{cm}^2$, they report that the oxide thickness increases only by 0.1–0.2 nm for a 3.5-nm oxide. Similar weak dependencies of the oxide thickness on the implanted fluorine dose have also been shown by Tsai *et al*. and Wright and Saraswat [45], [46]. Therefore, the applicability of fluorine in multiple gate oxide thickness technologies that may need oxide thickness in the range of a few multiples (say ~2–9 nm) appears problematic as it will require extremely high doses of fluorine. The introduction of fluorine through plasma-nitrided gate oxides degrades device performance through a large increase in the interface trap densities ($\sim 1 \times 10^{12}/\text{cm}^2$) and introducing substantial $V_T$ shifts with marginal increase in oxide thickness [108]. Furthermore, very high doses of fluorine were required to effect this marginal increase in the oxide thickness. Apart from dose loss of fluorine in the oxide, another possible reason could be due to the fact that nitrogen at the $Si/SiO_2$ interface has the effect of retarding the oxide thickness and hence high doses of fluorine is required to overcome the oxide growth retardation effect of nitrogen.

To summarize the above discussion on fluorine, pure oxide processes are not widely used in ULSI applications and the introduction of fluorine into nitrided oxides does appear to hold much promise for multigate oxide thickness processing.

More recently, Wakabayashi *et al*. [31], Ranade *et al*. [109], and Lin *et al*. [110] have reported that implanting nitrogen into Mo and TiN metal gates varies the work function. In Mo gates, the work function difference is a function of the dose of the nitrogen implanted. When metal gate technology becomes mainstream, this technique can then potentially be used to vary the threshold voltage and therefore obtain multi-$V_T$ devices for SOC.

## VI. Future Challenges

We have seen in the earlier sections that nitrogen incorporation at the $Si/SiO_2$ interface–especially through nitrogen implantation offers a technologically viable solution for multiple gate oxide growth for SOC. However, the picture is still not complete. We need a better understanding of the bonding of nitrogen at the $Si/SiO_2$ interface subsequent to nitrogen implantation and diffusion. The model of Adam *et al*. [63], [64] explained in Sections II and III only takes into account the accumulation of nitrogen at the interface limited by the surface site density. A study of the bonding of implanted nitrogen at the interface could help such models to better explain the oxidation retardation and also better explain the electrical data observed. While Section IV does provide a discussion on the device characteristics subsequent to nitrogen implantation, it will be more insightful to relate that to *ab initio* and experiment-based bonding arguments. It must be mentioned that there have been some *ab initio* bonding configuration studies performed on NO and $NH_3$-based nitridation processes [111]–[114]. However, it is quite possible that the bonding characteristics of nitrogen at the interface subsequent to implantation and diffusion in silicon is different from that of the above studies due to the different mechanisms and atomistics involved in how the nitrogen reaches the interface. This would require *ab initio* efforts augmented by characterization techniques like X-ray photoelectron spectroscopy (XPS) and time of flight SIMS (TOF-SIMS).

The window of optimization of the nitrogen implant should also be investigated in more detail. High doses of nitrogen (at about $5 \times 10^{14}$ $N_2^+$ and above at 40 keV) show that extended defects are created in the silicon substrate [115]. Similar effects are observed at comparable doses at 20 keV and below [39], [116]. At high doses, due to interactions with extended defects and possibly due to the finite number of interface sites, the effective diffusion of nitrogen toward the surface is slowed down. The diffusion behavior of nitrogen implanted at moderate doses after amorphizing doses of silicon has been modeled quite successfully [65]. However, a detailed understanding of the interaction of nitrogen with various types of extended defects under high dose nitrogen implant conditions needs further investigation. Therefore, there may exist a process window where the use of nitrogen implants may be attractive with minimal additional complexities arising from extended defect considerations. This will make the integration of the nitrogen implant process into existing manufacturing process flows particularly attractive. As mentioned in Section IV, the breakdown voltage of nitrogen implanted oxides decreases after a forming gas passivation anneal. This needs to be investigated further and understood.

The studies on moderating oxide growth subsequent to nitrogen implantation are based on the implantation of nitrogen into silicon. There have been a few papers that report device characteristics subsequent to nitrogen implantation into polysilicon [40], [78], [96]. The diffusion behavior of implanted nitrogen in polysilicon has also been studied through SIMS analysis by Nakayama *et al*. [117]. This method could possibly help reduce the interface trap density at the $Si/SiO_2$ interface while still achieving the device benefits of nitrogen implantation like suppression of boron penetration, gate current reduction, etc. The work in [78] reports that high doses of $1 \times 10^{16}/\text{cm}^2$ $N^+$ at 40 keV into polysilicon degrades transistor performance through poly depletion and increased sheet resistance. It needs to be investigated if there exists a window of optimization at lower doses where nitrogen implantation into polysilicon can be technologically attractive.

D'Souza *et al*. [118] and Liu *et al*. [119] reports that the $1/f$ flicker noise is improved as a result of nitrogen implantation as

compared to pure and NO-based nitrided oxides. However, the mechanism by which this occurs is not yet well understood. The effect of NBTI on nitrogen-implanted PMOSFETs also need to be better understood. As explained in the previous section, the applicability of nitrogen implants into metal gates is also quite promising. However, this needs much further investigation as well.

## VII. Summary

In this paper, we have reviewed the status of multiple gate oxide technologies for SOC with an emphasis on nitrogen-implant based techniques. We have reviewed how nitrogen diffuses in silicon and then moderates oxide growth. We also briefly explained models to support the same. We then went on to explain the device issues subsequent to nitrogen implantation and showed that nitrogen implants improve most of the device characteristics. Next, we reviewed alternate implant techniques that can also be used to achieve multi-$V_T$ devices. Based on the material presented, we believe that nitrogen implantation is currently a strong candidate for multiple oxide thickness technologies for SOC processes as the process integration complexity increases. Finally, we presented some missing gaps and identified some future directions to help develop a more comprehensive understanding of the use of nitrogen implants in silicon processing for SOC technologies.

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