Three-Dimensional Base Distributed Effects of Long Stripe BJT's: AC Effects on Input Characteristics

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***Abstract*— The small-signal voltage and current distributed effects in the polysilicon and intrinsic base regions of long stripe bipolar junction transistors (BJT's) at high frequencies are investigated, and simple analytic equations describing the voltage and current distribution in these regions are derived. It is shown that the frequency-dependent debiasing effects in the polysilicon contacts and intrinsic base region change the current behavior and modulate the input admittance. The current and voltage distributions in the polysilicon region are nonuniform and vary with frequency. Conventional two-dimensional (2-D) device simulations cannot accurately predict this three-dimensional (3-D) effect. A quasi-3D simulation scheme combining a 2-D device simulator and the distributed model is presented to properly and efficiently describe the input characteristics of the device at high frequencies. It is also shown the use of various polysilicon sheet resistances, geometry sizes, and layout structures changes the distributed characteristics and modulates device performance at high frequencies. The impact of the layout structure and geometry size on RF circuit design due to the distributed effects is also studied.**

***Index Terms*— Base resistance, bipolar transistor, debiasing, device simulation, three-dimensional.**

I. Introduction

DESIGN considerations for a microwave amplifier include stability, power gain, bandwidth, noise, and dc bias requirements [1]. A construction of an integrated circuit microwave amplifier usually starts with a proper design of the transistor; then the matching networks of the input and output ports are determined for a particular stability and gain criteria. An unconditionally stable transistor will not oscillate with any passive termination. On the other hand, a design using potentially unstable transistors requires careful analysis so that the matching network produces a stable amplifier. Thus, the accurate determination of the transistor characteristics is the first step to optimize the performance of a microwave amplifier.

The input impedance of a bipolar transistor in the common-emitter configuration is usually difficult to predict either by compact models or two-dimensional (2-D) device simulations due to the three-dimensional (3-D) distributed effect in the base region. This effect decreases the base admittance in magnitude with increasing frequency as a result of a high-frequency internal biasing effect. Several authors [2]–[4] have modeled the base impedance with a uniform transmission line in the intrinsic base region to account for the ac distributed effect at high frequency operations. However, in double polysilicon bipolar transistors [5], [6], the distributed characteristic in the polysilicon base region can also be significant at high frequencies, and no studies of this effect has been reported. Neglecting this effect may result in an inaccurate estimation of input impedance in the transistor and a poor design of an amplifier.

In this paper, we concentrate on the distributed effect in the polysilicon base region and its effect on the input characteristics of transistors and circuit performance. Since the distributed effect is a 3-D problem, a 3-D device simulator is required to characterize the input behavior of the device. However, 3-D device simulations are rarely used in device design due to extensive demands on hardware and CPU time. An accurate and efficient quasi-3D simulation scheme is proposed to characterize the input behavior of stripe bipolar junction transistors (BJT's) at high frequencies. In the scheme, a 2-D device simulation of FLorida Object Oriented Device Simulator (FLOODS) [7], [8] is combined with an analytical model to deal with the voltage and current nonuniformity in the third dimension of the device due to the distributed effects in the base polysilicon region. In high frequency simulations, the parasitic effects are extremely important. A coupled device/circuit simulator can take into account the parasitic effects and solve the device characteristics efficiently. Currently, these types of simulators have been applied to the steady state and transient cases of devices and circuits [9], [10]. However, the capability of performing ac simulations, one of the most important applications, is not yet available. A "tightly coupled" device/circuit simulation scheme is implemented into FLOODS for dc and ac simulations and the results are verified by comparing with the measured data. Uses of various base polysilicon sheet resistances, layout structures, and geometry sizes on the ac performance of BJT's are also investigated. The importance of the distributed effects on the RF circuit design is demonstrated as well.

II. Model Development

Fig. 1 illustrates three popular layout structures usually used in radio frequency (RF) design with double-polysilicon self-aligned BJT technologies. A single metal base (SMB) contact layout structure indicated in Fig. 1(a) has a metal base contact at one side of polysilicon contact (NPOLY, or Near POLY).

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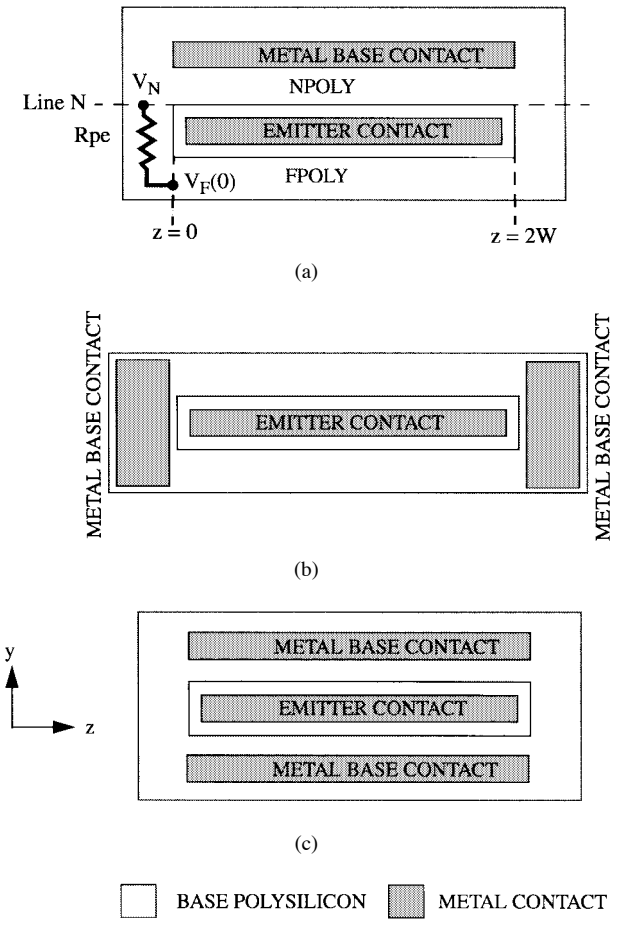


Fig. 1. Three layout structures for high speed BJT's. (a) Single metal base contact structure (SMB). (b) Interdigitated structure. (c) Double metal base contact structure (DMB), which is equivalent to a 2-D simulation structure because of the uniform voltage and current distribution in the z-direction. To compare with the other structures, the contact position of the interdigitated structure is slightly different from conventional interdigitated structure.

The base current at the other side of emitter is conducted through FPOLY (Far POLY) in the z-direction. The distributed effect occurs in FPOLY due to the relatively higher polysilicon sheet resistance than metal resistance. This structure is used as an example to model the 3-D base distributed effects. The same methodology is also applicable to an interdigitated structure [Fig. 1(b)], where the metal base contact locates at the short edge of emitter. Base current injecting into the active base region flows through two polysilicon fingers and the distributed effect takes place in both fingers. A double metal base (DMB) contact structure illustrated in Fig. 1(c) has a metal contact at each side of the base polysilicon contact. The distributed effect along the z-direction is negligible since the metal sheet resistance is quite small resulting in uniform voltage and current density distribution in the z-direction. Therefore, a DMB structure is equivalent to a 2-D device simulation structure where the voltage and current are assumed to be constant in the third dimension.

Fig. 2(a) shows the distributed network representation of a rectangular active base region if the emitter and collector contacts are ac grounded [2]. The diode represents the junction between the base and emitter, $R_{b\text{ext}}$ is the lumped extrinsic

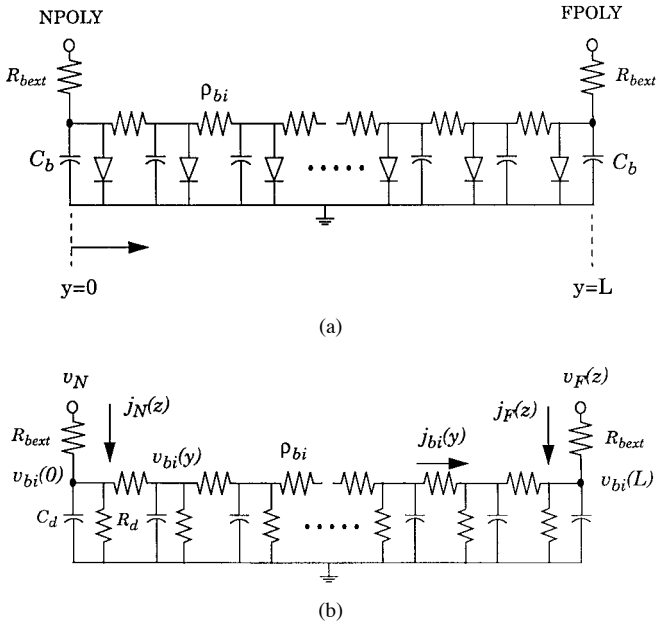


Fig. 2. Models of the distributed network in the active base region. (a) Large-signal equivalent circuit. (b) Small-signal equivalent circuit.

base resistance between polysilicon contact and intrinsic base region, ρ_{bi} is the intrinsic base resistivity, and the capacitance C_b accounts for the base-collector depletion capacitance under the emitter area and the geometric parasitic capacitance of the device. At a specific dc bias, the diode can be linearized by a parallel differential resistance R_d and a capacitance if the series inductance is negligible [11]. The small-signal admittance of a section can be represented by $Y_d = R_d^{-1} + jwC_d$ at a specific angular frequency w, where C_d includes the diffusion and depletion capacitance of the base-emitter junction and C_b. The complete small-signal equivalent circuit is plotted in Fig. 2(b).

At high current densities, high-current effects such as the Kirk effect [12] cause an increase of the transit time and, hence, a reduction of the cutoff frequency f_T. Because of this, we thus limit our interests in the current range where the maximum f_T is achieved. For the BJT device analyzed in [13], the maximum f_T is achieved at $V_{be} = 0.83$ V. Under this condition, the dc debiasing effects in the intrinsic base as well as polysilicon base regions are not significant (see [13, Fig. 3]) and the current injection from base to emitter is approximately constant in the intrinsic base area. Thus, Y_d can be assumed to be uniform across the intrinsic base region, and the network becomes a uniform RC transmission line.

The governing equations of the transmission line model can be expressed as second-order differential equations [3]. The solutions, the small-signal voltage $v_{bi}(y)$ and transverse current density $j_{bi}(y)$ in the intrinsic base region [see Fig. 2(b)], are given by

$$j_{bi}(y) = C_1 \sinh(\sqrt{Y_d \rho_{bi}}\, y) + C_2 \cosh(\sqrt{Y_d \rho_{bi}}\, y) \quad (1)$$

and

$$v_{bi}(y) = -\sqrt{\frac{\rho_{bi}}{Y_d}}\,(C_1 \cosh(\sqrt{Y_d \rho_{bi}}\, y) + C_2 \sinh(\sqrt{Y_d \rho_{bi}}\, y)) \quad (2)$$

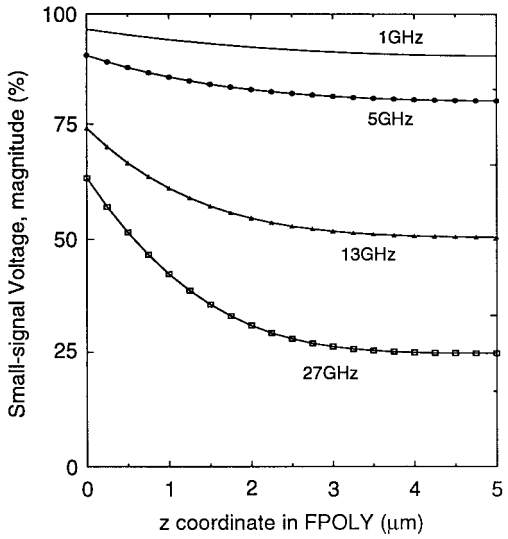


Fig. 3. Amplitude of the small-signal voltage along FPOLY calculated by the model. The emitter stripe length is 10 μm. The voltage and current are assumed to be symmetric to the center of the polysilicon base contact in the z-direction.

where

$$C_1 = -\sqrt{\frac{Y_d}{\rho_{bi}}}v_{bi}(0) \tag{3}$$

$$C_2 = j_{bi}(0). \tag{4}$$

The small-signal j-v relations at the boundaries of the intrinsic base region are

$$j_{bi}(0) = C_3 \cdot v_{bi}(0) - C_4 \cdot v_{bi}(L) \tag{5a}$$

and

$$j_{bi}(L) = C_4 \cdot v_{bi}(0) - C_3 \cdot v_{bi}(L) \tag{5b}$$

where

$$C_3 = \sqrt{\frac{Y_d}{\rho_{bi}}}\coth(\sqrt{Y_d\rho_{bi}}L) \tag{6}$$

$$C_4 = \sqrt{\frac{Y_d}{\rho_{bi}}}\,\mathrm{csch}(\sqrt{Y_d\rho_{bi}}L) \tag{7}$$

and L is the intrinsic base length. Using the same treatment as in the dc model [13], the relations of the terminal current densities and voltages at the polysilicon base contacts are given by

$$j_N(z) = j_{bi}(0) = C_5 \cdot v_N - C_6 \cdot v_F(z) \tag{8a}$$

and

$$j_F(z) = -j_{bi}(L) = C_5 \cdot v_F(z) - C_6 \cdot v_N \tag{8b}$$

where

$$C_5 = \frac{C_3 + C_4C_7R_{b\mathrm{ext}}}{1 + R_{b\mathrm{ext}}(C_3 + C_4)} \tag{9}$$

$$C_6 = \frac{C_4 - C_4C_7R_{b\mathrm{ext}}}{1 + R_{b\mathrm{ext}}(C_3 + C_4)} \tag{10}$$

and

$$C_n = \frac{C_3 - C_4}{1 + R_{b\mathrm{ext}} \cdot (C_3 - C_4)}. \tag{11}$$

The following assumptions are made in the derivation of the distributed model in the base polysilicon region.

1) The capacitance associated with the polysilicon base is neglected since it is in parallel with C_d and much smaller than C_d.
2) Since we limit our interests in the bias conditions before high current effects occur, the dc voltage bias is approximately constant along FPOLY, as can be seen in [13, Fig. 3].
3) The admittance Y_d is constant everywhere in the intrinsic base region due to the small dc voltage variation in FPOLY and the intrinsic base region.
4) The small-signal voltage along lineN in NPOLY [see Fig. 1(a)] is constant due to the small debiasing effect in NPOLY.

Therefore, following the same methodology used to solve the dc problem, the analytical solutions of voltage $v_{PF}(z)$ and current $j_{PF}(z)$ in FPOLY can be written as

$$v_{PF}(z) = v_{PF}(0) + \frac{j_{PF}(0)\rho_p}{C_8\sinh(C + 8W)} \cdot (\cosh((C_8(W - z)) - \cosh(C_8W))) \tag{12}$$

and

$$j_{PF}(z) = \frac{j_{PF}(0)}{\sinh(C_8W)} \cdot \sinh(C_8(W - z)) \tag{13}$$

where W is half of the emitter stripe length, ρ_p is the resistivity of base polysilicon

$$C_8 = \sqrt{\frac{C_5\rho_p}{A_p}} \tag{14}$$

and A_p is the cross section area of FPOLY. If the current injection from the short edges of emitter stripe is negligible, then the boundary conditions of small-signal voltage $v_{PF}(z)$ and current $j_{PF}(z)$ are given by

$$j_{PF}(0) = \frac{(C_5 - C_6)W}{C_9A_p} \cdot v_N \tag{15}$$

and

$$v_{PF}(0) = v_N - A_pR_{pe}j_{PF}(0) \tag{16}$$

where R_{pe} is the connecting polysilicon resistance between NPOLY and FPOLY and

$$C_9 = 1 - \frac{C_5\rho_p}{A_pC_8^2} + C_5WR_{pe} + \frac{C_5\rho_pW\coth(C_8W)}{A_pC_8}. \tag{17}$$

Note that the only variable in (15) and (16) is v_N which is the given small-signal bias at NPOLY.

TABLE I
THE DEVICE PARAMETERS REQUIRED FOR MODEL

parameters	value
Emitter width (Intrinsic base length), L	0.46μm
Intrinsic base width, W_b @Vbe=0.85V, Vcb=2V	0.05μm
Unit length extrinsic base resistance, R_{bext}	55Ω.μm
Intrinsic base resistivity, ρ_b @Vbe=0.6V, Vcb=2V	482Ω.μm
Polysilicon sheet resistance	78.4Ω/sq
Polysilicon thickness	0.25μm
FPOLY width	0.2μm
FPOLY cross section area, Ap	0.25 x 0.2μm^2
FPOLY connecting resistor, Rpe	274Ω
Emitter stripe length, 2W	10μm

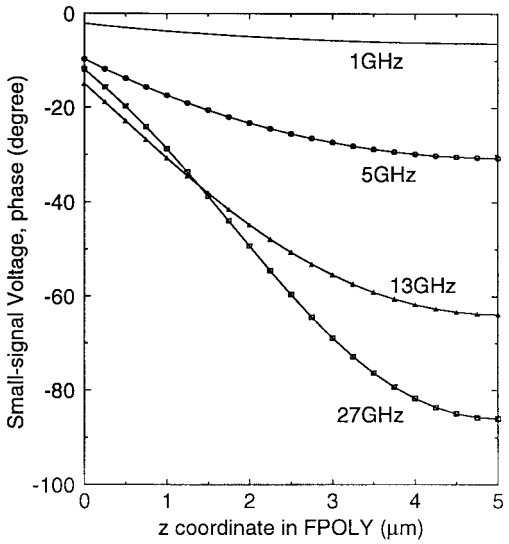


Fig. 4. Phase delay of the small-signal voltage along FPOLY computed by the model. All the phase delays refer to the voltage v_N.

III. RESULTS AND DISCUSSION

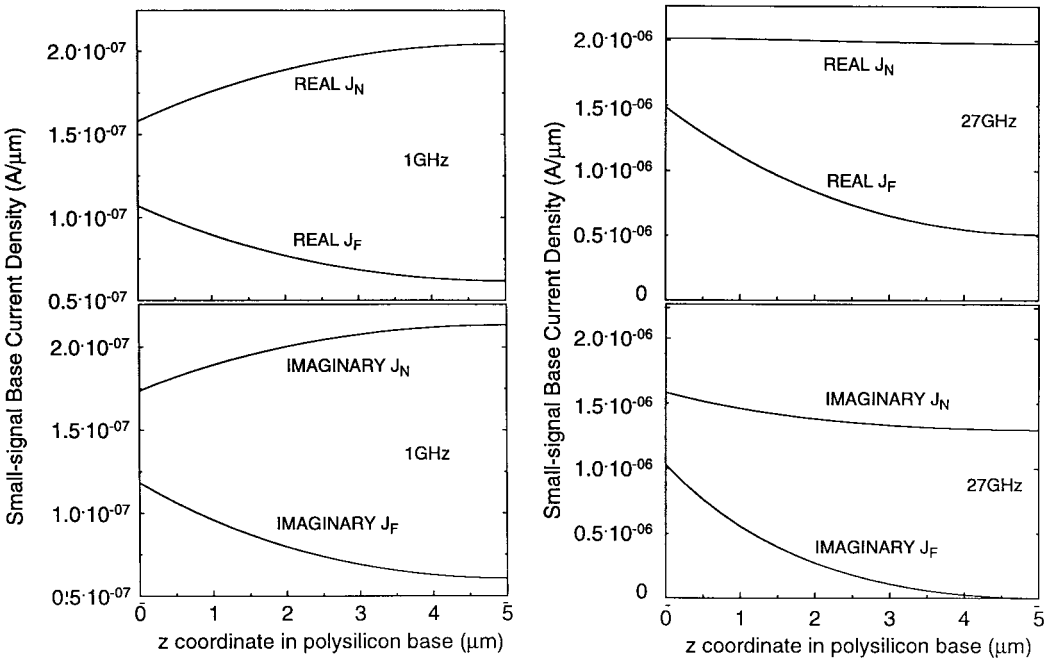
A device with a cutoff frequency of 32 GHz is used for the analysis. The device parameters are summarized in Table I. In all cases, dc biases $V_{be} = 0.85$ V and $V_{cb} = 2$ V are applied to the transistor. Fig. 3 shows the amplitude of the small-signal voltage along FPOLY at different frequencies. At low frequencies, the base current in the intrinsic base region is dominated by the current conducted through the resistance R_d. This current is small and has no significant debiasing effect in the active and polysilicon base regions. There is also no phase delay due to the insignificant capacitive characteristics of the network, as can be seen in Fig. 4. The displacement current through C_d increases with the frequency and eventually dominates the base current at high frequencies. The increasing current causes larger ohmic voltage drops along the FPOLY. For instance, the amplitude of the total small-signal current flowing through the FPOLY at 27 GHz is ten times larger than that at 1 GHz. The variation of small-signal voltage in FPOLY is more than 60% at a frequency of 27 GHz, whereas the variation is within 7% when the operation frequency is 1 GHz. The phase delay also increases at higher frequencies due to the prominent capacitive characteristics.

The modeled small-signal base current densities injecting from the polysilicon contact to the active base region are shown in Fig. 5 as a function of position in the base polysilicon. Fig. 5(a) illustrates the current densities when the operating frequency is 1 GHz. At this frequency, the current injection across the junction is approximately constant since the ohmic voltage drop is so small along the base polysilicon as well as in the intrinsic base region. However, the small ac debiasing in FPOLY does cause small but asymmetric ac biases between the base contacts. A similar current dividing phenomenon takes place in the intrinsic base region as that observed in the dc asymmetric bias conditions [13]. An obvious nonuniform current distribution is observed in both sides of the base polysilicon contacts and both the real and imaginary currents exhibit the compensation property as seen in the dc low current injection cases, i.e., the current lost in the FPOLY is balanced by the increase of current in the NPOLY, and the total current is approximately constant compared with the case of uniform bias in the FPOLY. As the frequency increases, the debiasing effect along the FPOLY becomes significant due to the increasing current resulting in a large decrease of ac voltage across the junction in the active base region. Thus, the total current decreases compared with the case of uniform bias in the FPOLY. Fig. 5(b) shows the current densities at 27 GHz. Note the ac current at 27 GHz is higher than that at 1 GHz which results in the considerable debiasing effect in FPOLY. Both the real and imaginary currents at both sides decrease toward the center of polysilicon base. So, both the real and imaginary base current calculated by a model that does not take into account the distributed effects in the polysilicon base region will be overestimated.

To characterize the high-frequency performance of a transistor, 2-D device simulations are frequently used. A key assumption of the simulations is that the voltage and current distribution in the third dimension are uniform. The results obtained using our 3-D distributed model suggest the assumption may be invalid in certain structures; for some cases, a 3-D device simulator is required. However, 3-D device simulations are rarely used in device design due to extensive demands on hardware and CPU time. The use of a 2-D device simulator coupled with the analytical model to handle the variation of voltage and current in the third dimension is an efficient way to characterize these transistors.

IV. QUASI-3D SIMULATIONS

The distributed model is coupled to FLOODS by effective contact lengths. Referring to the base current density plot as shown in Fig. 5, the total current $I_{N,F}$ associated with each side of the polysilicon base contact is the integration of the current density $J_{N,F}(z)$ along the polysilicon length



(a) (b)

Fig. 5. Small-signal base current densities inject from polysilicon base contact to active base region at a frequency of (a) 1 GHz and (b) 27 GHz.

(z-direction) which can be expressed as

$$I_N = j_{PF}(0) \cdot A_p \tag{18}$$

and

$$I_F = C_5 W v_N - C_6 W v_{PF}(0) + \frac{C_6 W \rho_p j_{PF}(0)}{C_8} \coth(C_8 W) - \frac{C_6 \rho_p j_{PF}(0)}{C_8^2}. \tag{19}$$

$I_{N,F}$ is also equivalent to the current density at the edge of polysilicon contact $J_{N,F}(0)$ times the effective contact length $L_{\text{eff},N,F}$, i.e., $I_{N,F} = J_{N,F}(0) \times L_{\text{eff}N,F}$. Fig. 6 illustrates the definition of effective lengths in the NPOLY and FPOLY for the current densities shown in Fig. 5(a). L_{eff} of NPOLY is longer than the actual polysilicon contact length L_{actual} since the current density increases along NPOLY. In contrast, L_{eff} of FPOLY is shorter than L_{actual} due to the decreasing current density along FPOLY. Thus, if we obtain the edge current densities $J_{N,F}(0)$ from FLOODS 2-D simulations and multiply by the $L_{\text{eff},N,F}$ from the model, we get the actual contact current from the nonuniform 3-D effect of the transistor.

The comparison of L_{eff} from the model and FLOODS 3-D simulations are plotted in Fig. 7 as a function of frequency and base polysilicon sheet resistance R_{sh}. At low frequencies, L_{eff} of NPOLY is longer and L_{eff} of FPOLY is shorter than L_{actual} ($= 5$ μm). The use of higher R_{sh} increases the difference. However, the sum of the two L_{eff}'s approximately equals two times L_{actual} due to the division of the constant base current between the two polysilicon contacts when the debiasing in the intrinsic base region is negligible. At intermediate frequencies, the magnitude of the small-signal voltage in FPOLY decreases slightly while the phase delay results in a shift from imaginary

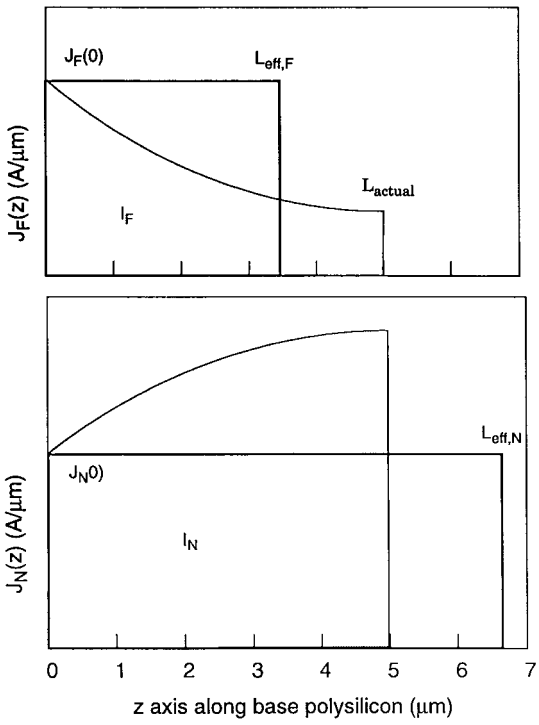


Fig. 6. Definition of effective length L_{eff}. The shaded area indicate the total current $I_{N,F}$ associated with each polysilicon base contact, which is also equivalent to the product of $L_{\text{eff},N,F}$ and $J_{N,F}(0)$.

to real current. Thus, the real L_{eff}'s become longer and the imaginary L_{eff}'s are shorter for both sides of the polysilicon contacts. As the operating frequency further increases, both the real and imaginary L_{eff}'s decrease for both contacts due to the large debiasing in FPOLY. The use of smaller R_{sh} in polysilicon contacts reduces the influences of debiasing effects

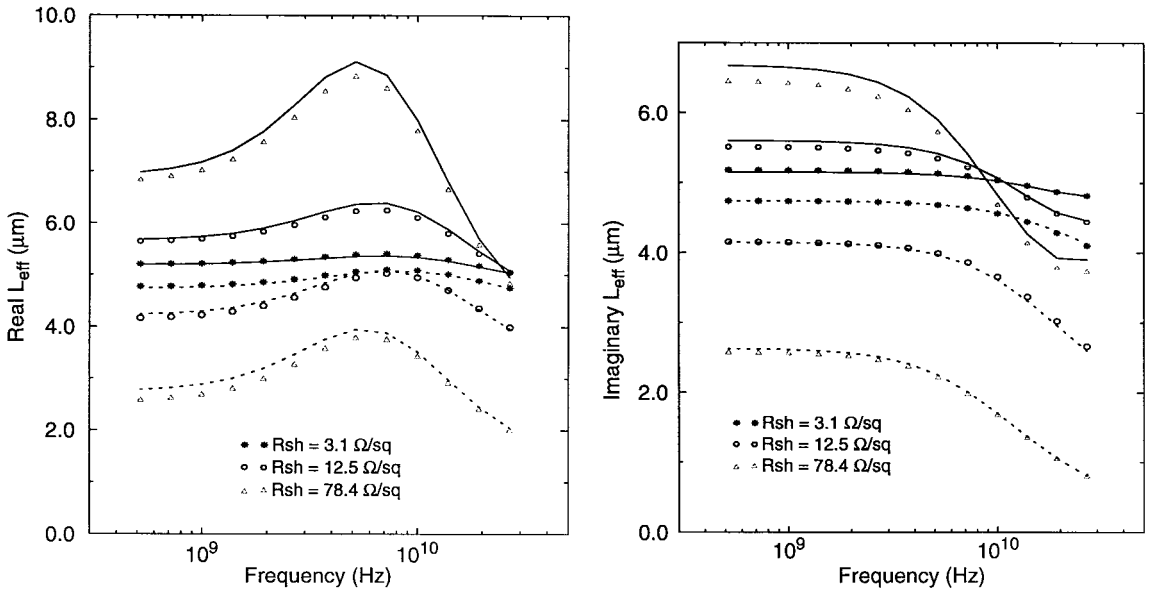


Fig. 7. (a) Real and (b) imaginary effective lengths of NPOLY and FPOLY in a SMB device at different frequencies. The symbols are obtained from 3-D simulations and lines are computed by 3-D distributed model. Solid lines indicate the $L_{\rm eff}$ curves of NPOLY and dashed lines are $L_{\rm eff}$ curves of FPOLY.

at all frequencies. Therefore, the $L_{\rm eff}$'s of both NPOLY and FPOLY are close to $L_{\rm actual}$ compared with devices having larger $R_{\rm sh}$. Good matches are obtained between the modeled and simulated $L_{\rm eff}$'s at all frequencies for different $R_{\rm sh}$'s verifying the accuracy and validity of the 3-D distributed model.

Quasi-3D simulations are performed using the coupling of 2-D simulations and $L_{\rm eff}$'s obtained in Fig. 7, and the resulting Y_{11}'s are compared with that of 3-D and 2-D simulations as shown in Fig. 8. For the DMB structure, Y_{11} from the 2-D simulation is the same as Y_{11} of the 3-D simulation since the voltage distribution in the polysilicon contacts of the device are uniform. Y_{11} of the SMB structure is similar to that of the DMB at low frequencies. The use of 2-D simulation can accurately predict the input characteristics of the SMB devices in this frequency range. However, Y_{11} of the SMB structures deviates from that of the DMB at high frequencies due to the debiasing and phase delay in FPOLY. The higher the sheet resistance, the larger the debiasing and phase delay, resulting in a bigger discrepancy between Y_{11} of the SMB and DMB structures. Two-dimensional simulation can no longer properly describe the input behavior of a SMB transistor at this condition. In contrast, quasi-3D simulations match the results of 3-D simulations at all frequency ranges of interest for various values of $R_{\rm sh}$.

To accurately simulate high-frequency characteristics of a transistor, the simulation structure must include all of the related parasitics outside the active region. In this device, the total area of interest is nine times larger than the active region. Since the structure contains sections which can be represented by lumped resistances or capacitances, simulation of the whole structure would be inefficient. The replacement of these large resistive or capacitive structures with lumped circuit components reduces a tremendous number of grid points which in turn reduces CPU time and memory requirements. To solve this problem, a circuit simulator has been implemented and tightly coupled to FLOODS where the device and circuit equations are solved simultaneously with Newton's method. The "tightly-coupled" method [9] requires no iteration between device and circuit simulations and exhibits better convergence than the "loosely-coupled" method [10], [14], [15]. In the equivalent structure, the device characteristics outside the active region are represented by lumped circuit components. The parasitic values can be obtained either from measurement or separate simulations.

Two-dimensional ac simulations are done to evaluate the parameters of the device. The coefficients C_5 and C_6 can be extracted from two 2-D ac device simulations with two different small-signal voltages applying to V_F while V_N is fixed. The knowledge of the detail device parameters, i.e., Y_d, ρ_{bi}, etc., is not required in this method. For each curve shown in Fig. 8, quasi-3D simulation requires about 400 M bytes of memory space and takes less than 4 h running on a Sun Ultrasparc 2 computer. In contrast, a 3-D simulation requires 1.5 G bytes of memory space running for more than 30 h.

The comparison of the measured and simulated Y_{11}'s of a BJT described in [13] is shown in Fig. 9 as a function of frequency. Fig. 9 shows both the 2-D and quasi-3D simulations are in agreement with the measured data at low frequencies since the debiasing is not significant at this frequency range. At high frequencies, 2-D simulation always overestimates the small-signal base current resulting in higher values of Y_{11}. In contrast, a quasi-3D simulation which takes into account the nonuniform distributed effect is in agreement with the measured data. The error of at cutoff frequency ($= 10.3$ GHz) is 2 and 21% for quasi-3D and 2-D simulations, respectively. The small discrepancy in the imaginary Y_{11} of the quasi-

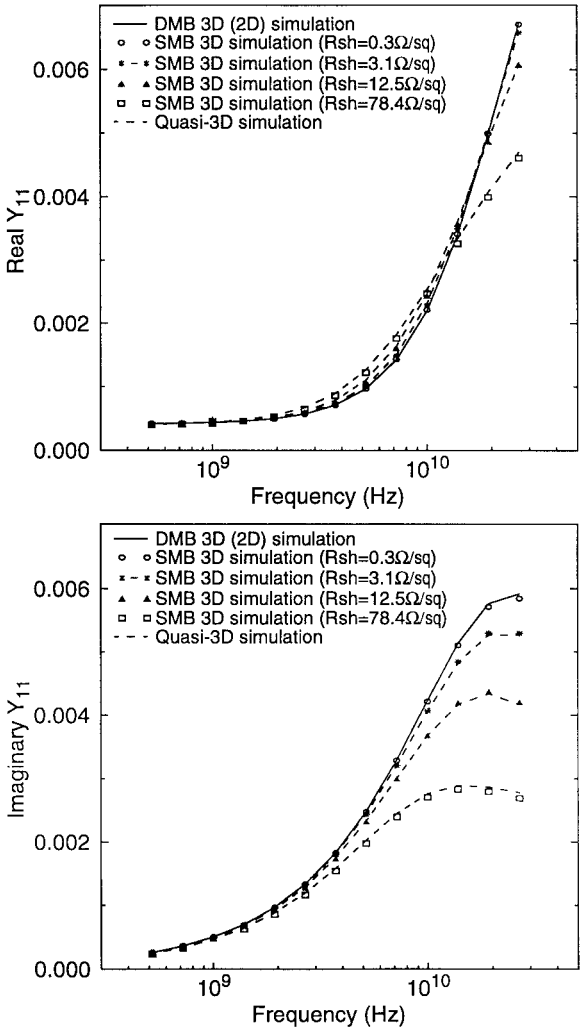


Fig. 8. Comparison of Y_{11} between 3-D, quasi-3D, and 2-D simulations with DMB and SMB layout structures.

3D simulation is probably due to the complicated parasitic network which cannot appropriately represented by the simple lumped circuit network.

V. Structure and Geometry Dependent AC Performance

The distributed effects acting in FPOLY of the SMB structure strongly influence the small-signal current behavior at high frequencies. For the interdigitated structure, similar distributed effects take place in both base polysilicon contacts. The modulation of current at high frequencies is more significant than in the SMB devices since debiasing occurs in both fingers of interdigitated structure. Fig. 10 compares Y_{11} for the DMB, SMB and interdigitated structures with $R_{\rm sh} = 12.5\ \Omega$/sq. It is seen that both the real and imaginary parts of Y_{11} of the interdigitated structure are smaller than that in the SMB device at high frequencies, and the deviation from Y_{11} of DMB is more significant compared with SMB devices. Thus, the characterization of the interdigitated structure with 2-D simulations results in a more significant error than the SMB structure.

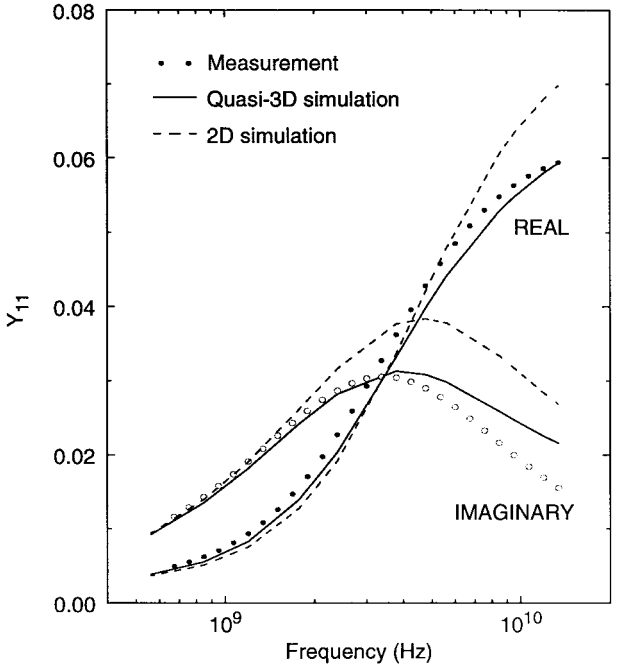


Fig. 9. Comparison of the measured and simulated Y_{11} as a function of frequency.

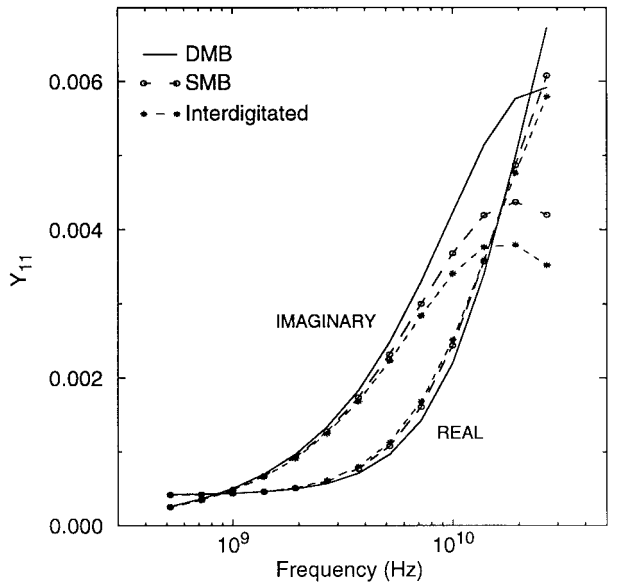


Fig. 10. Comparison of Y_{11} between DMB, SMB, and interdigitated structures with $R_{\rm sh} = 12.5\ \Omega$/sq obtained from 3-D simulations. The emitter stripe length is 10 μm.

The input and output small-signal current driving capability is usually assumed to be linearly proportional to the stripe length, and the phase delay in the polysilicon contacts are neglected. Y_{21} behaves similarly as Y_{11}, so the discussion will focus on Y_{11}. For the DMB structure, there are no distributed effects in the polysilicon contacts. Therefore, $|Y_{11}|$ is linearly proportional to the stripe length. The phase delays are also the same regardless of the length of the stripe used. Figs. 11 and 12 show the magnitude and phase of Y_{11}. However, in the presence of distributed effects, debiasing along FPOLY in the SMB and the fingers in interdigitated structures reduces

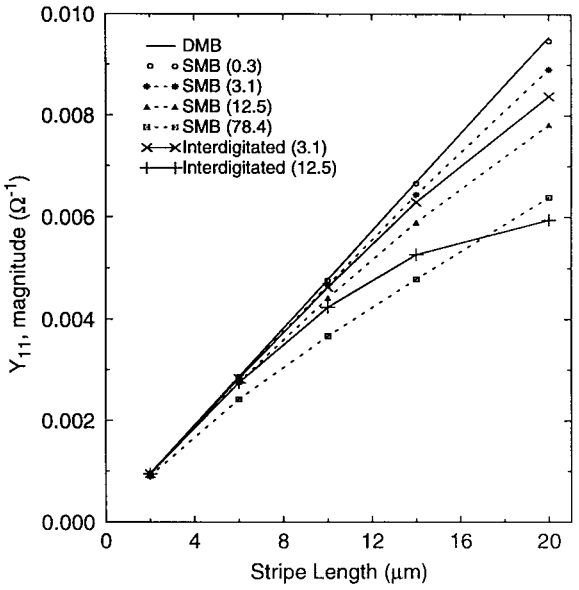


Fig. 11. Input current drive capability ($|Y11|$) of different layout structures as a function of stripe length and $R_{\rm sh}$ indicated in parentheses. The operating frequency is 10 GHz.

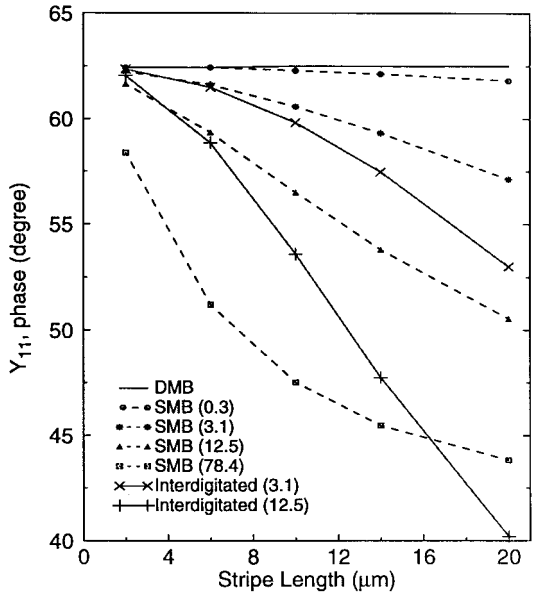


Fig. 12. The input phase delay ($\angle Y_{11}$) of different layout structures as a function of stripe length and $R_{\rm sh}$.

the input and output current drive and degrades the linearity at high frequencies. The signal propagating along FPOLY and the fingers also requires a longer time compared with that of the DMB structure resulting in additional phase delay. A longer stripe further degrades the current drive capability and enlarges the RC delay unless a very low value of $R_{\rm sh}$ is utilized. The sheet resistance of the base polysilicon contact plays a key role in determining current drive capability and phase delay in SMB and interdigitated devices.

The interdigitated structure has worse current driving capability and larger phase delay than the SMB device since the debiasing effects and RC delay take place in both polysilicon contacts. Due to distributed effects in the base polysilicon, at its worst, the current in a SMB device is totally supplied by NPOLY. For the interdigitated structure, the distributed effects keep affecting the current and phase delay as the frequencies and stripe length increase. Consequently, the input and output current drive of SMB devices increase monotonically, while the current supply of interdigitated devices tends to saturate as the stripe length increases. At the same time, the phase delay of the SMB is limited while that of the interdigitated structure keeps increasing following the increase of stripe length.

VI. Conclusion

An ac model has been developed to study the high frequency distributed effect of voltage and current in the intrinsic and polysilicon base regions. The small-signal voltage and current distributions in both regions have been described completely by the model. By the introduction of the effective contact length, the model has been used in conjunction with a 2-D device simulator for quasi-3D simulations. Y_{11} was extracted from quasi-3D simulations and compared with data from 3-D simulations and measurement. The results showed the quasi-3D simulations is accurate and significantly efficient than 3-D simulations.

The varied characteristics due to the use of different layout structures require individual design of the matching network. It is demonstrated that using 2-D device simulation, or applying an output matching network designed for a DMB structure to a SMB and interdigitated structure results in a significant degradation in the power gain. The stability properties can also be degraded in other cases. Therefore, the distributed effects must be taken into account in the design of SMB and interdigitated devices.

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