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Process dependence of 1/*f* noise and defects in ion implanted p-type piezoresistors

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The process dependence of 1/*f* noise in p-type piezoresistors was investigated in this work using both electrical and materials characterization approaches. P-type piezoresistors were fabricated with 20 keV and 40 keV boron implants with and without implant oxide and varying isochronal 900 °C inert anneals. The devices were characterized electrically using I-V, Hall Effect, and power spectral density (PSD) noise measurements. The defects were visualized using cross-section transmission electron microscopy and plane view TEM The measured 1/*f* noise PSDs in the p-type piezoresistors are systematically compared to the number and dimension of bulk defect densities measured with TEM after each annealing condition of the piezoresistors. The 1/*f* noise PSDs of the piezoresistors implanted with 20 keV boron track the TEM defect number densities while those implanted with 40 keV boron through SiO_2 with inert and oxidizing anneals track the faulted loop areas. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4740221]

I. INTRODUCTION

Noise plays an important role in the performance of analog integrated circuits and analog MEMS transducers since the minimum analog signal that can be detected and amplified is limited by noise. It has been observed that geometrically identical sensors fabricated with different fabrication processes may exhibit very different noise characteristics.[1,2] For example, in the MEMS piezoresistive microphone, the minimum detectable signal (MDS) can be reduced by improving the transducer sensitivity, reducing the noise, or both. Accordingly, researchers[3–12] have studied the process dependence of 1/*f* noise. Their results focus on electrical characterization of the noise power spectrum and indicate that low 1/*f* noise and low Hooge parameter α[13,14] can be achieved through low implant energy, long time or high temperature annealing conditions, good oxide quality, and a large number of carriers. In contrast for ion implantation studies, surface analytical techniques such as TEM are typically used to characterize the physical defects.[15–18] There is a need to compare the noise power spectrum present in the devices to the fabrication process and to the physical defects characterized by surface analytical techniques such as TEM. The contribution of this work is a comparison of the 1/*f* noise voltage power spectral density (PSD) to the bulk defects densities observed through TEM. The paper is organized as follows. First, the device fabrication is discussed followed by discussions of the experiment, noise power and surface analytical measurement results, and analysis.

II. FABRICATION

The silicon wafers used are 4 in.-diameter, N-type (phosphorous doped), (100) Czochralski-grown, 0.5–1 Ω cm, 525 ± 25 μm thick, and single side polished. Table I shows the implant and anneal conditions of the piezoresistors.

As shown in Table I, the piezoresistors are boron doped at 20 keV directly into the silicon substrate and at 40 keV through 0.1 μm of oxide into the silicon substrate. The implant oxide prevents channeling of the higher energy (40 keV) boron into the silicon substrate and also allows the peak concentration of the boron to reside inside the silicon near the Si/SiO_2 interface. The dose for each implant is fixed at 7×10^{14} cm^{-2} for a more straightforward analysis of the results. The depth range of the implants are computed using Florida Object Oriented Process Simulator (FLOOPS).[19] The ohmic contacts are implanted as is the channel with a dose of 7×10^{14} cm^{-2}. The surface concentration of the ohmic contact, from SIMS measurements, is on the order 1×10^{19} cm^{-3}.

After the boron ion implantation, an isothermal annealing at 900 °C was employed to investigate the time evolution of the defects. A passivation thermal 5 min dry/5 min wet/10 min dry oxide growth is performed on all the piezoresistors implanted at 20 keV, and piezoresistors implanted through an implant oxide at 40 keV are inert annealed for 10 and 30 min as shown in Table I.

III. EXPERIMENT

The electrical and surface analytical measurements performed are the noise power spectral density on piezoresistor devices and visualization of defects using TEM and Hall Effect on large-area samples that were subjected to the same process fabrication as the piezoresistors. Figure 1 shows the noise voltage setup which is composed of three nested Faraday cages, a low-noise preamplifier (SRS 560), a dynamic signal analyzer (SRS 785), lead-acid batteries, metal film

TABLE I. Piezoresistor implant and anneal conditions.

Sample	Implant species and energy (keV)	Implant oxide (Å)	Depth range (Å)	Temperature (°C)	Inert annealing time (min)	Dry/wet/dry thermal oxidation time (min)
20k20m	B, 20	NA	720	900	NA	5/5/10
20k30m					10	
20k50m					30	
40k10m	B, 40	1000	1480		10	NA
40k90m					90	
40k30m					10	5/5/10
40k50m					30	

resistors, double shielded coaxial cables (RG-223/U), and BNC connectors, all automated using LABVIEW. The preamplifier input is set to ac coupling with bandpass filter lower and higher limits set, respectively, to 0.03 Hz and 300 kHz with ±6 dB/octave roll off. The output of the low-noise preamplifier (60 dB gain) is fed to the input of the spectrum analyzer. A Hanning window is selected to minimize power spectral density leakage. The overall power spectral density is obtained by overlapping the measurements of the different frequency spans of 800 fast Fourier transform (FFT) lines.

The piezoresistor noise voltage PSD is extracted by noise circuit analysis of the noise equivalent circuit which was validated using a 1 kΩ metal film resistor.[20] The noise voltage PSDs are characterized as a function of the implant conditions and annealing processes. Four point probe measurements are used for the noise measurement in order to minimize the effect of the contact resistance.

For each fabrication process listed in Table I, three noise voltage PSDs were measured from three different piezoresistors at the same bias voltage. The average and standard deviation of the three noise voltage PSDs of each fabrication process were then computed. The average noise voltage PSDs of the piezoresistors implanted at 20 keV and 40 keV followed by inert and oxidizing anneals are shown in Sec. IV. The cross-section transmission electron microscopy (XTEM) and plan-view transmission electron microscopy (PTEM) images are used to visualize and analyze the crystallographic defect number and dimensions in the samples. XTEM allows side views of the defects and thus their depth into the samples while PTEM allows a top view of the defects and therefore is used to compute the defect densities. The electrically active dose, Q, is obtained from Hall Effect measurement and is used in the computation of the number of carriers, N. An accurate carrier number is necessary for a correct extraction of the Hooge parameter α from the measured PSD.

IV. RESULTS AND ANALYSIS

The noise voltage PSDs of the boron implanted piezoresistors are measured as described above and the low frequency noise monitored as a function of anneal time at fixed anneal temperature (900 °C). Prior to the noise measurements, I-V characteristics of the piezoresistors are obtained. The Hooge parameter corresponding to each noise voltage PSD is obtained from Eq. (1) at 1 Hz using the empirical Hooge formula[13,14] of the $1/f$ noise.

$$\alpha = \frac{S_V N f}{V^2}. \tag{1}$$

The Hooge parameter is a figure of merit parameter that reflects the quality of the crystal.[13,21] Values of Hooge parameter α have been reported to vary between 1×10^{-3} and 1×10^{-7} for various processed wafers.[4,5,8,9,11] In the Secs. IV A–IV C, the measured noise voltage PSDs are reported as a function of implant and annealing conditions followed by analyses of the PSDs with respect to the bulk defect densities.

A. B, 20 keV implant followed by inert and oxidation anneals

The noise voltage PSDs are compared for the 20 keV boron implant for total anneal times of 20, 30, and 50 min, all other process conditions unchanged. The noise voltage PSDs are averaged on three separate devices for each process condition.

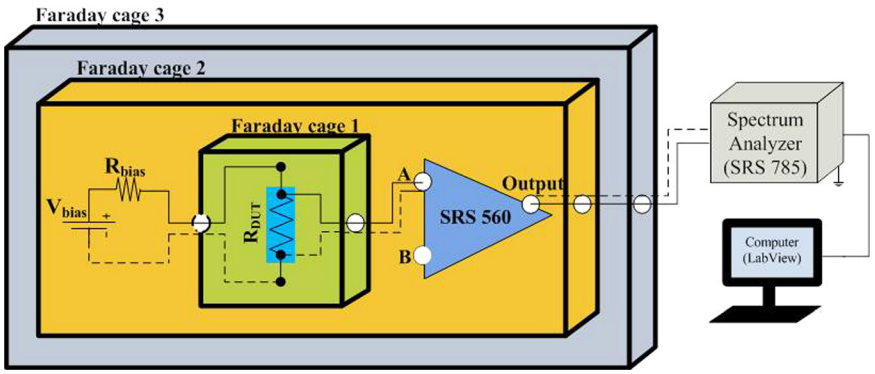

FIG. 1. Noise voltage measurement setup.

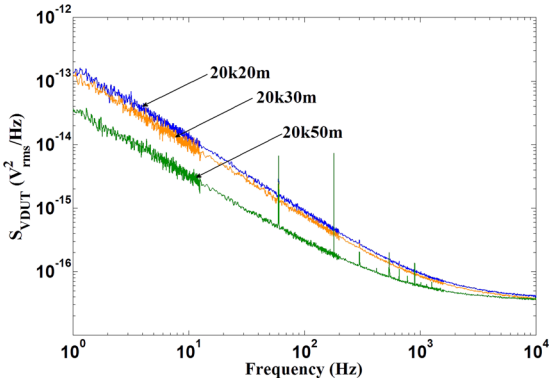

FIG. 2. Average noise voltage PSDs of piezoresistors implanted at 20 keV with total anneal times of 20, 30, and 50 min.

Figure 2 shows the noise voltage PSD as function of frequency for all piezoresistors biased at the same bias voltage of 3.3 V. The peaks in the PSD are 60 Hz power line harmonics. The nomenclature for each curve indicates the implant energy and the anneal duration, for example, 20k20m, refers to 20 keV implant energy and 20 min total anneal time at 900 °C. As seen in Fig. 2 for the 20 keV case, a decrease of the noise voltage PSD is observed as the annealing time increases. The slight variation in thermal noise is consistent with the variation in the measured DC resistance.

The Hooge parameter α for the 20 keV processes annealed for 20, 30, and 50 min extracted from the PSDs in Fig. 2 are, respectively, $(4.41 \pm 1.38) \times 10^{-4}$, $(3.42 \pm 1.17) \times 10^{-4}$, $(1.06 \pm 0.37) \times 10^{-5}$, a decrease of the Hooge parameter α as the annealing time increases.

To analyze the relation of the crystallographic defect densities on the electrical noise voltage PSDs and Hooge parameters, we use PTEM to visualize and compute the average defect densities for each process. The defect density is computed by taking PTEM images from ten samples of each process, counting the defects in each image and dividing by the area. Figure 3 shows the presence of dislocation loops in one such XTEM image and one such PTEM image obtained from the 20 keV boron implant and 30 min anneal process sample.

For annealing times of 20, 30, and 50 min, the bulk defect densities are $(6.82 \pm 0.71) \times 10^8\,\mathrm{cm}^{-2}$, $(5.89 \pm 0.82) \times 10^8\,\mathrm{cm}^{-2}$, and $(5.16 \pm 0.79) \times 10^8\,\mathrm{cm}^{-2}$, respectively, a decrease in defects densities as the annealing time increases. For all the 20 keV implanted samples, as the annealing time increases from 20 min to 30 min and to 50 min, the Hall mobility, the bulk defect density, and the measured $1/f$ noise PSD decrease; however, the percentage decrease in Hall mobility is much (order of magnitude) smaller than the decrease in the bulk defect density and the noise PSD. The voltage noise appears to track the defect density instead of the mobility. Next, the noise voltage PSDs, Hooge parameters, and defects densities of the piezoresistors implanted at 40 keV and subjected to inert anneal only are reported.

B. B, 40 keV implant followed by inert anneal only

The average noise voltage PSD is compared for B, 40 keV implanted samples through 0.1 μm implant oxide subjected to inert annealing only for times of 10 and 90 min at 900 °C. No subsequent oxidation is performed. The effect of electrically active defects is monitored via the measured $1/f$ noise voltage PSD of the piezoresistors. The results show a decreasing noise voltage PSD as the annealing time increases. The Hooge parameters α of the piezoresistors annealed for 10 and 90 min are $(9.67 \pm 4.13) \times 10^{-4}$ and $(4.94 \pm 1.73) \times 10^{-4}$, respectively. The PTEM shows dislocation loops with densities of $(9.09 \pm 1.44) \times 10^8\,\mathrm{cm}^{-2}$ and $(5.22 \pm 0.98) \times 10^8\,\mathrm{cm}^{-2}$ for the piezoresistors annealed for 10 and 90 min, respectively. The $1/f$ noise appears to track the defect density and not the mobility since the $1/f$ noise decreases although the Hall mobility slightly increases as the anneal time increases. The decrease of the noise voltage PSDs and the Hooge parameters α appear to be associated with the decrease in the defect densities as the anneal time is increased. The noise PSDs, Hooge parameters, and defect densities of the piezoresistors implanted at 40 keV and subjected to inert and oxidation anneals are discussed next.

C. B, 40 keV followed by inert and oxidation anneals

The average noise voltage PSD is compared for B, 40 keV implanted samples through 0.1 μm implant oxide subjected to both inert and oxidizing anneals for inert anneal times of 10 min and 30 min at 900 °C and thermal 5 min dry/5 min wet/10 min dry oxide growth. Figure 4 shows the noise voltage PSDs for the two different anneal times.

In contrast to the piezoresistors which are boron implanted at 20 keV on bare Si and subjected to both inert and oxidizing anneals and to the piezoresistors 40 keV boron implanted through 0.1 μm oxide subjected to only inert

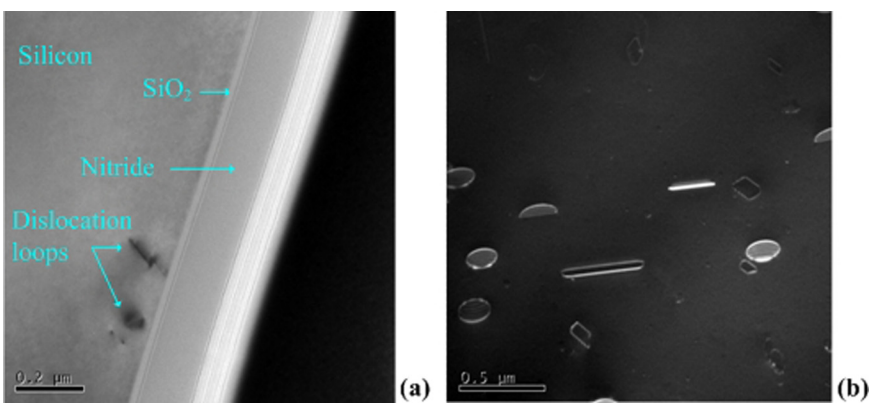

FIG. 3. (a) XTEM (0.2 μm scale) and (b) PTEM (0.5 μm scale) images of a piezoresistor implanted with B at 20 keV and annealed for 30 min.

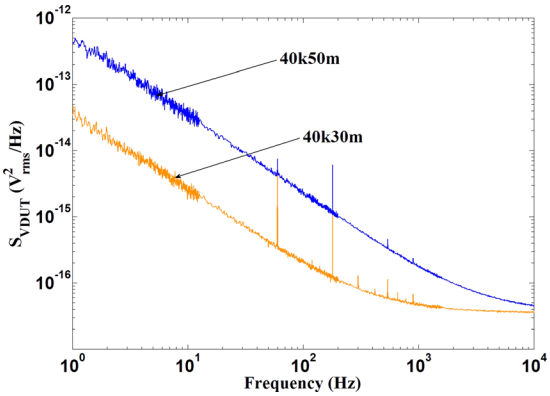

FIG. 4. Average noise voltage PSDs of piezoresistors implanted at 40 keV with total anneal (inert and oxidizing) times of 30 and 50 min.

annealing, the noise voltage PSDs of the piezoresistors implanted with 40 keV boron through 0.1 μm oxide and subjected to both inert and oxidizing anneals increase as the annealing time increases as shown in Fig. 4. As the annealing time increases, the Hall mobility slightly increases and the bulk defect density decreases. The Hooge parameters α are $(8.58 \pm 2.84) \times 10^{-5}$ and $(79.7 \pm 31.5) \times 10^{-5}$ but the PTEM defect densities are $(6.03 \pm 0.56) \times 10^{8}\,\mathrm{cm}^{-2}$ and $(4.55 \pm 0.77) \times 10^{8}\,\mathrm{cm}^{-2}$ for the piezoresistors annealed for 30 and 50 min, respectively, which are inconsistent with the tracking of the noise voltage PSDs with the PTEM defect densities. As shown, Figure 5 summarizes the interrelation of the Hooge parameter (noise voltage PSD), PTEM defect density, and total anneal time results for the three process conditions in a 3D plot.[22]

The 40 keV implanted piezoresistors through 0.1 μm implant oxide with inert and oxidizing anneals give unexpected results between Hooge parameter and PTEM defect density in Figs. 4 and 5. Unlike the 20 keV case and the 40 keV with inert anneal only, the PTEM defect densities decrease with increase in annealing time while the $1/f$ noise and Hooge parameters increase. To explore the inconsistency with the relatively simplistic PTEM defect density further, the faulted loop areas were investigated. Thus, the dimensions of the defects were measured including line length, the loop area, and the faulted loops areas. The measurements are

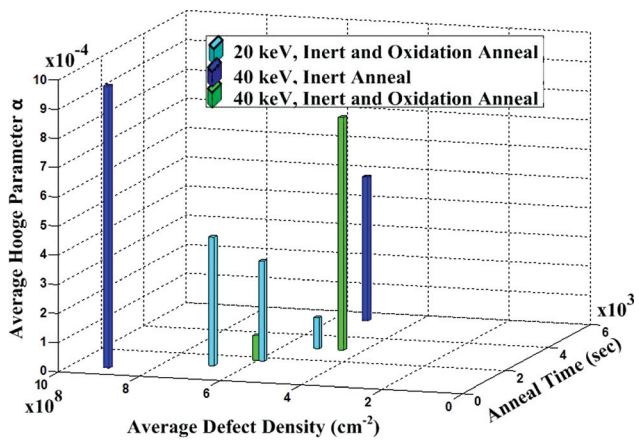

FIG. 5. Dependencies of Hooge parameter and TEM defect densities on implantation energy and anneal time.

conducted on only the readily observed loops. The line length is the total perimeter of the loops in three PTEM images. For the round loops, the perimeter is approximated by using πD for the non-surface terminated round defects, $(\pi D)/2$ for the surface terminated round defects, and $2l$ for the elongated defects where D is the longest axis for a round loop, and l is the length of the elongated defects. The loop area is the total area of the loops in three PTEM images. For the round loops, the area is approximated by using $\pi(D/2)^2$ for the non-surface terminated round defects and $[\pi(D/2)^2]/2$ for the surface terminated round defects. The elongated defects are not included in the loop area computation due to their small widths. The faulted loop area is the total area of the loops in three PTEM images for only the faulted non-surface terminated and surface terminated round defects. The equations used for the faulted loop areas are identical to those of the loop areas discussed above. Figure 6 shows the percentage change of the defect dimensions between 30 min and 50 min total anneal time. The inset in Fig. 6 is an example of a TEM image used in the computation of the defect dimensions.

The percent change in line length, loop area, and faulted loop area for the 20 keV and 40 keV boron implants with both inert and oxidizing anneals for total anneals of 30 and 50 min is analyzed. The percentage decrease of the line length between the 20 keV implant with 30 min anneal and the 20 keV implant with 50 min anneal is 6%. Also, the percentage decrease in the line length between the 40 keV implant with 30 min anneal and the 40 keV implant with 50 min anneal is 0.52%. Unlike the line length that decreased with increased annealing time, the loop areas and faulted loop areas increased with increased annealing time. However, the percentage increase of the loop areas and faulted loop areas for the 20 keV implant followed by 30 min and 50 min inert and oxidizing anneals are significantly smaller than the percentage increase of the loop areas and faulted loop areas of samples implanted at 40 keV and subjected to 30 min and 50 min inert and oxidizing anneals. The percentage increases of the loop areas and faulted loop areas for the

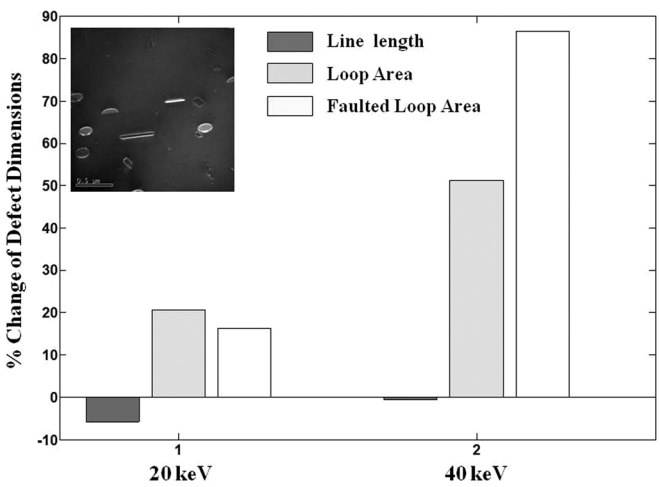

FIG. 6. Percentage change of defect dimensions between 30 min and 50 min anneals time for 20 keV and 40 keV implants with both inert and oxidizing anneals.

20 keV implant for 30 and 50 min anneals are 21% and 16%, respectively. For the 40 keV implant followed 30 and 50 min anneals, the percentage increases of the loop areas and faulted loop areas are 51% and 87%, respectively. The significant percentage increase in the faulted loop area appears to play a role in the increase of the magnitude of the $1/f$ noise of the 40 keV implant followed by increasing inert and oxidizing annealing time instead of the defect density and is indicative of the complex relationship between electrically active traps that participate in $1/f$ noise and the number and geometric (line, loop area, and faulted loop area) characteristics of defects in PTEM analysis.

V. CONCLUSIONS

It has been shown that longer annealing time helps decrease the defect densities but the decrease of the defect densities does not always correspond to a decrease of the noise voltage PSDs. For the 20 keV implant, it is shown that the $1/f$ noise PSDs decrease as the defect densities and the mobility decrease. While the Hall mobility also decreased, the percentage change was much smaller than that of the defect densities. For the 40 keV implant subjected to inert annealing only, it is shown that the $1/f$ noise PSDs decrease as the defect densities decrease while the mobilities slightly increase. Here, the $1/f$ noise appears to track the defect densities. However, this is not the case for the 40 keV implant followed by inert and oxidizing anneals where also the defect densities decrease and the mobilities slightly increase. The analysis of the XTEM and PTEM defect dimensions for the 20 keV implant shows that the line length of defects of the 20 keV implant samples followed by 30 and 50 min inert and oxidizing anneals decrease, while the percentage increases in the loop areas and faulted loops areas are not significant. This suggests that the decrease of $1/f$ noise of the 20 keV implants may be attributed to the overall decrease of bulk defect densities. For the 40 keV implant piezoresistors followed by inert and oxidation anneals, the noise voltage PSD and faulted loop areas both increase with increasing anneal time.

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