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# Pulsed-laser atom probe tomography of *p*-type field effect transistors on Si-on-insulator substrates

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Forty-five nanometer gate length *p*-type field effect transistors fabricated on Si-on-insulator substrates were analyzed using three-dimensional pulsed laser atom probe tomography. An optimized sample preparation methodology involving spacer etching and a change in sample orientation to align the Si/buried-SiO<sub>2</sub> interface with the analysis direction was developed to overcome the inherent difficulties in field evaporation of insulating materials present in the device structure. Atom probe tomography analysis of samples prepared in this cross-sectional orientation was used to observe B segregation to the gate SiO<sub>2</sub> at 5 nm from the edge of the gate, from both the poly-Si gate doping as well as the source–drain extension ion-implantation following rapid thermal annealing at 900 °C for 16 or 32 s. © 2011 American Vacuum Society. [DOI: 10.1116/1.3647879]

## I. INTRODUCTION

The ability of atom probe tomography (APT) to provide three-dimensional (3D) compositional mapping with sub-nanometer spatial resolution<sup>1–3</sup> suggests that it will be an important technique in the characterization of future generations of aggressively scaled and complex field effect transistors (FETs).<sup>4</sup> Traditionally limited to the analysis of metallic materials, recently developed pulsed-laser APT instruments have expanded the range of analyzable materials to include semiconductors and insulators<sup>5</sup> making it potentially capable of compositional analysis of modern FETs on Si-on-insulator (SOI) substrates. It can also potentially complement current two-dimensional characterization techniques, such as scanning spreading resistance microscopy, which uses local nanometer-scale electrical measurements developed from atomic-force microscopy,<sup>6</sup> but is capable of detecting only electrically active dopants.

However, even with the development of laser-assisted APT to allow analysis of insulating materials, APT of FETs on SOI substrates presents many challenges due to the presence of the SOI layer. Traditionally, APT analysis of layered structures has been performed in a “top-down” orientation,<sup>1,3,7–9</sup> where each layer is evaporated in series rather than in parallel, as shown in Fig. 1(a). If there is little variability in the evaporation field and thermal conductivity between the layers, performing top-down analysis is straightforward. However, when the variations are large, this can result in sample fracture at the transition from evaporating one layer to another in addition to analysis artifacts.<sup>10,11</sup> Here, a cross-sectional orientation method<sup>12</sup> for preparation of APT of *p*-FETs on SOI substrates is used where the FET is rotated 90° along the channel to situate the buried-SiO<sub>2</sub> layer along the length of the tip, as illustrated schematically in Fig. 1(b); this results in evaporation of the layers in parallel,

rather than in series. It is believed that this cross-sectional orientation aids in thermal dissipation of heat from the pulsed laser during analysis, and also removes the buried SiO<sub>2</sub> from the field of view of the local electrode. Using this geometry enables the exploration of a critical question in microelectronic processing, namely the lateral segregation of boron to the gate oxide. The goal of this paper is to use this unique geometry in APT to observe boron segregation to the gate oxide at various positions laterally in an SOI device after rapid thermal annealing (RTA).

## II. EXPERIMENT

Forty-five nanometer gate length *p*-FETs were fabricated on SOI wafers up through source/drain ion implantation and pulled prior to a RTA anneal and Ni silicidation. At 15 nm offset to the gate edge masked by thermal oxide spacer, the source/drain extensions were preamorphized using 40 keV Xe<sup>+</sup> implantation to a dose of  $5.0 \times 10^{13} \text{ cm}^{-2}$  followed by a B extension implant performed using BF<sub>2</sub><sup>+</sup> implantation at 3 keV to a dose of  $9.0 \times 10^{14} \text{ cm}^{-2}$ ; the deep source/drain B implant was done using BF<sub>2</sub><sup>+</sup> implantation at 9 keV to a dose of  $2.5 \times 10^{15} \text{ cm}^{-2}$  at 50 nm offset from the gate edge masked by the SiN<sub>x</sub> sidewall spacer. Due to the inherent

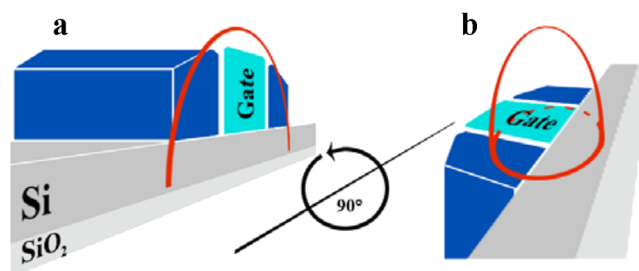


FIG. 1. (Color online) Schematic representation comparing two different methods of APT sample orientation of FETs on SOI substrates: (a) a traditional top-down analysis volume for an atom probe tip centered about the gate to (b) cross-sectional orientation.

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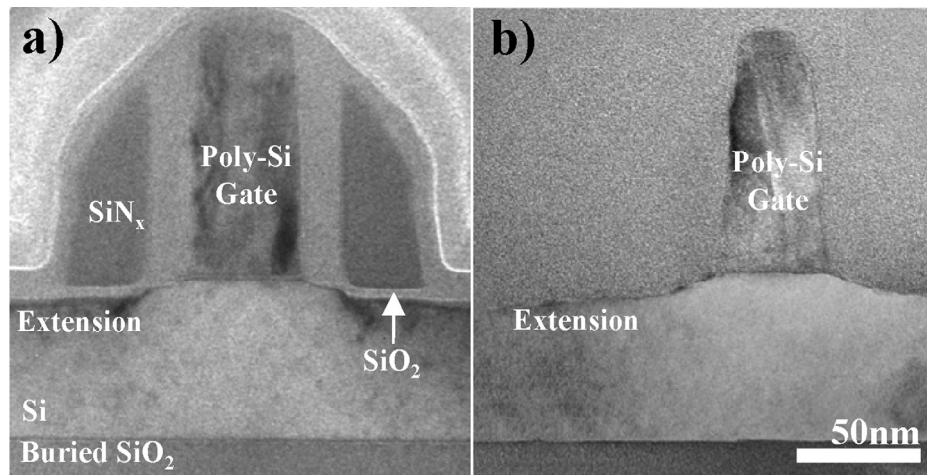


FIG. 2. XTEM micrograph of the *p*-FET structure used in this work: (a) the as-received structure and (b) the structure with  $\text{SiN}_x$  sidewall spacer and thermal  $\text{SiO}_2$  spacer removed after hot  $\text{H}_3\text{PO}_4$  and dilute HF etching.

difficulties in performing APT analysis of insulating materials, the  $\text{SiN}_x$  sidewall spacers were removed prior to APT sample preparation with a combination of etching in hot  $\text{H}_3\text{PO}_4$  (85% concentration at  $140^\circ\text{C}$  for 8 min) followed by etching with dilute HF (2% concentration for 20 s). Figure 2 shows cross-sectional transmission electron microscopy (XTEM) images of the device structure prior to and after the spacer etch treatment. Samples were then annealed using RTA at  $900^\circ\text{C}$  for 16 or 32 s to study B diffusion/segregation behavior. Prior to APT sample preparation, 300 nm of Si was deposited via plasma-enhanced chemical vapor deposition to allow conformal filling of the space between gate structures and provide a buffer material for focused ion beam (FIB) APT tip preparation.

APT samples in both top-down and cross-sectional orientation were fabricated using the traditional FIB lift-out method<sup>8</sup>; in the case of samples with cross-sectional orientation, a change in sample geometry was used: prior to mounting the wedge onto the microtip coupon array, the wedge was rotated  $90^\circ$  along its long axis placing the APT analysis direction orthogonal to the channel direction (parallel to the Si/buried- $\text{SiO}_2$  interface). This orientation allows the buried- $\text{SiO}_2$  layer to run down the side of the tip, and is thought to provide more area for thermal conduction from the pulsed

laser, compared to the traditional top-down orientation where a buried- $\text{SiO}_2$  layer effectively acts as a thermal sink during laser-assisted APT. Following rotation, a 50 nm layer of Ni was deposited on the wedge to protect against  $\text{Ga}^+$ -implantation from the ion beam, and the wedge attached to a microtip array for sectioning and sharpening using annular milling. This procedure is shown in the scanning electron microscopy (SEM) images presented in Fig. 3.

Specimens were analyzed using an Imago local electrode atom probe LEAP<sup>®</sup> 3000X-Si with a stage temperature of 60 K. A 532 nm green laser was used to aid in field evaporation of the specimen tip. The laser pulse frequency was set to 250 kHz with a pulse energy of 0.5 nJ, and the target evaporation rate was set to 0.2% of the laser pulse rate. Subsequent reconstructions of the data sets were performed using the Imago IVAS software suite; typical data sets consisted of  $8\text{--}10 \times 10^6$  ions.

### III. RESULTS AND DISCUSSION

3D APT analysis was attempted for both top-down and cross-sectional samples for as-implanted samples and samples annealed at  $900^\circ\text{C}$  for 16 and 32 s. However, because of specimen tip fracture during analysis, no successful data

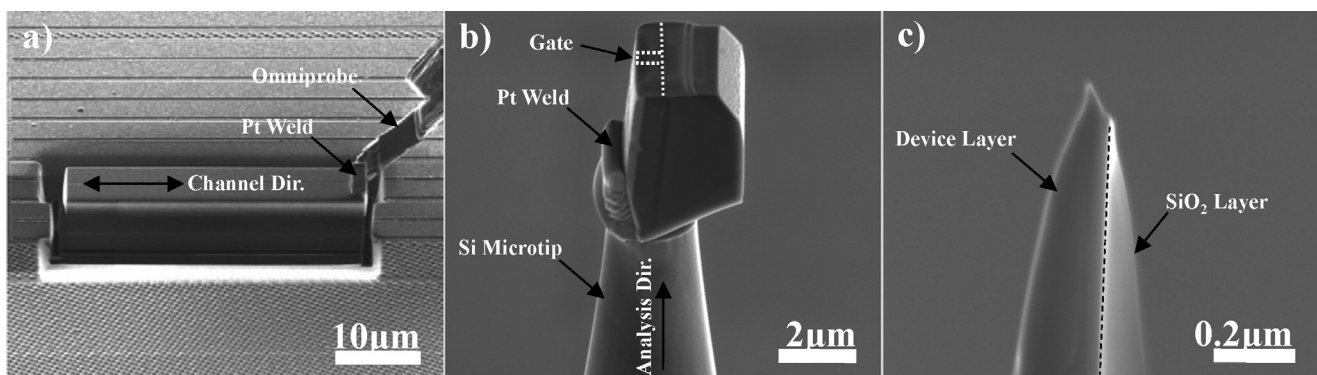


FIG. 3. SEM micrographs of APT sample preparation via FIB milling: (a) an in situ micromanipulator removes an ion-milled wedge from an array of *p*-FETs, (b) the wedge is rotated  $90^\circ$  about the long axis (so the analysis direction lies within the plane of the Si/buried- $\text{SiO}_2$  interface and is perpendicular to the channel direction) coated with  $\sim 50$  nm of Ni, and mounted/sectioned to a Si microtip, and (c) the tip is sharpened into final shape via annular milling.



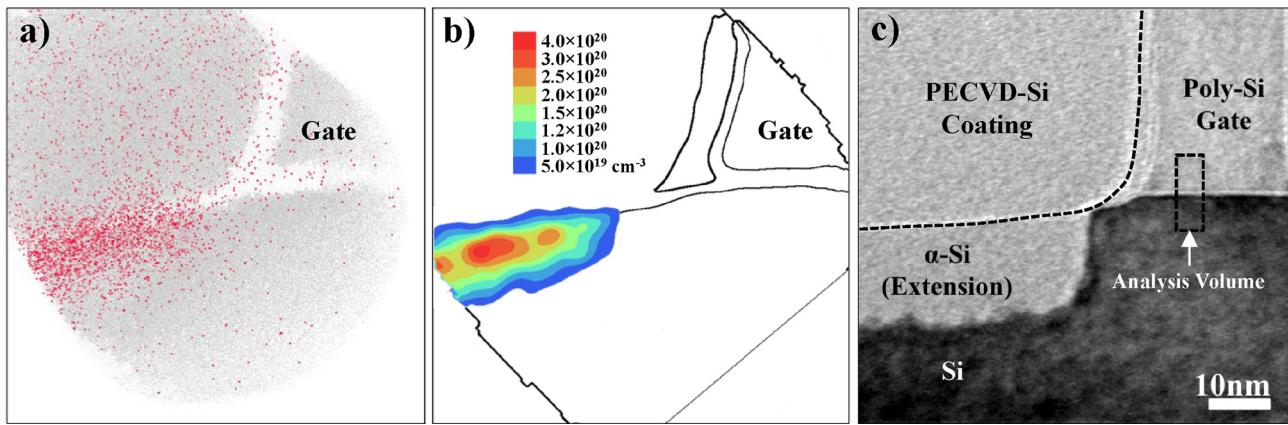


FIG. 4. (Color online) 3D reconstruction of as-implanted *p*-FET. (a) 3D analysis cone rotated to show the B extension implant (dark dots) left of the gate; 5% Si ions shown (light dots), (b) 2D contour plot showing concentration values for the B extension implant, and (c) XTEM micrograph from the same area of the device. An analysis volume outlines the location of the extracted 1D concentration profile.

from top-down samples were collected. This is indicative of the challenges associated with sequential field evaporation of layered structures containing insulating materials. Figure 4(a) presents a reconstructed volume of the gate edge region from an as-implanted cross-sectional APT sample displaying individual B atoms; an extracted two-dimensional B concentration contour plot is provided for comparison in Fig. 4(b) with an XTEM micrograph of the same region shown in Fig. 4(c). The two-dimensional contour plot was generated by assigning color values to concentration ranges within a  $1 \text{ nm} \times 1 \text{ nm}$  area.

A small analysis volume of  $5 \text{ nm} \times 10 \text{ nm} \times 20 \text{ nm}$  at  $5 \text{ nm}$  from the gate edge was extracted from the total device reconstruction to examine the segregation of B laterally to the gate  $\text{SiO}_2$ . The B concentration across the gate  $\text{SiO}_2$  in this region is plotted at  $0.5 \text{ nm}$  bin widths in Fig. 5 for differ-

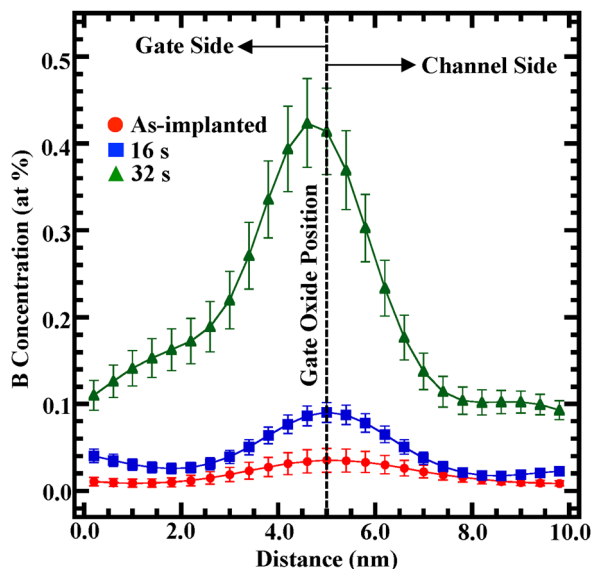


FIG. 5. (Color online) 1D B concentration profiles across the gate  $\text{SiO}_2$  region of *p*-FETs after annealing at  $900^\circ\text{C}$  as measured by APT: as-implanted ( $\bullet$ ), 16 s of annealing ( $\blacksquare$ ), and 32 s of annealing ( $\blacktriangle$ ); all concentration profiles were acquired at  $5 \text{ nm}$  from the gate edge. Error bars represent 1 standard deviation.

ent annealing times at  $900^\circ\text{C}$ ; accumulation of B at the gate  $\text{SiO}_2$  is clearly evident. The segregation coefficient of boron was calculated to be  $\sim 4$ , which is slightly below the reported values in the literature at the anneal temperature used.<sup>13,14</sup> Colby and Katz<sup>14</sup> report a segregation coefficient of 5.1, whereas Pfister *et al.*<sup>13</sup> estimate a value between 4 and 6 depending on the effective B diffusivity in the oxide. It is important to note that this segregation not only comes from the poly-Si gate doping, but the lateral diffusion from the source drain extension implant, which is observed here directly. This is evidenced by the increasing concentration seen in the channel region with increasing anneal time. It is difficult to determine the exact mechanism for B accumulation at the gate  $\text{SiO}_2$ . It may be the result of segregation to the oxidized surface in the implanted region followed by an enhanced lateral diffusion under the gate through the  $\text{SiO}_2$ .<sup>13</sup> It is also possible that because B diffuses by an interstitial-kickout mechanism,<sup>15</sup> and both the implant and anneal conditions are conducive for transient enhanced diffusion,<sup>16</sup> this segregation may occur if the B from the implant diffuses laterally in the silicon and subsequently follows the gradient of implantation induced interstitials up to the gate oxide. This has been proposed to explain the so-called reverse short channel effect.<sup>16,17</sup> Also, because  $\text{BF}_2^+$  is the implantation species, the incorporation of F from ion implantation has been shown to enhance gate oxide penetration,<sup>13,18,19</sup> the diffusivity of boron within the  $\text{SiO}_2$  has been shown to be further enhanced as thickness is reduced.<sup>18</sup> Prior APT work of blanket gate electrode poly-Si implanted with  $\text{B}^+$  instead of  $\text{BF}_2^+$  revealed B diffusing into the gate oxide,<sup>20</sup> but neither accumulation in, nor penetration through, the  $\text{SiO}_2$  was observed following annealing, suggesting that the presence of F is responsible for the results seen here.

This work shows that 3D APT data allows site-specific analysis from commercially processed devices on SOI wafers when the cross-sectional method is used. However, it is important to note that the analyzed volume in a 3D device reconstruction is  $\sim 10^6$  times smaller than the volume analyzed using conventional secondary ion mass spectrometry on a blanket SOI wafer; naturally, the dynamic range and

sensitivity will be reduced. However, an additional benefit of using a cross-sectional geometry is that with a sufficiently high ion count, the B concentration can be averaged through the width of the gate; therefore producing more accurate data. Nevertheless, there is a set maximum analysis volume before the tip widens to the point that the buried-SiO<sub>2</sub> layer is in the field of view; it is usually at this point that sample fracture was observed to occur in samples prepared in cross-sectional orientation.

#### IV. CONCLUSIONS

In this work, a cross-sectional method of atom probe tomography sample preparation was presented to allow analysis of field effect transistors on Si-on-insulator substrates. By using a cross-sectional orientation compared to the top-down approach, sample fracture was avoided and sufficiently large data sets were collected. It was demonstrated that performing atom probe tomography analysis of *p*-type field effect transistors on Si-on-insulator substrates in this orientation allowed for the effective study of lateral B diffusion and segregation to the gate SiO<sub>2</sub> following rapid thermal annealing at 900 °C.

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