DOPANT-DEFECT INTERACTIONS IN SI DOPED INGAAS

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To everyone who has ever encouraged me to seek, recognize, and profess the truth

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ALD	Atomic layer deposition
BJT	Bipolar junction transistor
CMOS	Complimentary metal oxide semiconductor
C_{ox}	Oxide capacitance
DIBL	Drain induced barrier lowering
EDS	Energy dispersive spectroscopy
EELS	Electron energy loss spectroscopy
EOR	End of range
EOT	Equivalent oxide thickness
FIB	Focused ion beam
Fin-FET	Fin field effect transistor
GaAs	Gallium arsenide
HBT	Heterojunction bipolar transistor
HR-TEM	High resolution transmission electron microscopy
III-V	Three-five
InAs	Indium arsenide
InGaAs	Indium gallium arsenide
LEC	Liquid encapsulated Chzochralski
LPE	Liquid Phase epitaxy
MBE	Molecular beam epitaxy
MOCVD	Metal-organic chemical vapor deposition
MOMBE	Metal-organic molecular beam epitaxy
MOSFET	Metal-oxide semiconductor field effect transistor

N_s	Sheet number
PA	Pre-amorphized
PECVD	Plasma enhanced chemical vapor deposition
PTEM	Plan-view transmission electron microscopy
RBS	Rutherford backscattering spectroscopy
R_p	Projected range
R_s	Sheet resistance
RTA	Rapid thermal anneal
SIMS	Secondary ion mass spectroscopy
SPEG	Solid phase epitaxial growth
SRIM	Stopping range of ion in matter
STEM	Scanning transmission electron microscopy
TEM	Transmission electron microscopy
UV	Ultra violet
V_d	Drain voltage
V_h	Hall voltage
V_{inj}	Injection velocity
WBDF	Weak-beam dark field
XRD	X-ray diffraction
XTEM	Cross sectional transmission electron microscopy

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III-V materials such as InGaAs and InAs may be good candidates for future, sub-10 nm nMOS devices as their high electron injection velocities result in improved on-state drive currents at reduced operating voltages relative to conventional Si channels. Many challenges to integrating III-V materials into future CMOS device exist but one common limitation to all III-V arsenides is the nearly two orders of magnitude lower active n-type doping concentration achievable in these materials relative to Si which poses a significant challenge for creating heavily doped source and drain regions required needed for low contact resistances in these devices.

Historically, Si has been one of the most promising ion-implanted dopant species for InGaAs given previous reports of limited diffusion and n-type activation levels up to 1×10^{19} cm^{-3}, but growth based doping techniques report maximum activation of 3×10^{19} - 6×10^{19} cm^{-3}. Previous explanations of the observed n-type doping limits in ion-implanted and growth doped InGaAs have been attributed to residual implant damage, amphoteric site selection of Si, limited chemical solubility or native point defects but these previous explanations are largely speculative. This work explores optimizing ion implantation conditions for maximizing the achievable Si doping concentrations in InGaAs as well as the evidence for some previous explanations for limited Si activation in both ion

implanted and growth doped InGaAs substrates. Experiments in this work show a common activation limit for both growth-doped and ion implanted Si after equilibrium thermal annealing, the ineffectiveness of co-doping, enhanced extended defect dissolution in heavily n-doped substrates and highly concentration dependent diffusion of Si. These findings indicate that Si doping at high concentrations is limited by changes in point defect populations of InGaAs and, in particular, cation vacancies rather than amphoteric site selection or chemical solubility of Si. Ion implantation and changes in the Fermi level are shown to be useful for modulating the population of point defects to control the diffusion and activation behavior of Si in ion implanted and growth-doped substrates.

CHAPTER 1
INTRODUCTION AND BACKGROUND

1.1 Plenty of Room at the Bottom

A little less than thirty years after the development of silicon transistors in 1954 an electrical engineering student went to talk to his advisor at a small state university in North Dakota about the course he was about to fail. Despite the student wanting to become an electrical engineer to work on radios and telephones, technologies that had existed for nearly a hundred years already, the advisor was clear that there was not enough room to keep poorly performing students who had seemingly little aptitude in coursework to become electrical engineers in the program. The student had taken some of the very first, courses in computer programming the university had offered, however, and managed to do quite well in the courses. The advisor had noticed the high marks in the computer programming courses and mentioned that the mathematic department was developing a new degree in “Computer Science” but the advisor did leave the student with one caveat before he decided to switch majors “I’m not sure if computers are going to amount to anything”. The rest is history as they say. That student was my father. He received his degree in computer science and has been working on computers in some capacity ever since. It seems almost laughable now to think that there was a time when computers were seemingly a novelty compared to the modern day when computers are often viewed as a necessity.

While it is true that initial computers and calculators often took up large rooms and could do little computationally than a freshman-engineering student supplied with log tables and slide rule, it is clear in hindsight that detractors lacked the imagination or optimism necessary to see how this technology could one day be an age-defining

breakthrough. In Richard Feynman's aptly titled 1959 lecture "There's plenty of room at the bottom" he illustrated quite clearly how the advent of miniaturization and "tiny machines" as he called it could one day revolutionize life, as we knew it despite having little inclination when he delivered the talk that these tiny machines would be the transistor[1]. In 1965, Gordon Moore, the future CEO of Intel, famously predicted that the number of transistors on a single chip would double every 2 years[2]. "Moore's Law", as this prediction is known, has been used as a benchmark to set performance targets in industry. This miniaturization has been used to great effect to increase the number of transistors on a single computer chip and at the same time reduce the cost of computing by orders of magnitude. Former Intel CEO Paul Otellini has made the case that the entire history of computing can be distilled in essence into one chart, which is recreated in Figure 1-1. While early computing involved relatively small numbers of public or private entities buying $10,000 dollar computers, by the time computers cost $1,000 the computer industry as a whole sold nearly 100,000,000 units. In the current era of mobile computing where units are now cellular phones, tablets, laptops, and, increasingly, "wearable's" billions to 10 of billions of units are sold with prices of $100-10. While initial versions of computers are available only to corporations and rich individuals or the top few percent of wage earners globally, $10 to $100 dollar computers have opened up the market to nearly 100% of the billions of wage owners globally.

1.2 III-V Materials for Digital Logic

Within the available semiconducting materials there are elemental semiconductors and compound semiconductors. Elemental semiconductors are composed of a single element such as Si or Ge but the alloying of Si with Ge results in

a compound semiconductor. Elemental semiconductors have a diamond-cubic structure, are covalently bonded, and are said to be sp^3 hybridized. In the sp^3 configuration, each atom shares its four electron with the neighboring four neighboring atoms resulting a stable octet of electrons.

III-V materials are necessarily compound semiconductors as they are formed with a one to one ratio of atoms from group III and V of the periodic table arranged in what is known as a zincblende (Figure 1-2) or in some cases, as with most III-V nitrides, Wurtzite, structure where the sharing of three electrons and five electrons making for a stable octet. The possibility of alloying differing amounts and species of group III and V elements results in a large number of engineering possibilities and result in a nearly limitless amount of III-V materials. III-V materials are also “direct-gap” materials meaning that the conduction band and valence band minima occur at the center of the Brillouin zone unlike elemental group IV semiconductors. Figure 1-3 shows a schematic E-k or “Band diagram” for both direct-gap and indirect gap materials where the kinetic energy of an electron as a function of wavevector (k) can be calculated assuming a parabolic band approximation as shown in Eq. (1-1)

$$E = \frac{\hbar^2 k^2}{2m_e} \tag{1-1}$$

High band gap III-V materials made form nitrides such as GaN are very useful in high-frequency, high-power RF devices due to the large bandgap (>3.0 eV) and high breakdown strength of many III-V nitrides. GaAs, InP and alloys of these compounds of have found much more use in optoelectronics as their band gaps are in the range of visible light (1-1.5 eV). III-V materials can be alloyed to nearly any band-gap energy

can be engineered making them extremely valuable in creating devices such as light emitting diodes, solar cells and optical sensors from the UV-infrared regions of the electromagnetic spectrum. The direct bandgap of these materials further improves the collection and emission efficiency of light as photon absorption/emission is not dependent on simultaneous photon/phonon excitation as is the case in indirect band-gap materials.

Generally, the electron mobility of III-V materials is much higher than that of Si. The mobility of carrier is determined in large part by the effective mass, m_e, which is proportional to the inverse of the second derivative of energy with respect to momentum as shown in Eq. (1-2). Bands with high curvature result in low electron effective masses.

$$m_e = \hbar^2 \left(\frac{\partial^2 E}{\partial k^2}\right)^{-1} \quad (1\text{-}2)$$

Mobility, shown in Eq. (1-3) is maximized when effective mass is minimized. Mobility in bulk materials also depends in large part on the number of scattering events that occur due to ionized impurity scattering or phonon scattering in the lattice.

$$\mu = \frac{e\tau}{m^*} \quad (1\text{-}3)$$

It is the high electron mobility and subsequent injection velocity of III-V materials, which make them especially appealing for integration into III-V logic devices for improved power scaling. Figure 1-5a-b shows a chart of electron mobility and relative permittivity as a function of band gap energies for common semiconductors.

The electron mobilities are generally much higher than the hole mobilities in most III-V materials. Ge has a much higher hole mobility and as a result, Ge is thought to be

a more suitable candidate for pMOS devices while III-V's are best suited for nMOS devices. Of the high mobility semiconductors, not all are necessarily suitable for creating n-channel CMOS devices. Another important consideration beyond the ultimate mobility is the actual band gap. InAs and InSb have very high electron mobilities but the band gaps of 0.45 and 0.17 eV respectively are likely too small for CMOS logic applications. The reasoning for this goes back again to actual device physics. Maintaining high I_{on} is important but the ratio of I_{on} to I_{off} determines how good a switch is. Off state leakage current is the current flowing through a device when the applied voltage is 0. One of the main contributors of leakage current in III-V materials is due to band-to-band tunneling in which carriers can tunnel from the conduction to the valence band due to thermal energy alone. Low band-gap materials have much higher band-to-band tunneling since there is less of a barrier to tunnel through as a result, most calculations and simulations seem to suggest that a band gap of at least 0.4 eV. $In_{0.7}Ga_{0.3}As$ is likely the channel material of choice given the band-gap constraints imposed by the off-state leakage current for a bulk device. Narrow band gap materials can be integrated as channel materials for very small feature sizes since quantum confinement effects can increase the effect band gap of these materials over the bulk materials.[3]

1.3 A Brief Introduction to MOSFET Devices

In general, semiconductor devices of all types are useful because they do not obey ohms law like a bulk material. Instead, transistors have non-linear current voltage or I-V characteristics, which are often referred to as rectifying. Ferdinand Braun first discovered this rectifying behavior in PbS in what is a naturally occurring mineral known as Galena.[4] The nonlinear I-V characteristics had been identified and employed before

the advent of Si and Ge based microelectronics with vacuum tubes and Schottky contacts but it wasn't until the advent of the point contact transistor and field effect transistor proposed by Shockley that semiconductor transistors started toward their current level of ubiquity.[5], [6] Figure 1-6 shows the I-V characteristics of ohmic devices, p-n junctions and a MOSFET. In semiconductor devices, the usefulness of rectifying behavior of a single transistor is extended as it can be arranged in circuits with other components and transistors to cause amplification or act as a switch. For digital electronics and in particular logic devices, this switching behavior is most important and is used to form logic gates that are the basis of modern computing.

The metal oxide semiconductor field effect transistor or MOSFET is not the most imaginative description of the device that billions of people now rely on everyday but it is very descriptive of the basic materials (metals, oxides, semiconductors) that go into the creation of these devices. There are multiple materials configurations and geometries suitable for the creation of switches but MOSFETS are the device of choice for computing due to the much lower static power consumption relative to other devices such as the BJT and JFET. The development of complimentary metal oxide semiconductors or CMOS was a further improvement in logic gate technology to reduce static power consumption.

Switching behavior in these devices is in many ways analogous to the switch controlling the overhead lights in a room or the knob controlling the water from a faucet. In the case of a hose there is some obstruction or valve preventing water from flowing from the water source such to the basin of a sink and down through the drain. When we modulate the degree of obstruction, the water is allowed to flow freely from the source

to and down the drain. Figure 1-7 shows the basic components of a MOSFET. In the case of a MOSFET, the carrier flow from the source to the drain is modulated by the application of voltage over the gate electrode. The applied voltage creates an electric field in the oxide layer that can then either deplete or accumulate the number of carriers in the channel. The depletion of carriers or “inversion” as it is called allows carriers to flow from the source to the drain much more freely. It is the ability to turn on and turn off carrier flow in a MOSFET device that constitutes the switching behavior.

Like all good switches it is desirable to create devices that are off when they are off and on when they are on. Just as leaky faucets are a problem as they can waste resources, leaky microelectronic switches are also a problem that can waste energy. Furthermore high performing switches allow high current flows. The analogy to water is used once again as faucets or showers with low current flow tend to be unsatisfying. Just as in plumbing so also in microelectronics. For this reason most improvements in CMOS and MOSFET devices target at three things: improving the current flow (I_{on}), reducing leakage (I_{off}), and limiting the amount of applied voltage required to change from I_{on} to I_{off} which is known and the subthreshold swing. One figure of merit for how well a transistor turn on and off is the I_{on} to I_{off} ratio. Good microelectronic devices have on/off ratios greater than 10^6 but this is not enough as the off state leakage current must also be low enough to prevent excessive off-state power consumption.

1.3.1 Increasing I_{on}

Perhaps the best way to begin thinking of a MOSFET is in terms of current as shown in Eq. (1-4). In a MOSFET, charge carriers moving at an electric field dependent velocity (v). in an inversion layer (Q_i) formed under the gate move from the source to

the drain in effect causing a current to flow through the thickness of inversion layer along the width of the gate (*W*) as shown in Eq. (1-4).

$$I_D = -WQ_i(x)v_d(x)\ . \tag{1-4}$$

For MOS devices, it is more useful to reformulate these equations with respect to the oxide capacitance and the applied biases to the gate and drain in the linear regime and the carrier mobility in the inversion layer, μ_{inv}, as shown in Eq. (1-5). In modern MOSFET devices where $V_{DS} \approx 1.0$V and channel lengths are less than 100nm the high electric fields across the channel result in electric field independent velocity saturation of carriers at $\approx 10^7$ cm/s due to scattering in the channel. The drain current in the saturated regime is given in Eq. (1-6)

$$I_{D-lin} = \frac{W}{L}\mu_{inv}C_{ox}(V_{GS} - V_T)V_{DS} \tag{1-5}$$

$$I_{D-sat} = W\ v_{sat}\ C_{ox}(V_{GS} - V_T) \tag{1-6}$$

Continued scaling of devices requires that channels and the actual amount of material for carrier to flow through become smaller and smaller and as a result the actual output current for a single device is continually decreasing. In order to improve on-state drive currents in single devices reduction of the equivalent oxide thickness (EOT) is used to increase the amount of carriers in the inversion layer. EOT has been reduced by using thinner dielectric layers but also by the introduction of high-k dielectrics as well to reduce current losses due to tunneling through the gate oxide. Device currents have also been improved by increasing carrier velocities. Uniaxial compressive strain has been used to increase carrier mobilities in pMOS devices by removing the degeneracy of the light and heavy-hole bands at the valence band

maximum but biaxial tensile strain yields much more modest increases in electron mobility in diamond cubic or zincblende structures prompting the move to materials with higher unstrained mobilities such as III-V's. For III-V materials the velocity at which carrier saturate is higher than that in Si, but this velocity is not orders of magnitude higher as is the case with the mobilities. As a result, even using materials with order of magnitude better bulk mobilities will not result in order of magnitude better output currents in short channel devices. For sub-10 nm devices, scattering of carriers in the channel can be avoided and devices operated high electric fields carrier transport can become ballistic-limited. In this case, v_{sat} is replaced by the thermal injection velocity v_T as show in in Eq. (1-7) where v_T is shown to depend heavily on effective mass and temperature as shown in Eq. (1-8) and as a result, ballistic-limited devices can have carrier velocities that are much higher than v_{sat}.

$$I_{D-sat} = W\, v_T\, C_{ox}(V_{GS} - V_T) \tag{1-7}$$

$$v_T = \sqrt{\frac{2k_bT}{\pi m^*}} \tag{1-8}$$

1.3.2 Decreasing I_{off}

Even when we turn a MOSFET "off" there is still a small amount of "leakage" current flowing between source and drain. When there are billions of devices on a single chip even a small amount of leakage in a device can end up being a big problem. If the two billion transistors in the Apple A8 each had off state currents of a seemingly reasonable 1 nA, the battery would be depleted in an hour just from static power consumption. At V_{gs} less than V_t there is a small amount of inverted carriers that result in a current flow from the source to the drain. Smaller threshold voltages will reduce the

amount of leakage for a given transistor but smaller V_t will also result in lower I_{on}. Instead, the approach taken by designed is to reduce the sub-threshold swing, S.

In an ideal MOSFET the sub-threshold slope is due to the thermal excitation of carriers over the barrier such that the sub-threshold slope, given in Eq. (1-9), approaches the ideal value of 60 mV/decade at room temperature. The relation of sub-threshold slope, S, to I_{off} is also shown graphically in Figure 1-8

$$S = 2.3\frac{k_b T}{q}\left(1 + \frac{C_{dep}}{C_{ox}}\right) \tag{1-9}$$

One way that the sub-threshold swing can be lowered in a non-ideal configuration is to increase the oxide capacitance or reduce the depletion capacitance in order to improve the gate control over the channel. Oxide capacitance was increased early on by using thinner and thinner gate oxides but eventually tunneling from the channel through the gate oxide becomes a problem when the oxide layers is less than 2 nm or so. In order to prevent tunneling though the gate oxide high-k dielectrics were introduces along with metal gates as the previously used poly-silicon gates suffered from depletion that reduced the oxide capacitance. The current generations for state of the art MOSFETS have employed finFET technology to effectively place more of the channel near the gate to further improve gate control over the channel. The current exploration of nanowire and 2-D channel materials is similarly aimed largely at reducing short channel effects in an effort to curtail the high leakage currents associated with small devices. Leakage in short channel devices was also exacerbated by a condition known as drain induced barrier lowering or DIBL. In DIBL the electrostatic coupling between the channel and the depletion from the applied drain voltage results in lower effective channel lengths making it easier for carriers to move from the source to the drain.

1.4 New Requirements for the Age of Mobile Computing: Power Constrained Scaling

While Moore's law is often cited as the rule for device shrinkage it was actually Dennard who first developed the scaling laws for CMOS device performance and power consumption scaling with decreasing feature size.[7] The ultimate limits of CMOS scaling are in large part determined by power consumption and it is easy to see why if one estimates the power consumption of a CMOS devices scaled to the theoretical limit. First, the Shannon-von Neumann Landauer minimum energy to switch a transistor at room temperature is calculated from the following equation.

$$E_m = \ln(2)\, k_b T = 0.017 \text{ eV}$$

Then use the Heisenberg uncertainty principle to determine the minimum transistor size

$$L_m = \frac{\hbar}{\sqrt{2 m_e E_m}} = 1.5 \text{ nm}$$

the number of devices that we can fit in one square cm can be calculated

$$n_{devices} = \frac{1}{{L_m}^2} = 4.7 \times 10^{13}/\text{cm}^2$$

as well as the minimum switching speed

$$\tau_m = \frac{\hbar}{E_m} = 0.4 \text{ ps}$$

the dissipated power can be calculated from the following formula

$$P_m = \frac{n_{devices} E_m}{\tau_m} = 3.7 \times 10^6 \text{ W/cm}^2$$

This is a phenomenal amount of heat flux. In fact, this is a higher radiosity than present at the surface of the sun (only about 6.5×10^3 W/cm^2). In reality, it would be impossible to reach that point since the amount of heating would cause the switching

behavior to fall apart completely and Si would be vaporized well before it could reach temperatures approaching the surface of the sun. Practical limits dictate that Si cannot dissipate more than 100 W/cm^2 without the requirement of active cooling and transistor densities and operating voltages and frequencies can now easily exceed the Si heat dissipation limit of 100 W/cm^2. The thermal dissipation limit of Si explains the stagnant clock speeds since the 90 nm node and the huge amount of cooling needed in data centers.

The new era of cheap, mobile computers requires the development of existing technologies to meet demands accordingly. Early generations of computing often had little in the way of power constraints other than the heat dissipation limit of Si but the age of mobile computing relies in large part on batteries with limited capacities that have not been fortunate the see the same order of magnitude technological improvements in capacity the last fifty years. On-State power dissipation in a single CMOS device can be shown to be proportional to the product of the frequency and capacity of a single device multiplied by the square of the operating voltage as shown in Eq. (1.9).

$$P_{dynamic} = fCV_{DD}^2 \tag{1-9}$$

$$P_{static} = I_{off}V_{DD} \tag{1-10}$$

$$P_{die} = fE_s n_{devices} \tag{1-11}$$

$$P_{die} = fCV_{DD}^2 n_{devices} \tag{1-12}$$

Power dissipation chips manufactured at the 90nm node and smaller have used reductions in V_{dd} to curtail power consumption and since 2005 there have been little

improvements in operating frequency with manufactures building “dual core” and “quad core” processors instead. Ultimate scaling of V_{dd} may be limited to a few tenths of a volt for CMOS device structures due to V_t roll off and noise.[8] Further miniaturization of devices and reductions in V_{dd} lead to a resultant decrease in actual on state drive current. Reductions in on-state drive current necessarily result in worse transistors, as the main goal of CMOS design is to preserve a high ratio of I_{on} to I_{off}. The switch to III-V materials is primarily motivated by the desire to maintain similar on-state drive currents to Si but at reduced operating voltages in effort to reduce the on-state power consumption or alternatively it may be possible to have higher on-state drive currents at the same V_{dd} for high power applications.

1.5 Integration Challenges for III-V Materials with Existing Si Technology

For CMOS applications, Si has been the material of choice for decades and rightly so. Si is one of the most abundant elements in the earth’s crust. Si is easy to refine and form into large boules and large >12’ diameter wafers which help scale microelectronics and reduce costs. It is easy to dope both n and p-type and has a phenomenal oxide layer that is strongly adhered to the Si crystal and results in relatively few dangling bonds compared to other crystalline materials. For these reasons, Si and in particular Si substrates will likely always be one of the dominant materials in microelectronic devices requiring any new materials such as III-V’s and even 2-D materials to be compatible with existing Si processing technologies. Early CMOS devices settled on Si because the native oxide formed by Si had a few major advantages over the native oxides formed on Ge and III-V materials. Native oxides on germanium are soluble in water, which made them incompatible with existing wet chemistry process in photolithography and etching steps. Similar problems with

thermally unstable native oxides III-V materials made CMOS devices poor choices until the advent of deposition techniques of better performing oxides.[9], [10] The development of better gate dielectrics and new deposition techniques has made it easier to make good performing devices on III-V materials but there are still other challenges related to III-V/dielectric interfaces that are being addressed.[11]-[14]

1.5.1 Growth-Related Defects

In the case of III-V growth on Si, there are a few major defects associated with the lattice mismatch and the chemical bonding in III-V materials. Homo-epitaxial growth of III-V materials generally results in low defect density, high-quality epitaxy but cost scaling requires that new materials be easily integrated onto wafers of Si that are easily made into 300 mm and larger wafers. Raw materials costs for bulk wafers prevent III-V materials from competing with Si in this case. The larger atomic radii and less covalent nature lend InGaAs and other III-V materials to larger lattice parameters than Si resulting in a lattice mismatch between the two layers. The layer thickness at which relaxation for a thin film occurs is known as the pseudomorphic thickness. As epitaxial layers increase in thickness, the stress in these layers also increases until the thin film undergoes relaxation. Below the pseudomorphic thickness, epitaxial layers are relatively free of stacking faults, twinning, and misfit dislocations. Above the pseudomorphic thickness, a large number of defects can be formed by the accommodation of film stress. The larger the lattice mismatches between materials, the smaller the pseudomorphic thickness. Direct growth of InGaAs and InAs on Si generally results in very defective epitaxial layers due to the large lattice mismatch. As a result, complicated buffer layer structures have been used to gradually reduce the strain over the thickness of a few microns to achieve relatively defect-free surface layers. More recent studies

have used aspect ratio trapping and selective epitaxy of faceted surface to further reduce defects in these heterogeneous structures.[15]-[17]

Defects themselves result in shorts and traps in completed devices both of which are deleterious to final device performance. The less covalent bonding and larger atomic radii also result in lower melting points such that Si and III-V processing must occur at substantially different temperatures. The differences in bonding in Si and III-V materials also results in growth related defects. In Si the bonding is perfectly covalent non-polar in contrast to GaAs and other III-V materials that have partially ionic behavior and form polar interfaces depending on whether surface are group III or group V terminated. One defect associated with this is the antiphase domain boundary in which an entire plane of Ga-Ga bonds exists instead of Ga-As bonds.[18] In all cases, growth-related defects are detrimental to derive performance as they can result in shorting between devices, which lower the transistor yield on a given die and act as carrier traps in devices.

1.5.2 Density of Interface Traps

GaAs has long been recognized as a potential nMOS material due to the higher electron mobilities, but Si has long been the dominant channel material in devices and much of this is due the excellent native oxide properties of Si. SiO_2 and is a wonderfully stable oxide that readily passivates dangling Si bonds. In the case of GaAs, native oxides do not passivate as many dangling bonds near the semiconductor-oxide interface. Furthermore, the native oxides in III-V materials are much less thermally stable and considerably more difficult to passivate. Dangling bonds and other defects at the oxide/semiconductor interface act as traps for carriers travelling from the source to the drain. This results in a higher density of interface traps along the inversion layer in

the channel that results in a degradation of on-state drive currents and leads to a higher sub-threshold slopes as well. A considerable amount of research into semiconductor dielectric interfaces as well as cleaning methods and surface treatments has been performed in recent years to improve the quality of the oxide-semiconductor interface.[19]

1.5.3 Density of States Bottleneck

Another fundamental limit of these materials is due in part to the nature of their high mobilities. With all materials there is a trade-off between the electron mobility and the density of states. In nm-scale devices and channels with equivalent oxide thicknesses less than 2 nm, quantum effects become a large part of device performance. The high mobilities in III-V materials are integral to lower density of states. The low density of states in these materials results in much lower quantum capacitance and the reduction in quantum capacitance results in a reduced number of carriers in the inversion layer and reduces on state drive currents in nm-sized devices. The lower quantum capacitance should allow for higher achievable switching speeds, but the gains in on state drive current from the improved ballistic injection velocity in III-V materials may be a improvement over Si even if the quantum capacitance is low.

1.5.4 Off-State Device Leakage

Sub-threshold leakage will be a problem in any nanometer-scale MOSFET device as detailed in section 1.3.2 but III-V materials also have additional leakage challenges not present in Si-based devices. Leakage due to band-to-band tunneling is likely to be the most significant source of off state device leakage for III-V channel materials as this effect is exacerbated in materials with narrower, direct band gaps. For this reason channel materials will require band gaps of 0.4 eV or higher. For bulk

devices it is unlikely that $In_xGa_{1-x}As$ compositions where x is greater than 0.7 can be used for this reason but for very small channel dimensions the actual band gap of a material will increase due to quantum effects such that higher In concentrations may be used for devices with feature sizes of a few nanometers. III-V materials also have a high dielectric permittivity that increases the electrostatic coupling between the drain and channel as well as higher D_{it} with the currently available gate dielectrics. Both of these properties will result in further deviations from the ideal values for *S* in devices with III-V channels.

1.5.5 Contact Resistivity

For micron scale devices, the bulk resistivity of the channel is the main component of resistance in a single MOSFET device but the aggressive gate length scaling in these materials, which will likely have ballistic carriers, have reached the point at which contact resistance is the dominant resistive term. It is necessary to reduce parasitic resistances and capacitances in order to improve operating frequencies but resistances also have deleterious effects on output currents.[20]-[24] Even resistances in the growing number of metallization layers now worry some engineers who are trying to continually scale electronic devices. Contact resistance problems are important in III-V materials and it will continue to remain important in aggressively scaled devices that rely on ballistic transport. This includes more recently developed 2-D materials like graphene, carbon nanotubes and even transition metal di-chalcogenides where it was found in ballistic devices such as carbon nanotubes the output drive currents were severely limited by contact resistance as determined from channel length independent output currents.[25]

In theory, the contact resistivity should be dependent on the barrier height resulting from the work function differences between the metal and semiconductor but in practice it is observed that contact metal work function has a limited effect over barrier height due to the phenomena known as Fermi level pinning.[26] As a result higher doping of the semiconductor material has more effect on lowering overall contact resistance than contact metal choice as shown in the equation below.[27] It is also seen from the equation that contact resistance will increase for materials with higher relative permittivity as is the case in most III-V materials but the lower effective mass also reduces the intrinsic contributions to contact resistance.

$$\rho_c = \rho_{c0}\, exp\left[\frac{2\phi_b}{\hbar}\left(\sqrt{\frac{m^*\varepsilon_s}{n}}\right)\right] \tag{1-13}$$

It is desirable to increase n to concentrations as high as possible and with Si, n-type doping density as high as 10^{20} or 10^{21} are regularly achieved. III-V Arsenides materials generally have order of magnitude lower dopant densities due in part to their limited density of states. For InGaAs, the highest reported active doping concentration is 8×10^{19} cm^{-3}. The conductivity of bulk III-V's is still much higher given that the bulk conductivity, σ, depends on the bulk carrier mobility, which is often one to two orders of magnitude higher than Si as shown in Eq. (1-14). Specific contact resistance is largely a tunneling or reflection phenomenon and shown to depend on the doping concentration and not on the bulk conductivity of a material given in the equation below. Reducing the contact resistance is important for realizing the benefits of higher on-state drive currents in devices made from III-V's.

$$\sigma = ne\mu_{bulk} \tag{1-14}$$

1.6 Stated Goals of This Research

A large amount of ongoing research is focused on addressing some of the previously mentioned challenges for integrating III-V materials into future generations of MOSFET devices but this study is focused towards understanding of Si doping of InGaAs at an atomic level. More specifically, this research is intended to develop a more complete understanding of the nature of point defects in InGaAs resulting from ion implantation and doping and the effect that different types of point defects have on the activation and diffusion behavior of n-type dopants in InGaAs. Better fundamental understanding of fundamental point defect behavior will be useful for informing engineering decisions related to integration and doping of InGaAs and related III-V materials in microelectronic devices to improve contact resistivity and accurately predict dopant activation and diffusion behavior.

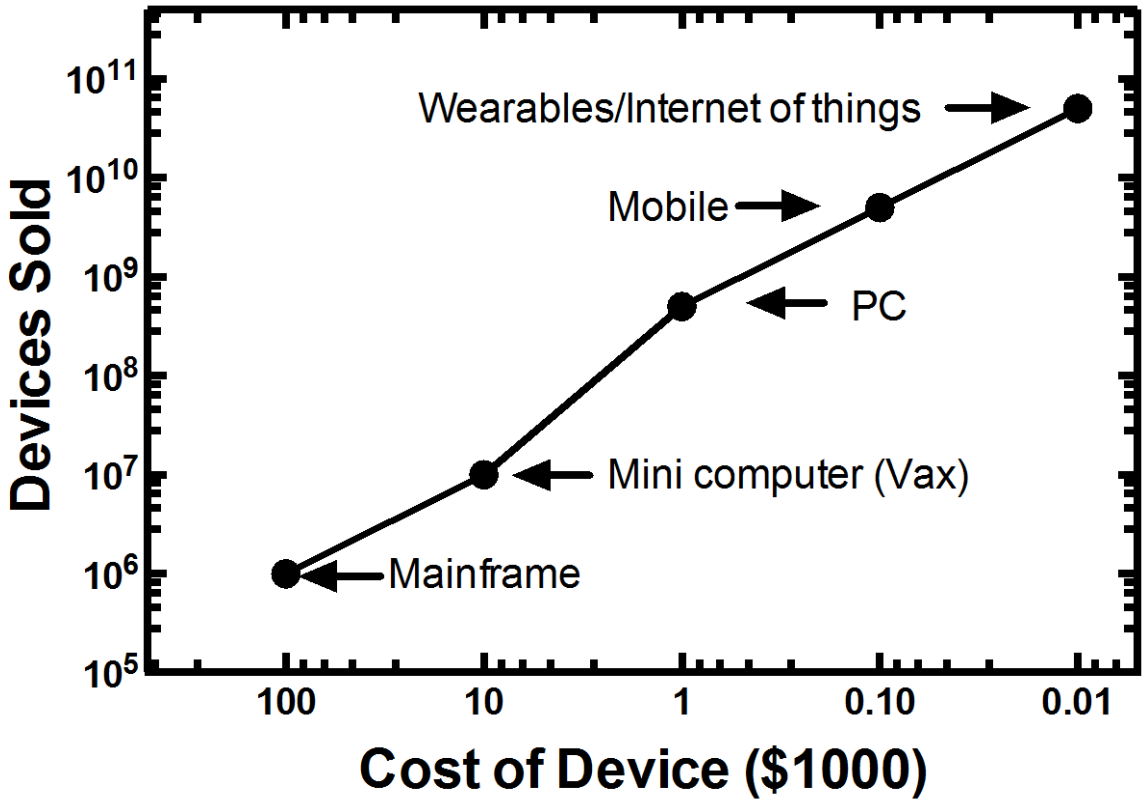

Figure 1-1. The history of computing in one chart. (from Paul Otellini)

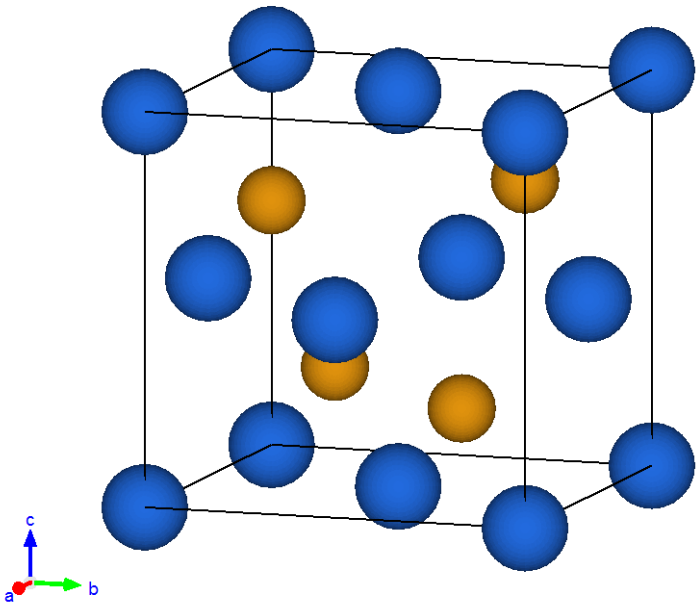

Figure 1-2. Model of GaAs structure with Ga atoms in blue and As atoms in orange.

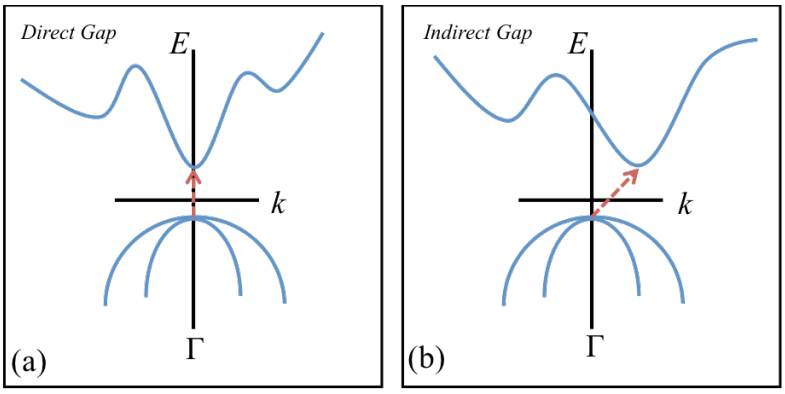

Figure 1-3. Energy band diagrams of two types of semiconductors. The diagram highlights the difference in conduction band and valence band alignments for (a) direct gap and (b) indirect gap semiconductors.

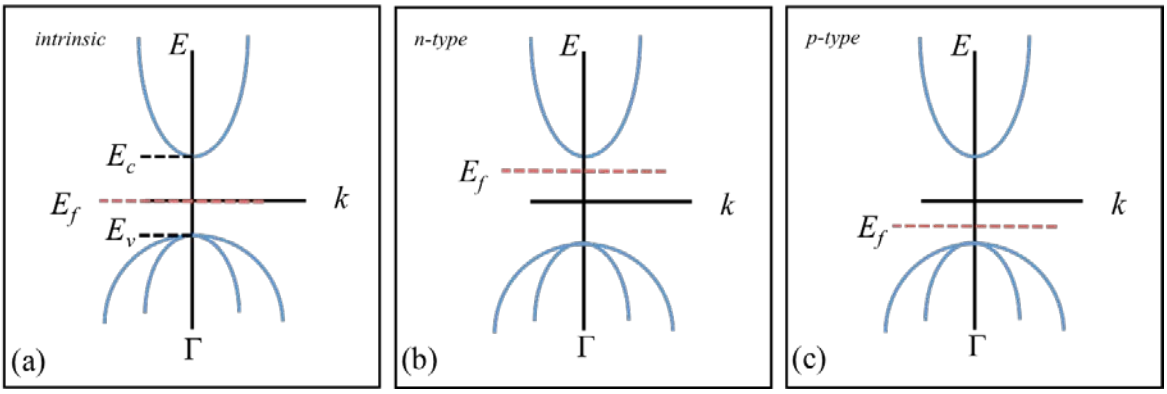

Figure 1-4. Schematic diagram showing the Fermi level relative to the valance and conduction band edge. Diagrams correspond to (a) intrinsic or un-doped (b) n-type and (c) p-type semiconductors.

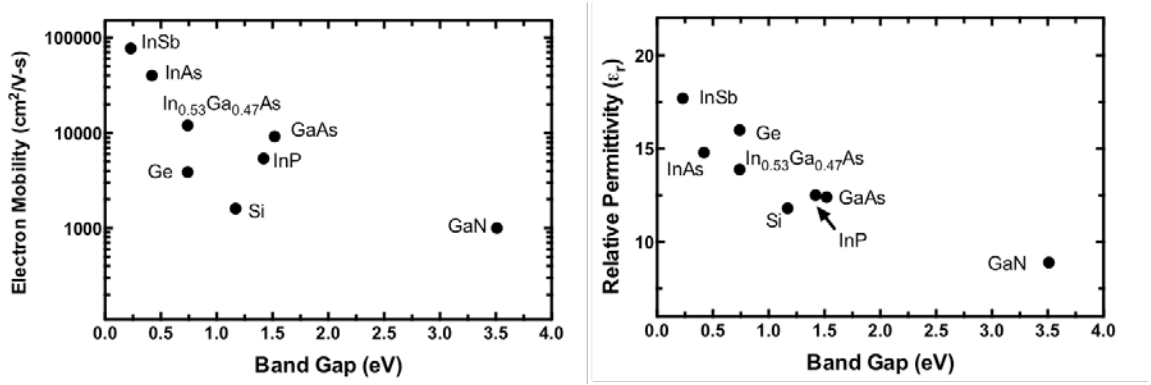

Figure 1-5. Plot of electron mobility and dielectric permittivity as a function of band gap energy. Relative permittivity and mobility both decrease with increasing bandgap.

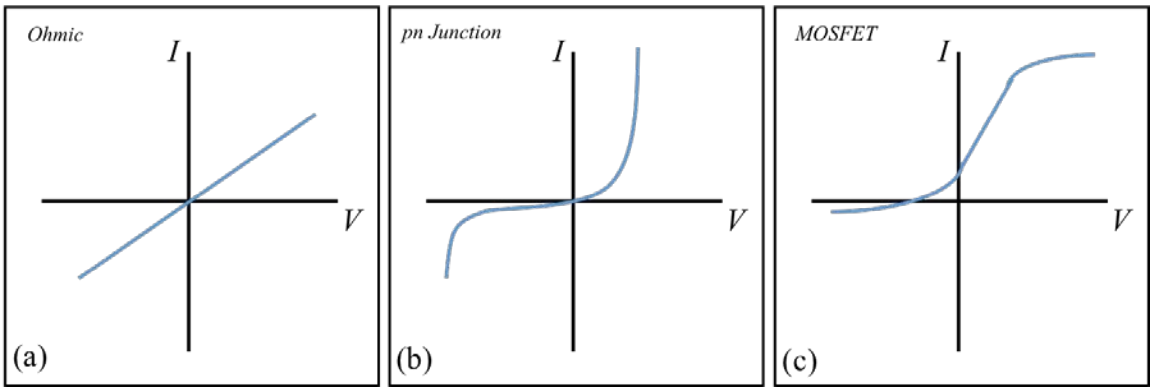

Figure 1-6. I-V curves for various devices. Schematic diagram showing (a) ohmic behavior, and rectifying behavior for a (b) pn-junction diode and (c) MOSFET

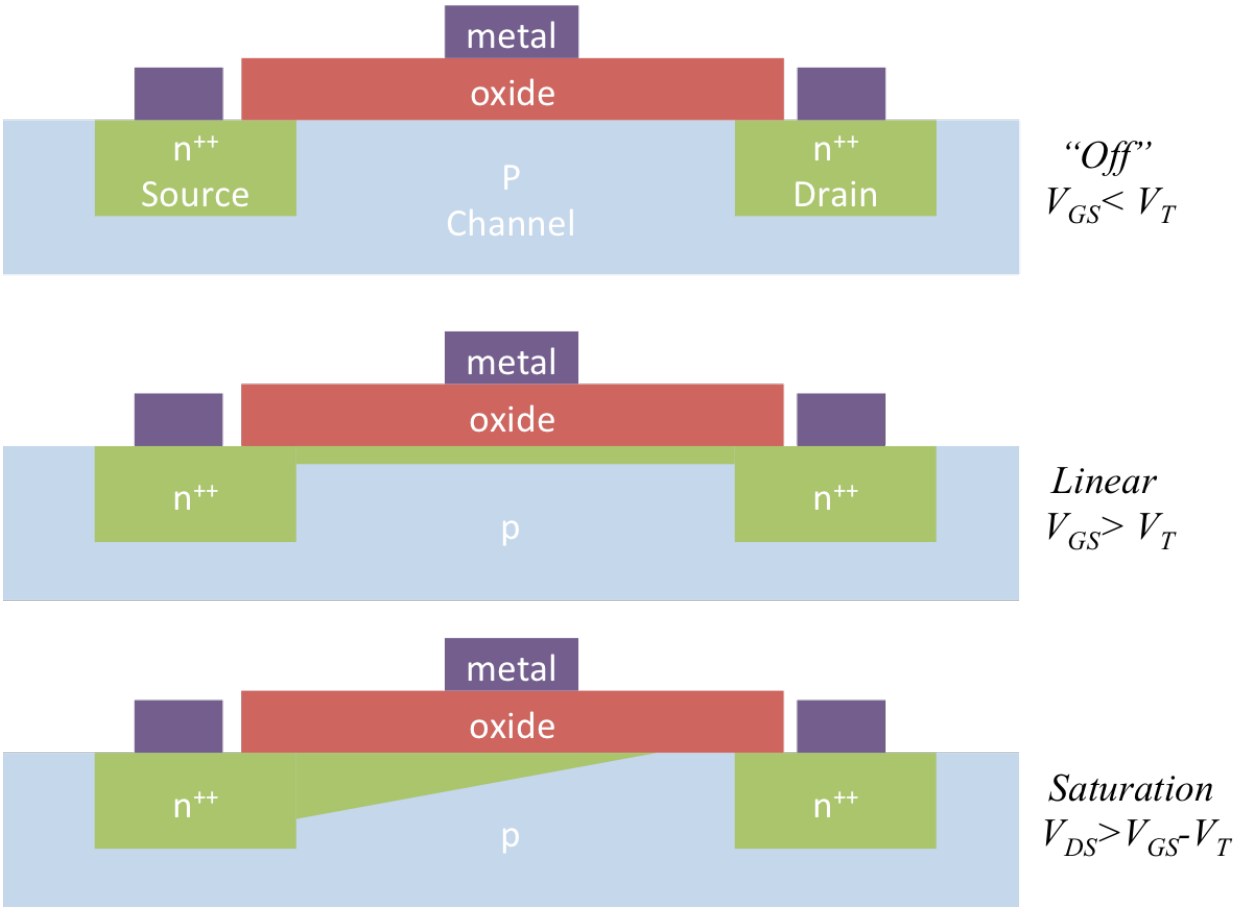

Figure 1-7. Schematic diagram showing the channel inversion of a MOSFET. Inversion is shown for the (a) "off" state, (b) linear and (c) saturation regimes.

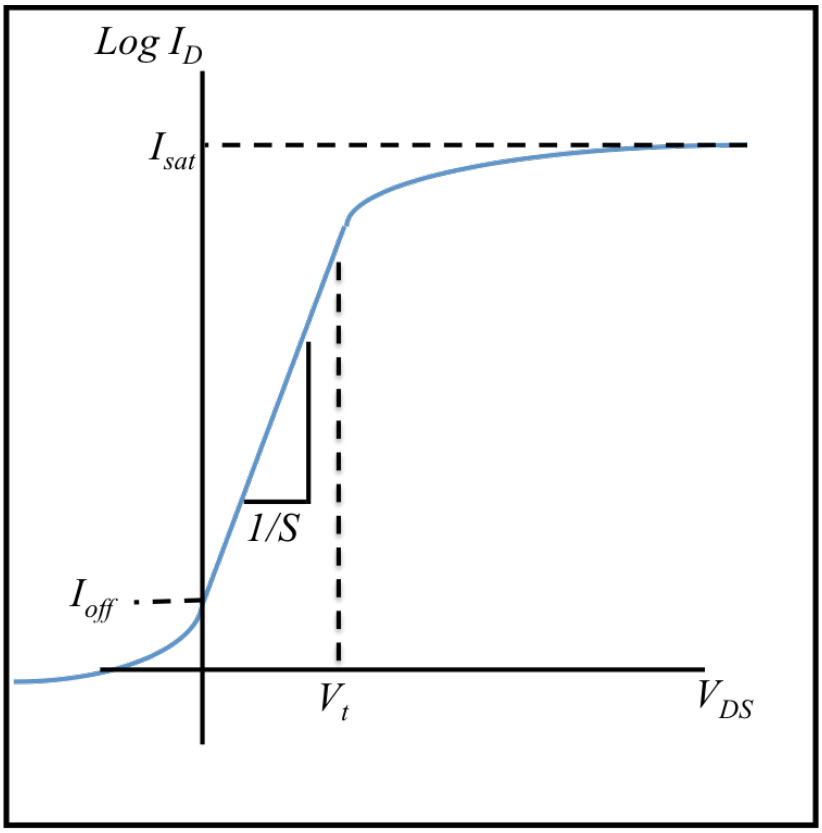

Figure 1-8. Schematic diagram showing the current behavior of a MOSFET as a function of drain voltage.

CHAPTER 2
DEFECTS AND DOPING IN III-V ARSENIDES

2.1 The Powerful Idea in Semiconductors

Two major properties make semiconductors useful for device creation. The ability of a semiconductor to support an internal electrical field and the ability to modulate the charge carrier concentrations with the addition of imperfections. Metals are defined as materials with a Fermi surface. As a result of this Fermi surface, metals have no ability support internal electric fields whereas materials with band gaps which are more commonly referred to as semiconductors or insulators do have this unique ability as their Fermi energies lie in this “band gap” and as a result these materials support an internal electric field. Of the materials with band gaps not all of them are easily utilized in the formations of microelectronic devices that rely on the presence of minority and majority carriers required to make functional devices which rely on the transport of carriers from one region to another.

Large band gap insulators such SiO_2, perovskites, and transparent conducting oxides such as $InSnO_x$ (ITO) are widely used in devices for their dielectric properties and ability to be transparent conductors respectively but most oxide materials generally exhibit only n-type conduction behavior[28]. Semiconductors that are useful for microelectronic device fabrication have further requirements beyond a band gap that make them good materials for microelectronic device. One requirement is that they can be doped both n and p-type and another is that ideally, the doping range in these materials can be controlled from ranges of parts per hundred to parts per billion to or in terms of atomic concentration 10^{12}-10^{21} cm^{-3}. It is precisely for these previously stated

reasons that Si, Ge and III-V materials have achieved their current level of ubiquity in modern microelectronic devices.

In recent years a large amount of research has been directed towards carbon based microelectronics but the lack of a bandgap in graphene and difficulty in controlling n or p-type conductivity in carbon based microelectronics[29], [30] has prompted investigation of newer 2-D materials such as transition metal di-chalcogenides (TMDC).[31]-[33] TMDC's have distinct band gaps but effective doping techniques in TMDC's are still in their infancy relative to Si and III-V materials.[34], [35]

2.2 Defects in III-V Arsenides

Multiple classes of deviations from perfect crystallinity or "defects" exist and they are broadly characterized by their dimensionality with the most useful defects in semiconductors belonging to zero-dimensional point defects and one-dimensional line defects as well as two dimensional area defects. Much like humans, semiconductors and materials in general are made interesting by their imperfections. The ability to control the electrical or ionic conduction in most materials is due to the presence of point defects. Dislocations and the movement of dislocations are largely responsible for the ductile nature of metals in and the inability to move dislocations in many ceramics and glasses results in the propensity for ceramics and glasses to shatter. It is from this microscopic understanding of imperfections in solids that an understanding of macroscopic observations in everyday life such as the shattering of windshields and the bending of bumpers in a car crash and why some diamonds cost more than others can be formed. In a similar fashion, these microscopic defects are the result in the observed current-voltage behavior of microelectronic devices.

2.2.1 Point Defects (0-D)

Point defects are of two varieties. Native point defects are intrinsic to the host material and impurities are point defects that are foreign to the host material. A large number of both type of point defects exist in most materials and both are exceptionally important in semiconductor devices.

2.2.1.1 Native point defects

The equilibrium number of native defects is proportional to the energy of forming a given defect and the temperature of a crystal as shown in the equation below.

$$N_{defects} \propto N\ exp\left(\frac{-E_d}{kT}\right) \quad (2\text{-}1)$$

At any temperature above 0K there will be an equilibrium number of point defects proportional to the energy to form a given defect. There are four main types of native point defect in elemental semiconductors. Interstitial defects occur when excess atoms inhabit an interstitial site. Vacancy defects result from the absence of atoms. Schottky defects are the result of a coupled interstitial and vacancy and Frenkel pairs result where a host atom becomes interstitial and leaves a vacancy. In III-V semiconductors, there exists the same four types of defects but they can exist for both the group III and group V sublattice doubling the number of possible types of native point defects. In addition to the defects that are common to elemental and compound semiconductors, compound semiconductors also exhibit a unique type of point defect know as anti-site defects.

The anti-site defects can occur when a group III species such as Ga result in p-type carrier generation when group III atoms occupy group V sites. The occupation of

group III sites by group V atoms could similarly result in n-type carrier. This doping configuration is more commonly referred to as an anti-site defect. From the above equation it can be inferred that defect formations with the lowest energy form will dominate at a given temperature. Vacancy defects generally have lower formation energies than interstitials and anti-site defects have the highest formation energies in compound semiconductors. Figure 2-1 shows a schematic of some of the possible native point defects that form in III-V Arsenides. Phenomena such as diffusion, oxidation, and grain growth and sintering all rely on vacancies and interstitials and complex interactions between point defects to transport atoms through solids.[36]

2.2.1.2 Impurities

Chemical deviations from perfect crystallinity offer opportunities to control the number and type of point defects in semiconductor crystals. Early attempts to fabricate microelectronic devices from Si, Ge and other III-V materials were often fraught with wildly different device performances. New crystal growth and impurity refinement methods were developed to further reduce the background impurity profiles in semiconducting materials, leading to results that are more consistent for individual experimenters and allowing precise doping control over semiconductors. Semiconducting materials with congruent melting temperatures such as Si and GaAs are much easier to refine and create bulk high purity materials whereas high purity ternary semiconductors such as InGaAs that have incongruent melting temperatures must be formed by non-equilibrium deposition techniques such as MBE and MOCVD.[37] For both of these growth techniques carbon and hydrogen incorporation from the precursors used to form the materials can significantly alter the material and device properties.[38], [39]

Doping in elemental semiconductors requires that aliovalent impurity atoms be integrated onto lattice sites in the semiconductor crystal. Introduction of isovalent chemical impurities will not cause large changes in electrical behavior since no hole or electrons can be generated with the satisfied octet. In the case of Si the introduction of impurity atoms with fewer than 4 valence electrons such as B and Al results in holes or p-type conducting behavior. The introduction of impurity atoms such as P and As with greater than 4 valence electrons results in n-type carriers. For III-V materials the number of doping configurations is much more varied. Aliovalent group II and VI impurities such as Be and S will result in holes and electrons when added to III-V materials. Dopants from Group IV such as Si and C are known as amphoteric dopants since they can occupy either group III or group V sites but in practice most amphoteric dopants prefer to occupy one sublattice or the other for a given material. Perfectly amphoteric dopants would result in no net change in n or p-type conduction. Si is predominately a donor in InAs and GaAs but carbon is more amphoteric in that carbon results in generally n-type behavior in InAs and generally p-type behavior in GaAs.

Chemical impurities or dopants are often further classified into shallow level impurities and deep level impurities. Deep level impurities are often used to create semi-insulating materials, as the carrier type of these impurities is dependent on the location of the Fermi level relative to the impurity level in the band gap. Shallow level impurities are either n-type or p-type depending on whether they are close to the valance (p-type) or conduction (n-type) bands. While deep level impurities typically have ionization energies around 0.5 eV, shallow impurities in Si typically require energies of 25 meV or less to cause either electron or hole delocalization in the bulk and the higher

relative permittivity of III-V materials often results in lower dopant ionization energies than in Si as shown in Eq. (2-1). The ionization energies required for shallow level dopants in Si and most III-V's are easily obtained at room temperature. For shallow level dopants in Si it is often possible to freeze out carriers at liquid nitrogen temperatures and the concentration at which the carrier concentrations freeze out regime turns into the full slope freeze out from half slope freeze out can be used to estimate the acceptor concentration. Determination of the background acceptor concentration in the narrow band gap III-V's is complicated by the increased dielectric constant of many III-V and InGaAs and InAs such that liquid He temperatures are necessary to freeze out shallow level impurities.

$$E_{binding} = \frac{m_e{}^* e^4}{8\varepsilon_r{}^2 \varepsilon_0{}^2 h^2} \tag{2-1}$$

2.2.2 Line Defects (1-D)

The agglomeration and assembly of a large number of point defects leads to the formation of extended or (1-D) defects. In semiconductors, these defects are often observed due to imperfect growth caused by lattice strains during heteroepitaxy (misfit or threading dislocation). Line defects are generally undesirable in semiconductor devices because they often cause shorting between devices or act as traps for carriers. These types of defects are often present in GaN grown on sapphire, [111] Si and SiC substrates where they act as optical traps and the reduction of these defects can greatly improve the optical efficiency of light emitting diodes and the DC characteristics of transistors made from GaN.[40], [41]

2.2.3 Area Defects (2-D)

2-D Growth related defects, such as stacking faults and anti-phase domain boundaries, are planar in nature and often occur during heteroepitaxial growth. 2-D defects are also frequently observed upon solid phase regrowth of III-V materials where heavily damaged material that has become amorphous returns to crystallinity. The agglomeration of 0-D interstitial and vacancy defects can also take the form of self-enclosed loops consisting of excess or missing planes of atoms. Loop defects in semiconductors are often the result of radiation damage and are discussed in more detail in subsequent sections. 2-D defects are deleterious to device performance for the same reasons mentioned for line defects and they can also affect carrier mobility in highly defective substrates due to phonon scattering. Surfaces and interfaces between materials play a very important role in most microelectronic devices and these interfaces can be thought of as 2-D defects. In Si, the presence of an amorphous native oxide passivates many of the dangling bonds but in III-V materials the native oxides are less adept at passivation and the resultant defective surface leads to interface traps, which indeed trap carriers as they move along the surface of the material. Interface traps are concerning in field effect transistors as the majority of charge carriers travel near the surface. The junction of metals with semiconductors also leads to Fermi-level pinning, which has been proposed by some to be the result of defects created by contact of metals with the semiconductor surface.[26]

2.2.4 Volume Defects (3-D)

Volume defects such as inclusions are relatively rare in semiconductors due to their low background impurity concentrations in semiconductors but high dose inert gas implants can result in voiding or bubbling. This is used to great effect in the manufacture

of SOI or XOI with SmartCut. High dose implantations can introduce volume defects into Ge and the antimonides and this effect has been used to form nanostructured anodes of Ge for use in Li-ion batteries. In general, volume defects are easily avoided and of limited technological importance in a individual microelectronic device but the existence of such defects are mentioned here for the sake of completeness.

2.3 Doping in Semiconductors

Doping is the most useful defect in semiconductors and is often controlled from parts per billion or less in concentration to parts per hundred or more making them the primary means of controlling the behavior of semiconductor devices. Multiple species and methods for doping semiconductor materials exist and brief overview of dopant or impurity incorporation methods and practical considerations is provided here with regards to doping in III-V semiconductor systems and the group III-arsenides in particular.

2.4 Methods of Dopant Incorporation

Many techniques have been developed to precisely control the number of dopants that are introduced into a crystal all of which have specific advantages and disadvantages, which may make one technique more suited than other depending on the applications. Practical considerations limit the possibility of using certain doping depending on whether a semiconductor is a binary or ternary semiconductor. Some exotic forms of doping have been developed but only diffusion, growth-doping and ion implantation are discussed since these make up the majority of doping processes in industry and literature.

2.4.1 Bulk Doping

Bulk doping is performed during growth of the semiconductor boule by introducing impurity atoms directly into the melt. For most Si devices a lightly p-doped substrate is used and further functionalized by the addition of subsequent processing steps. This bulk doping can be performed during CZ growth as well as with Bridgeman and LPE growth that is more common in the production of III-V boules. Liquid phase growth of III-V materials is strictly limited to systems to that have congruent melting points in order to maintain stoichiometry in a given phase and as result MOCVD or MBE processes must be used to grow many ternary compounds including InGaAs.[37]

2.4.2 Source Diffusion of Dopants

One of the first methods of dopant incorporation employed by the semiconductor industry was source diffusion. With this technique, the semiconductor was annealed in the presence of a solid or gas dopant source and the thermal annealing was sufficient to drive the dopant from the surface into the bulk.[42], [43] This method has limited usefulness in III-V semiconductors due to their propensity to undergo component evaporation and surface degradation. However, monolayer doping is a more modern take this previously used technology.[44], [45]

In monolayer doping a source dopant is introduced onto the surface at a temperature low enough that surface degradation is not an issue but also usually so low that dopants are unable to diffuse into the bulk. Once the surface is saturated with the desired dopant, a dielectric cap that prevents surface decomposition is deposited and the entire sample is annealed at elevated temperatures such that the surface dopants are driven in to the bulk.[46] The resulting process is still limited by the equilibrium diffusion of dopants into the bulk, but heavily doped and highly abrupt junction, have

been formed with this method. Monolayer doping may be a interesting method for forming abrupt, heavily doped junctions in future devices where the 3-D topography may prevent conformal doping with methods such as ion implantation.

2.4.3 Thin-Film Growth Doping

Both molecular beam epitaxy and chemical vapor epitaxy use the vapor phase of a semiconductor constituent to grown the material in a layer-by-layer fashion. The layer-by-layer growth allows for the creation of a wide array of heterostructures with this technique as well as the formation of compounds that cannot be formed by equilibrium thermal processing.[47], [48] The growth of these films is often performed at temperatures much lower than required for dopant diffusion and much less than the melting temperature of the material being deposited. MBE and CVD have another benefit over other techniques in that the non-equilibrium nature of the process can allow incorporation of dopants well over the chemical solubility in some cases. Historically, the highest measured doping concentration in III-V materials come from MBE grown films.[49], [50]

Chemical vapor epitaxy or chemical vapor deposition has the benefit of being a high throughput process but the metal organic precursor used often result in film that have large amounts of excess carbon which can be a problem if carbon acts a dopant in the grown material. MBE can be performed from high purity solid sources as well as metallorganics. MBE requires much higher vacuum (10^{-8} Torr) than MOCVD and has lower throughput, which make is less ideal for large-scale fabrication, but it has the advantage of having lower background impurities especially when high purity solid sources are used. More recent reports of Te and Sn doping in InGaAs via MOCVD provide evidence of very high achievable doping concentrations.[51], [52]

Growth doping of source and drains in MOSFET devices is increasingly done in Si-based microelectronics. In the case of p-FET devices the source and drains are regrown using SiGe instead of Si. The addition of Ge which has a larger lattice parameter materials induces a uniaxial compressive strain in the channel regions which further improves the carrier mobility in p-FET devices and has the additional benefit that the incorporation of B is increased with increasing Ge content.[53]

2.4.4 Ion Implantation

Like MBE and MOCVD, ion implantation is a far from equilibrium process but similarity between this and other doping methods stops there. Extensive overviews of the ion implant process in Si and III-V materials exist in the literature and the reader is recommended to consult these resources.[54]-[58] Because the focus of this dissertation is directed towards the investigation of implanted Si dopants and implantation damage, a more thorough treatment of ion implantation will be undertaken relative to the other doping methodologies.

2.4.4.1 Process overview

In ion implantation, dopant atoms are ionized and accelerated through an electric field before being separated in a magnet and crashing into the target substrate. The chemical purity of ion implantation can be controlled to a very high degree by separating magnets, which make use of the Lorentz force to filter out only species with the proper mass to charge ratio. The depth and location of the chemical impurities is controlled by the accelerating energy. To a first order approximation assuming a Gaussian distribution, the implanted ion concentration as a function of depth, (x), can be modeled as shown in the following equation. Where Φ_D is the implanted dose, and R_p and ΔR_p

are the projected range and the straggle of the distribution. Example profiles of implanted B in Si as a function of dose and energy are shown in Figure 2-2.

$$C(x) = \frac{\phi_D}{\sqrt{2\pi}\Delta R_p} exp\left[\frac{-(x-R_p)^2}{2(\Delta R_p)^2}\right] \quad (2\text{-}2)$$

The peak concentration for a implant is controlled by increasing or decreasing the number of ions (dose) the target material is bombarded with by increasing or decreasing the implantation time or beam current. Real implant profiles generally have more skewness and kurtosis to their distributions due to the more complex interaction of the nucleus and electrons of implanted ions with solids as well as ion channeling and amorphous layer creation. Pearson IV distributions are also commonly used to generate analytical approximations of implanted ion distributions in amorphous materials.[59] Monte Carlo methods such as crystal-TRIM[60] and UT-MARLOWE[61] are also used to generate simulated implant profiles in crystalline material that can account for channeling, tilt angles and ion dose and energy dependent changes in the properties of implanted materials.

2.4.4.2 Radiation damage in crystalline materials

The ion implantation process is quite violent in that many of the host atoms become displaced when incident atoms are accelerated into the host crystal.[62]-[65] Ions travelling at a large fraction of the speed of light enter the host lattice where the incident ion begins to interact with the host lattice. For energies above 100 keV most interactions occur between the incident ion and the electron cloud of the constituent target atoms. This is known as electronic stopping and is modeled as an inelastic collision. Once inelastic collisions have reduced the kinetic energy of the incident ions

significantly, the incident ions begin to react more strongly with the nuclei of the target atoms as shown in Figure 2-3.

$$-\frac{dE}{dx} = N(S_n(E) + S_e(E)) \quad (2\text{-}3)$$

This interaction is elastic in nature and causes displacement of the host atoms. These displaced host atoms can further displace other host atoms in the “collision cascade”. This process continues until the energy of the incident ion is dissipated into the target material by either nuclear or electronic stopping as indicated in Eq 2-2. The majority of these displaced atoms can move back onto lattice sites and do not result in damage (dynamic annealing) but a fraction of these displaced atoms become stuck in interstices and result in vacancies. The introduction of excess impurity atoms introduces further interstitials and is said to be non-conservative. With very large amounts of incorporated impurity atoms or “high doses” the number of point defects can increase until the crystalline substrate becomes amorphous. Figure 2-4 shows the net interstitial and vacancy profiles as wall as the Ga ion profile for 100 keV Ga implant into InGaAs showing the dissociation of point defects in the irradiated solid with vacancy rich regions near the surface and interstitial rich regions deeper into the bulk. Both implant energy and dose have a large degree of control over the placement and magnitude of damage in an irradiated crystal for a given implant species into a host material. Interatomic bond strength also has a role limiting damage and substrates with high bond strengths such as diamond and AlN are not readily amorphized irrespective of implant species unlike more weakly bound materials such as GaAs and InP which are readily amorphized.[66]

The ability of a solid to anneal damage occurring from implantation during the implantation is known as dynamic annealing. The ability of a material to undergo

dynamic annealing is dependent on the thermal conductivity of the material but also the ability of the material to quickly re-order interatomic bonds. The threshold amorphization dose for III-V materials is usually lower than that for elemental semiconductors due to the more complex bonding arrangement, and in fact, some ternary alloys such as InGaAs amorphize more readily than their binary constituents, GaAs and InAs due to differences in bond lengths.[67]-[70] Dynamic annealing can be further reduced by cooling the implanted material and radiation damage is shown to accumulate much faster in materials as they are cooled to lower fractions of their respective melting temperatures.[69], [71]-[73]

Radiation damage in solids can be either n-type or p-type in nature. Proton irradiation studies of InAs showed that radiation damage causes pinning of a defect level in the conduction band[74], [75] but radiation damage in most other solids results in defect levels that are inside the band gap.[74], [76], [77] As a result, these defects may result in either n or p-type compensation depending on the initial Fermi level in the implanted solid. The radiation damage in GaAs and InGaAs formed in the bandgap has been shown to compensate donors in these materials. Because of this, it is desirable to reduce radiation damage in these materials if high levels of n-type doping are to be achieved. Conversely, radiation damage in these materials may help improve the activation of p-type dopants in these materials and explain why p-type dopants generally activate at lower temperatures than n-type dopants in III-V materials.[78]

2.4.4.3 Post-implant electrical activation

Ion implant is also different from the previous mentioned doping techniques as the incorporated dopant atoms are not yet active. In order for a dopant to become active, it must occupy a lattice site and have sufficient thermal energy to ionize the

dopant or acceptor. Annealing after implantation is required to give the dopant atoms enough energy to diffuse onto lattice sites and recover damage due to implantation. During this diffusion process other point defect often coalesce and extended defects as in the case of loops formed by the excess interstitials.[79], [80] In the case of amorphization, dopants in the amorphized region are incorporated onto lattice sites when the amorphous layer is regrown. Regrowth of amorphous layers occurs at temperatures much less than the melting point and at temperature much less than required to diffuse the implanted dopants.[81]-[84]

2.4.4.4 Self-alignment

Historically the biggest advantage of ion implant over other doping techniques in the creation of devices over other techniques is self-alignment. When forming source and drains and well as source drain extension in CMOS devices, the gate dielectric, photoresist, metallization or other layers can serve as a mask to protect the channel regions from being doped while maintaining excellent composition and spatial control of the introduced dopants. This advantage is important enough that the disadvantages of extra annealing steps and increased thermal budgets required with implant processes are tolerated.

2.5 Thermal Treatment of III-V Semiconductors

The thermal treatment of III-V semiconductors is much more complicated than elemental semiconductors for essentially one reason: III-V materials tend to decompose from group V loss at the surface at the temperatures required to activate implanted dopants.[85]-[91] The magnitude of surface degradation is dependent on the temperature and time at which the material is being annealed. The subsequent component evaporation can lead to deviations in stoichiometry at surfaces and even

macroscopic degradation evidenced by haze and discolorations on the once specular surface well before melting.[86], [92], [93] In some materials with high melting temperatures, like the nitrides, this problem is lessened, but in group III arsenides and especially in group III phosphides, component evaporation upon annealing is a serious problem that must be addressed if functional devices are to be made.

2.5.1 Strategies for Preventing Surface Degradation

Multiple strategies have been employed in the thermal processing of III-V materials in order to prevent or lessen the degree of surface degradation. Early experimenters generally used proximity caps or annealing in As rich ambients.[2], [72], [90], [91], [94]-[97] Both of these methods work in a similar fashion. In the proximity cap method, a wafer of the same or a different material is placed on top of the semiconductor to be annealed. During annealing the “proximity” of the capping wafer prevents arsenic from moving into the atmosphere immediately and in theory raises the arsenic overpressure near the surface of the wafer limiting or preventing severe surface degradation. Annealing in a As rich ambient can be performed by annealing in the presence of AsH_3 gas but other experiments were able to anneal in excess group V ambient by annealing sample in closed quartz ampoules where excess As or P or III-V powders had been placed. In both of these methods, higher group V partial pressure prevents or limits the continued evaporation of the group V element from the surface.

The most common method for more recent experiments is to replace the proximity cap with thin film encapsulation.[58], [87], [98]-[102] Thin film encapsulation improves upon As rich ambient and proximity caps and is usually much more stable at high temperatures. In the proximity cap method, the intimate coverage of the cap with the surface does a better job at maintaining high As overpressures inside the

encapsulated region and further prevents out diffusion of the group V species. Silicon oxides and nitrides as well as silicon oxynitrides, silicate glasses and aluminum oxides have been tested as dielectric caps. While nearly any film can be used, practical considerations dictate that the best encapsulating films can be removed by methods which do not cause degradation to the underlying substrate, are composed of species that do no interact with the films at elevated annealing temperatures, and the films can be deposited at temperatures that avoid surface degradation that are easily removed by selective etching and have good uniformity. Films that meet these requirements tend to be the best performers. Perhaps the best annealing film right now is formed by atomic layer deposition of Al_2O_3. These films are readily removed by selective etching in HF of BOE, have excellent uniformity and coverage, and the high degree of thickness control allows very thin films that can better accommodate stresses during annealing from mismatches in thermal expansion. It is these stresses that tend to generate cracks and pinholes in films which then act as pathways for out diffusion.[100]

2.5.2 Annealing Methods

Furnace annealing is the most popular method in literature to perform annealing but current VLSI processing generally seeks to limit any diffusion of incorporated dopants past what is required to achieve the modeled device performance. The total time and temperature experience by a device or wafer is often referred to as the "thermal budget". Great efforts are undertaken to reduce the temperatures and time that current devices are subjected to during the annealing processes and many new thermal processing methods have been developed to limit the thermal budget.

Rapid thermal annealing was one of the first methods used to achieve reduced thermal budgets. In rapid thermal annealing halogen lamps are generally used to induce

ramp rates of hundreds of °C per second. Flash rapid thermal processing uses a similar technique where the wafer is raised quickly to an intermediate temperature before being exposed by a flash lamp that heats the sample a further 400-600°C degrees over a time of a few ms. Laser annealing is also often performed and has the advantage of being able to have very high energy densities over a very limited amounts of time.[103]-[106] Both laser annealing and flash RTP have the added advantage of being surface sensitive and do not result in equilibrium thermal annealing, as is the case in furnace annealing and halogen lamp RTA. Other methods such as microwave annealing and graphite strip thermal annealing have been used in laboratory setting to induce different annealing conditions but these methods are generally not prevalent in high volume production.[107]

With respect to ion implantation, annealing methods are useful if they can efficiently recover implant damage or give dopants enough thermal energy to promote the desired amount of diffusion or incorporation on the lattice. Short anneal times and further from equilibrium processing methods are in fashion in modern devices since very abrupt junctions are generally required and as a result most annealing methods for implanted material seek to minimize diffusion while maximizing activation. Dopant selection becomes very important in this case since proper dopant selection can further reduce the diffusion that occurs during activation or back-end thermal processing.

2.6 Dopant Selection in GaAs, InGaAs and InAs

Dopant selection is decided in large part by the desired application and device structure. For future CMOS devices high concentration acceptor doping of III-V's is of limited interest as Ge is a much more suitable pMOS material.[108] Many different n-type dopants exist for III-V systems but all dopants have unique behaviors. Dopant

selection can be further limited by the method of dopant incorporation and perhaps most importantly by the diffusion and activation characteristics of a given dopant species. In the case of ion implantation the diffusivity of particular dopants can be increased or diminished by implant damage and the propensity of a implant to amorphize the substrate is increased with increasing ion mass. Lighter ions are also generally preferred for ion implantation in order to reduce implant damage and avoiding amorphization in III-V materials is especially important since these materials have poor regrowth behavior.

2.6.1 Acceptor Dopants

A large number of dopants have been successfully used in III-V arsenides. Transition metals such as Zn, Mg, Cd, and Hg have all been used to form p-type arsenides but these dopants are less than ideal for most microelectronics applications as the high diffusivity of these dopants is not suitable for creating the shallow, abrupt junctions needed in modern microelectronic devices.[109]-[118] Other transition metal dopants such as Fe and Cr have been shown to create deep levels in these materials that turn the substrates into semi insulating substrates, which are useful for isolating active layers. Be is by far the most commonly implanted p-type dopant but the small Be atoms prefer interstitial diffusion mechanisms and it has a very high diffusivity because of this.[110], [115], [119]-[126]

2.6.2 Donor Dopants

Group VI dopants have also been extensively studied in these materials with S, Se, and Te all showing n-type behavior.[72], [85], [98], [127]-[139] S shows faster diffusion relative to the amphoteric dopants.[140], [141] Group VI dopants are also generally heavier than group IV dopants and result in higher amounts of implanted

damage and result in amorphization at lower implanted doses. Dopant activation of heavier species is generally less than that of lighter species in ion implantation. This result is usually attributed to the increased damage occurring from heavy ion bombardment relative to lighter ions. S and Se generally show higher electrical activation than Te for cases of ion implantation but some reports of Se dopants in InGaAs report activations that are similar to Si and the more commonly used amphoteric dopants in the III-V arsenide systems.

2.6.3 Amphoteric Dopants

C, Si, Sn and Ge are all group IV species known as amphoteric dopants in III-V systems. Amphoteric dopants deviate from common acceptor and donor species in that they can behave as donors or acceptors in depending on which sublattice these dopants occupy in III-V systems.[142] Carbon is a majority acceptor in GaAs and it also has shown negligible diffusion relative to other p-type dopants in GaAs such as Be. The limited diffusivity of C in GaAs however is offset by the very low activation of C in cases of ion implantation. Other authors have show that carbon activation can be increased by the co-implantation but from these studies it is not clear whether the co-implant effect is a damage effect or a chemical effect.[143] Carbon switches from net acceptor to net donor in InGaAs for In fractions greater than 0.7 and for the lattice matched composition most reports indicate that implanted C shows negligible activation and diffusion in $In_{0.5}Ga_{0.5}As$.[144]

Si is by far the most promising n-type dopant for implanted InGaAs as previous reports show that Si has some of the best activation and has shown limited diffusion in ion implant studies.[98], [115], [127], [145] It has the further benefit for ion implantation of being a light ion relative to the host crystal material and because of this it is less

damaging than Se or other dopants, which have shown similar levels of dopant activation.[131] Ge and Sn are less popular amphoteric dopants as previous authors have shown that it tends to have less activation in GaAs and InP and even reporting that carrier type can switch from n to p-type depending on annealing temperature.[2], [146] The higher atomic mass of Ge and Sn also results in increased radiation damage, which has historically been thought to be partly to blame for the low observed activation relative to Si.

Using MBE, experimenters have been able to grown both n and p type regions in GaAs using Si.[147]-[152] Some experimenters have taken this idea even further and have been able to create pn junction on the same GaAs wafer using only Si as a dopant.[153], [154] The non-equilibrium incorporation as well as the unique surface orientation makes for easier control over lattice location of Si impurities in GaAs, which allow experimenters to control between n and p-type doping. These experiments are regularly cited as proof of the amphoteric nature of these dopants but there are no reports as to whether these dopant configurations are stable with post-growth thermal treatment. Ion implantation of the amphoteric dopants results in preferential occupation of one sublattice (n or p-type) and no dopant is perfectly amphoteric such that no change in n or p-type conductivity is observed despite some dopants such as Ge and Si showing type conversion in GaAs depending on post implant annealing temperature.[146], [155], [156]

MBE experiments highlight the amphoteric nature of incorporated dopants with changes in carrier type, but in the case of ion implantation the amphoteric nature is often inferred from type switching of dopants or from the low percent activation of large

doses (>1×10^{14} cm^{-2}). While these are plausible explanations for limited n-type activation, compensating defects or clustering could also be possible reason for the observed activation limits without direct evidence of amphoteric dopant incorporation. In order to conclusively prove that the amphoteric nature of Si dopants is the reason for the observed low activation in ion implantation, methods that can resolve the specific lattice locations of impurities must be used.

2.6.4 Direct Observation of Dopant Sublattice Occupation

Early on experimenters recognized the need to determine sublattice location of impurities in III-V semiconductors. While electrical measurements are often enough to infer lattice location in elemental and group IV compound semiconductors, the more complex nature of native and impurity defects in III-V materials complicates the interpretation of the degree of amphoteric behavior based solely on electrical results. Early RBS/PIXE experiments by Bhattacharya indicated that for high dose S and Si implants, the majority of introduced dopants were shown to exists on lattice sites after annealing indicating that the reduces level of dopant activation in these materials was not due to implanted ions existing interstitially or in clusters.[157]-[161] This result suggested that all dopants were on active sites and the discrepancy between dopants on lattice sites and the measured activation was the result of self-compensation. This self-compensation may have taken the form of Si-Si next nearest pairs or from complexing with Si_{III} and Si_{V} sites existing. RBS is not sensitive to the presence of low concentration of vacancies in a lattice, however, so vacancy compensation cannot be rules out by RBS techniques.

Raman is another technique that has previously been used to measure the lattice location of impurities, as Si-Ga bonds will have different scattering energies than Si-As

bonds. This method has been used in GaAs to observe lattice location by comparison of the relative signals of Si-Ga peaks to Si-As peaks.[124], [162]-[170] While the method has proved useful in GaAs, in ternary compounds of InGaAs, the vibrational peaks of Si_{III} and Si_V are too close to be resolved.[171] X-ray absorption fine structure of XAFS has the best resolution of any of the techniques and has been used to study the nature of Si doping in GaAs and Ge doping of InP but the results of Si in GaAs are suspect in that many data manipulations were used in order to separate the Si-Ga and Si-As bond lengths.[172]-[174] In the case of Ge in InP, this technique is more robust as the bond length differences and associated atomic masses between In-Ge and P-Ge are much greater than for Si-Ga and Si-As making quantification much easier. XAFS is further complicated by the fact that the Si K edge is at 2 keV, which is between the energies at which most beamlines operate. At 2 keV the x-ray penetration depth is low so only the near surface region is explored. While direct observation of lattice location of some dopants is possible, unfortunately for the Si in InGaAs system, there does not seem to exist a method that can quantitatively determine the relative ratio of Si_{III} to Si_V, which further complicates subsequent interpretations of electrical activation results.

2.6.5 Dopant Diffusion

Diffusion of the dopant species is one of the most important selection properties for devices. Ideal dopants have limited diffusivity and high activation. The host lattice and dopant atom predominately governs dopant diffusivity, but incorporation method can also affect the observed diffusivity.

Dopants diffuse by either an interstitial or vacancy mechanisms in a crystalline solids. Species that diffuse via an interstitial mechanisms generally out-diffuse species that diffuse via a vacancy mechanism as the energy to diffuse interstitially is often less

than required to diffuse via a vacancy mechanism. Be is a small atom relative to In, Ga, and As and it is unsurprising that Be can easily move interstitially thought the crystalline lattice. S and some of the transition metal dopants are also thought to diffuse via an interstitial mechanism. Some of the larger atoms such as Se, Si and Ge show much lower diffusivities in the III-V arsenides and are though to diffuse via a predominately vacancy assisted method. Even within the vacancy and interstitial diffusion types many dopants exhibit very specific mechanisms (interstitial kick out, divacancy, transient enhanced diffusion, oxidation enhanced diffusion, etc) that are dopant/host specific but a formal treatment and understanding of these individual dopant/host mechanisms is outside the scope of this work.

2.6.6 Concentration Effects

Concentration effects play a large role in the observed diffusivity of dopants in III-V materials. Previous authors have shown that the background p-type doping in a material can affect the diffusivity of n-type dopants and this same effect of background doping on diffusivity has been studied for p and n-type dopants in GaAs.[175]-[180] Quantum well and heterojunction intermixing studies also show a great deal of evidence for concentration dependent diffusion effects.[181]-[183] The bulk diffusivity of a dopant is proportional to the sum of the vacancy diffusivity times the concentration of vacancies plus the interstitials diffusivity times the concentration of interstitials as show in the equation below.

$$D_{eff} \approx D_V N_V + D_I N_I \tag{2-3}$$

Dopants that diffuse via vacancy mechanisms will show enhanced diffusivity when vacancies are introduced and dopants that diffuse via interstitial mechanisms will

show an enhancement when the concentration of interstitial are increases. Injection of excess vacancies and interstitials at the surface has been observed via nitridation or oxidation of Si which can result in enhanced or diminished diffusion of dopants near surface depending on their predominate diffusion mechanism.[184], [185] Ion implantation has also been used a method to introduce high concentrations of vacancies and interstitials into a host material at precise depths. This fact has been used extensively in marker layer studies in order to determine the nature of diffusion for a given dopant species.[186] Marker layers of vacancy type diffusers will show enhanced diffusion when a vacancy rich region is formed in the layer and the same layer will be generally unaffected when saturated with interstitials.

This concentration effect occurring from implantation has had serious implications in devices with one such phenomenon known as transient enhanced diffusion.[186]-[191] Transient enhanced diffusion as observed in B implants into Si and subsequent studies confirmed that excess interstitials in the tail of the implant occurring from the ion implantation of B into Si had the effect of increasing B diffusivity in Si.[187] Be dopants in InGaAs have also been shown to be susceptible to transient enhanced diffusion and a larger number of dopants in other semiconductor-dopant systems have also shown transient enhanced diffusion behavior due to point defects.[192]

2.7 Summary of Defects and Doping in Semiconductors

From the above discussion it is obvious that there are a variety of different types of defects occurring in semiconductors that can result in desirable or sometimes undesirable properties in the final engineered material. In some respects the entirety of the semiconductor industry is based on the ability to accurately and precisely control the number of defects that result in the desired engineering properties and mitigate the

presence of defects that undermine the intended device performance. With this understanding, the value in knowing and predicting how different dopants and processing methods can affect the character and population of defects becomes readily apparent. In this work we are most interested in the understanding the nature of dopant-defect interactions in n-type InGaAs material formed by ion implantation.

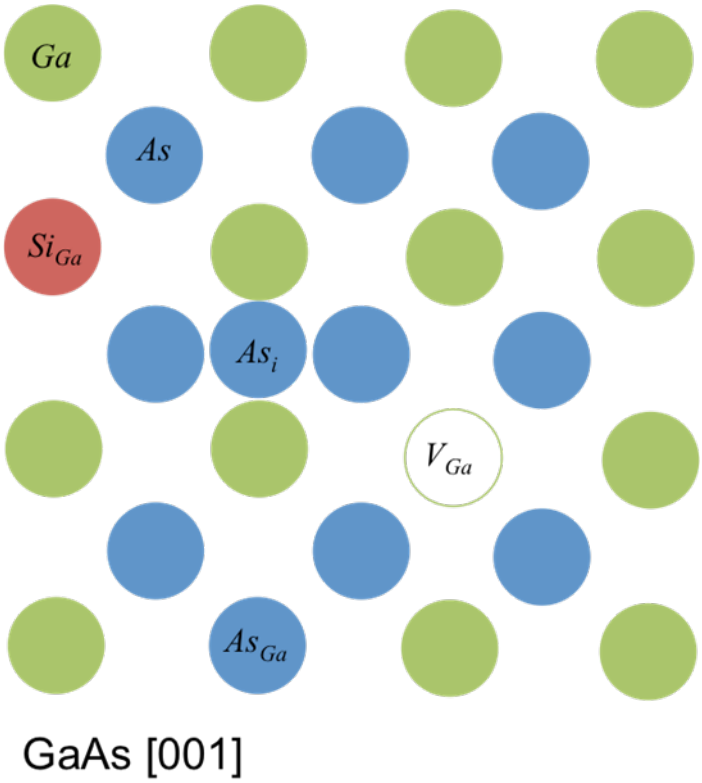

Figure 2-1 Schematic diagram of various point defects in GaAs.

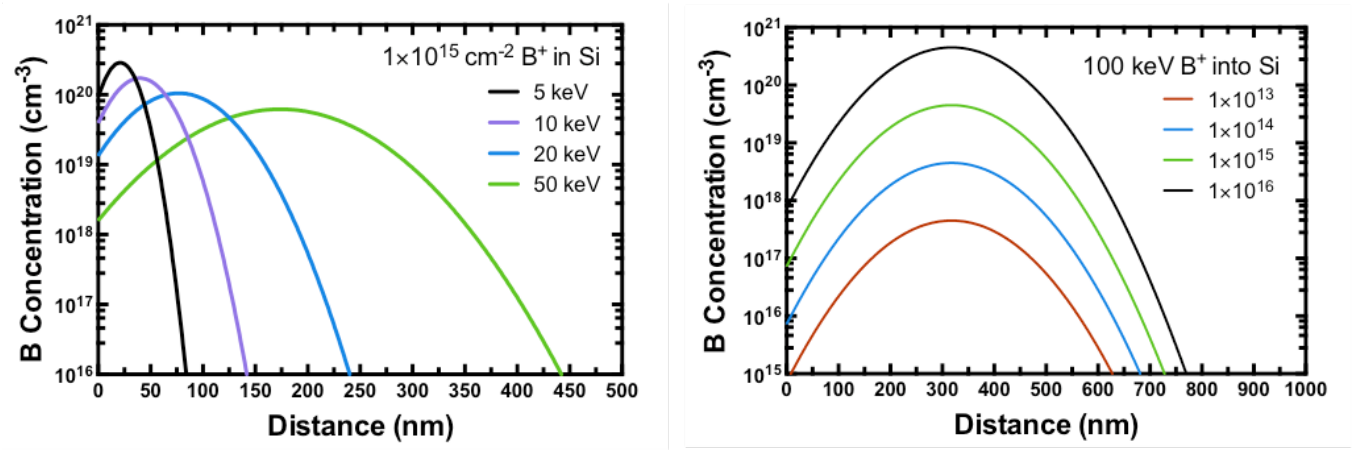

Figure 2-2. The calculated implanted concentration profiles of B in Si. The concentration as a function of depth highlights the effect of implant energy for a fixed implant dose and implant dose for a fixed implant energy

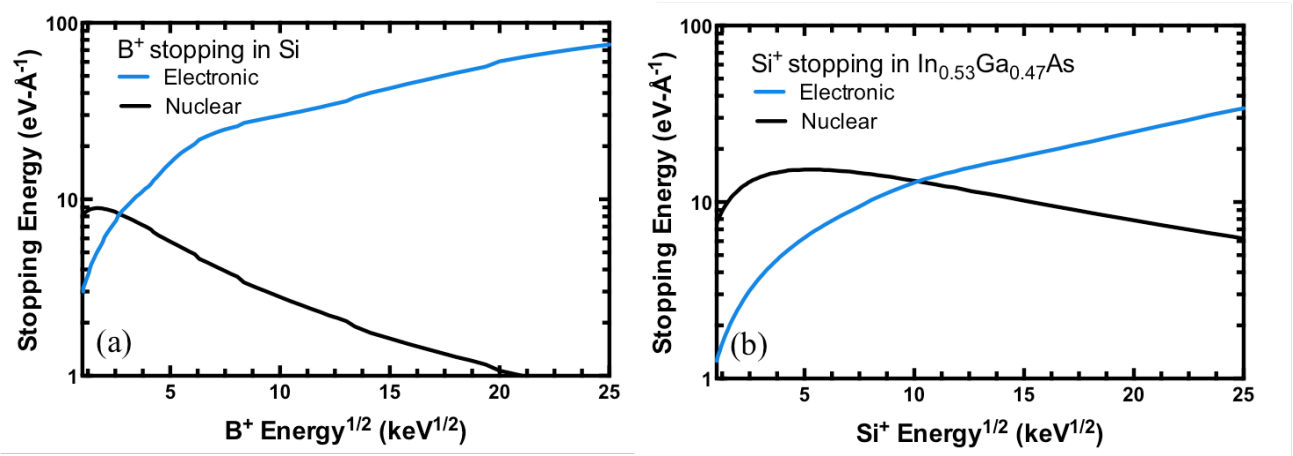

Figure 2-3. The calculated contributions of electronic and nuclear stopping as a function of ion energy. The stopping contributions are calculated for (a) B^+ implants into Si and (b) Si^+ implants into $In_{0.53}Ga_{0.47}As$. Notice that the peak of nuclear stopping occurs at an energy in keV near the atomic mass of the incident ion.

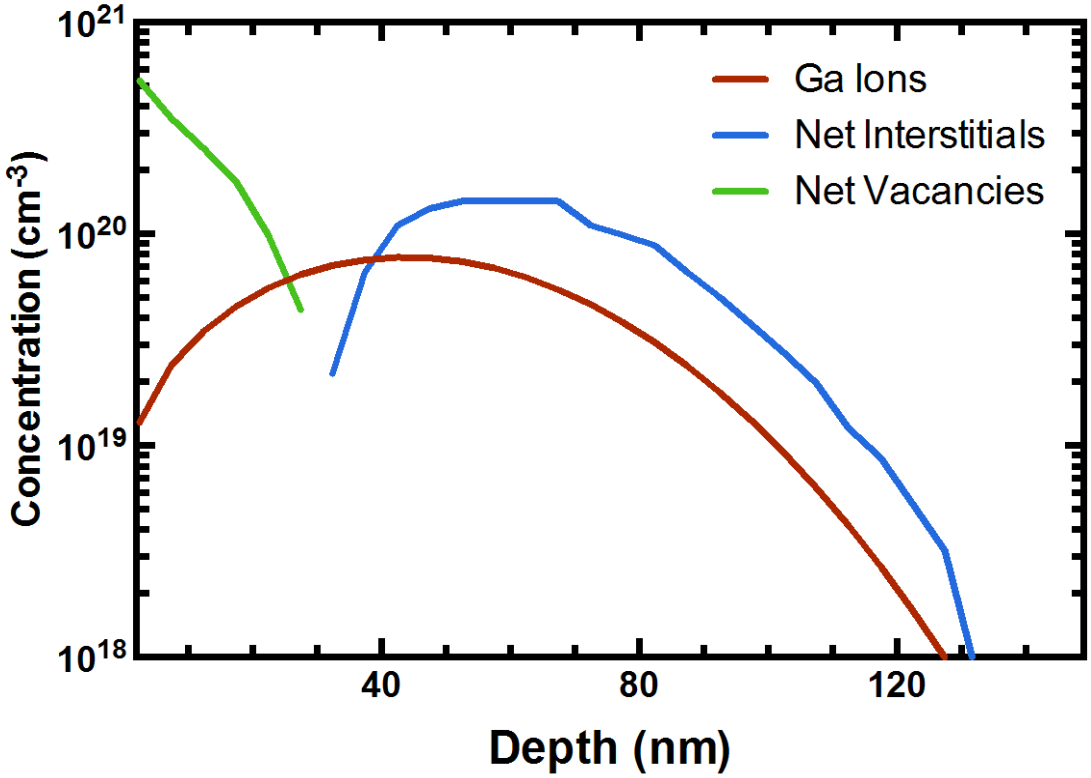

Figure 2-4. The calculated profile of implanted Ga ions, net interstitials and net vacancies using Boltzmann transport equations. The calculation is for a 100 keV, 6×10^{14} cm^{-2} Ga implants into $In_{0.53}Ga_{0.47}As$.

CHAPTER 3
CHARACTERIZATION AND EXPERIMENTAL METHODS

In many ways the questions we ask determines the information we receive. Perhaps this idea is most beautifully illustrated by the nature of light. The wave-particle duality of light actually arises from the nature of the questions we ask. When we ask light questions as waves we receive our answers in waves and when we ask particle-like questions we receive particle-like answers. In order to arrive at the proper conclusions, we must then make use of the appropriate tool and methods for our questioning. In this work we are generally concerned with discerning the truth about the chemical, structural and electrical nature of Si dopants in InGaAs. As such, some tools are more adept than other at determining information about structure whereas some are more adept at discerning the chemical nature of our samples. Some of the more versatile tools can combine information about the structure, chemistry, and electrical nature of samples into one analysis technique.

3.1 Secondary Ion Mass Spectroscopy

Secondary ion mass spectroscopy or SIMS is an especially sensitive technique for inquiring about the chemical nature of materials. There are a variety of specific SIMS methods but the SIMS results in presented in this body of work is more exclusively dynamic, time of flight SIMS performed with 350 eV Cs^+ primary ions to improve the depth resolution and secondary ion yield for the concentration profiles. Dynamic SIMS measurements presented in this work were performed by Evans Analytical Group using their point correlated, time of flight (PCOR-SIMS) with a 350 eV Cs^+ primary ion beam. Time of flight mass spectroscopy is used to uniquely identify the sputtered atoms. Individual atom mass and the corresponding mass to charge ratio is to atoms and

molecules as fingerprints are to humans. From these unique combinations of mass to charge it is possible to determine the chemical makeup of a sample. Unlike electron and scattering spectroscopic methods which are part of a continuum, mass spectroscopy is discrete which greatly improves the chemical sensitivity of SIMS relative to other chemical identification techniques even if there are only small differences in mass between species. Species with higher mass to charge ratios will have longer times of flight as evidenced by Eq. (3-1) below.

$$t = k\sqrt{\frac{m}{q}} \tag{3-1}$$

SIMS has the added benefit of being sensitive to concentrations of parts per million and less, which make it especially useful in semiconductors where impurity concentrations in the order of parts per billion are often used. With proper calibration of sputtering rates and secondary ion yields for a given material, SIMS can be used to monitor chemical composition along a sputtered depth of a sample and as such will give concentrations of the constituents over a depth ranging from nm to um of material. One limitation of dynamic time-of-flight SIMS is that it can only yield 1-D concentration data from a sputtered surface. More modern techniques such as atom probe are being explored to give 3-D compositional and spatial reconstructions using a similar time of flight technique.[193]-[197]

3.2 Rutherford Backscattering Spectroscopy

Rutherford backscattering spectroscopy or (RBS) is similar to SIMS in that incident particles are required to probe for information but RBS is capable of probing both the structural and chemical makeup of a material. In RBS, the incident particle is

often an alpha particle or proton that is accelerated at energies from 1-3 meV. Structural information of a material can be determined from the ability of an incident ion to be channeled through a lattice. In channeling mode (RBS/C) the energy of reflected ions can be correlated to the structural arrangement of atoms the target material. For cubic semiconductors with a diamond or zincblende structure, incident ions channel readily down the specific crystallographic directions such as the <100> or <110> directions but deviations in crystallinity will cause the incident ions to collide and be ejected back to the surface. The energy of the backscattered ion is proportional to the depth into the sample, which the ion travelled. Furthermore, the frequency of backscattering can be related to the number of deviations from crystallinity along a channeling direction that can cause backscattering. This is used to great effect in determining the depth and formation of amorphous layers in radiation-damaged solids. The differing mass of the target materials will also scatter the incident to greater or lesser degrees and affect the backscattered energy. Atomic species will have peaks at differing energies depending on the scattering radius of the nucleus in the target materials. From this, chemical composition can be inferred indirectly from deviations in mass of the constituent atoms in the target material. Particle induced x-ray emission or PIXE can be performed during RBS and chemical data can be ascertained. PIXE has been used to determine he makeup of interstitial atom clusters or even the lattice locations of dopants in some materials systems. RBS measurements presented in this work were performed by Mark Ridgway at Australia National University with a 2 MeV He beam.

3.3 Raman Spectroscopy

Raman spectroscopy is similar to other energy-based spectroscopies in that the reduction of energy of an incident source is used to determine chemical or structural

information based on the amount of scattering that occurs. In Raman spectroscopy the incident probe is a photon. Inelastic photon scattering is a rather weak phenomenon and as a result high intensity light sources such as lasers are often required to obtain detailed scattering information. Raman is an incredibly versatile tool and it is often used to probe the nature of intermolecular bonds[124], [163], [164], [168], [170], [198] but it can also be used to determine free carrier concentrations in polar semiconductors due to photon-phonon interactions, which is the extent of Raman spectroscopy performed in this work.

Longitudinal optical phonons readily couple with the plasmon oscillations of the free carriers in polar semiconductors resulting in low frequency scattering events. The shifts of the L_- and L_+ longitudinal optical phonon-plasmon coupling modes are directly dependent on the free carrier concentration and the measured shift can be correlated to a free carrier density. The L_+ coupled mode is especially sensitive at high electron concentrations and has been used to many III-V compounds to estimate the free carrier concentration.[162], [199]-[202] This technique has advantages over techniques such as Hall effect where contacting can in some instances result in complications such as the case with InAs or other materials which form surface inversion layers. It also has the added benefit that the technique is a direct measurement of carrier concentration whereas active carrier concentrations in other materials must be calculated form sheet number measurements and corresponding knowledge of dopant concentration profiles.

Raman spectroscopy performed in this work was done at the Nanoscale Research Facility using a Horiba Jobin-Yvonne LabRAM Aramis spectrometer with a charge-coupled detector and the 1800 g/mm diffraction grating. The reported Raman

shifts are relative to the Rayleigh line of the incident 532 nm laser which was chosen to limit the optical depth of the subsequent measurements to the near surface region of the sample.

3.4 Transmission Electron Microscopy

Transmission electron microscopy (TEM) is a wonderfully effective instrument for probing the structure and chemistry of materials as well. Unlike SIMS and RBS transmission electron microscopy relies on the use of electrons instead of ions. Electrons have much less mass than ions and as a result cause much less sample damage and are easier to accelerate to high velocities yielding much smaller wavelengths and higher spatial resolutions than are possible with ion beam techniques. In fact, the most advanced instruments available today can resolve structural and chemical information of individual atoms. TEM has another advantage over SIMS and RBS in that the images are direct representations of the sample structure. In TEM images, information about relative chemical composition and thickness of layered structures can be directly observed whereas isn't SIMS and RBS information about structure must be inferred. While RBS is adequate for detecting the presence of an amorphous layer in solid, TEM is much better at correctly discerning the thickness and even the roughness of the layer in question. Furthermore, multiple modes of TEM operation exist that can be used to discern even more specific information about a given sample. The contrast that forms a micrograph results from a few different mechanisms that can be used to obtain information about the nature of crystallinity, defects, and chemical composition in a TEM sample.

Diffraction contrast can tell us about the crystallographic orientation and makeup of a specimen. In the TEM, electron diffraction results can be obtained using the same

principles and equations, which were first developed in x-ray diffraction. Instead of photons, electrons are used resulting in a change in incident probing wavelength. The observed diffraction contrast is from the constructive interference according to Bragg's law shown in Eq. (3-2).

$$n\lambda = 2d \sin\theta \tag{3-2}$$

Polycrystalline samples with random orientations will yield a continuous ring structure in diffraction mode, whereas single crystalline structures will result in discrete patterns when the diffraction condition is met as shown in Figure 3-1. It is also possible to look at diffraction over small areas with selected are diffraction and depending on the size of the crystallites it is possible to see diffraction patters between the single crystal and classic polycrystalline patterns.

In bright field images, strongly diffracting areas will appear light and areas that do not satisfy a diffraction condition will appear darker. Mass contrast also present in bright field images results from differences in the scattering cross sections of a material. Heavier Z atoms scatter more than light elements and result in darker regions of a micrograph.

Diffraction and mass-thickness contrast is observed in BF, DF, and HR-TEM modes. Chemical information can be observed in BF-TEM mode from the mass contrast, as heavier elements tend to induce more scattering and as a result transmit fewer electrons and appearing as darker elements in a given micrograph. BF-TEM and DF-TEM is also sensitive to variations in lattice strain and resultant changes in electron diffraction. In BF-TEM, defects cause local lattice strains where the proper diffraction condition is not met and they appear as dark areas. While extended defects were

hypothesized to exist in solids and explain the large deviation in actual strength from theoretical strength of metals, it wasn't until the invention of the TEM that they could be directly observed and quantified. In DF-TEM, the diffraction condition is changed such that deviations from crystallinity that do not meet the proper diffraction condition appear lighter in contrast by tilting the beam off of the zone axis. Mass contrast is less discernible in this configuration although sample thickness and scattering due to sample thickness is still apparent. Weak-beam dark field TEM or WBDF has the further distinction of having much better resolution of extended defects in a since only the dislocation core is at the proper condition to result in diffraction and this technique is the gold standard for quantifying dislocation densities in a given material.

Phase contrast is the defining contrast mechanism for HR-TEM. High resolution TEM is fundamentally the same as bright field TEM, but the additional information of extra diffracting Bragg beams results in phase contrast in the image. The periodic arrangement of atoms in a crystalline lattice results in multiple diffraction conditions existing and as a result the interaction of the diffracted beams with the solid can be observed with the formation of a lattice. In HR-TEM chemical information about mass is the same as for BF-TEM with light elements appearing lighter in contrast to heavier elements that appear darker.

3.5 Scanning TEM

Scanning TEM is similar to scanning electron microscopy and distinct from normal transmission electron microscopy in that a converged probe is used rather than a parallel beam. In converged mode the resultant micrograph is not dependent on diffraction data. Depending on the detector placement either a BF of DF condition may be obtained. In the case of DF stem, the annular detector is place between the sample

and electron source and information about the same comes from reflected electrons. In this case, heavier elements appear lighter as they scatter more electrons back into the detector. In the case of BF stem, the detector is placed behind the sample and incident electron beam. In STEM mode the probe is ideally converged on the sample surface and there is no resultant diffraction data to be obtained. Diffraction contrast from defects is no longer visible so the information in a micrograph of a given sample is mostly chemical in nature similar to the information see in TEM. In the case of aberration corrected Cs-TEM also referred to as high angle annular dark field stem (HAADF-STEM), the probe size is less than that of an atom and because of this, individual atoms can be resolved. This can be used to observe some crystallographic defects in this case.

In STEM mode the electron probe is rastered over a large area to form the image. However, the rastering allows the probe position to be correlated to a location on the lamella. When spatial information is coupled with energy dispersive spectroscopy (EDS) or electron energy loss spectroscopy (EELS), STEM mode operation can be used to discern absolute chemical information as opposed to relative chemical information. EDS is based on the characteristic energy emitted by the return of outer shell electron from the excited to the ground state and with EELS the loss of incident electrons can be related to the interaction of the incident electron beam with the electron shell of the material through with the beam is transmitted. EELS is generally more sensitive to light elements and is more sensitive to lower concentrations than EDS. All of the TEM and STEM presented in this work was performed at an operating

voltage of 200 keV with the JEOL 2010F located in the Major Analytical Instrumentation Center.

3.6 TEM Sample Preparation

TEM sample preparation is perhaps the trickiest aspect of performing TEM. Without optimized samples it is nearly impossible to extract the desired information from a TEM sample. For most materials, samples must be 100 nm thick or less to be electron transparent. For HR-TEM images, lattice imaging is improved with lamella thicknesses of 50 nm or less. Samples with light elements that scatter less are often more forgiving in terms of thickness than sample made of heavy elements. In all cases, generating large, areas of view with uniform thinness can be tricky. Sample preparation for TEM of nanoparticles and nanowires is relatively straightforward as the samples are often already thin enough to be electron transparent and as such require only placement on a TEM grid. Multiple methods of sample preparation exist and to aid the preparation of metal, ceramic, or semiconducting TEM foils from bulk materials such as jet polishing, etching and ion milling. However, for this work two focused ion beam (FIB) methods of sample preparation were used on the FEI Dual-Beam Strata DB235 FIB located in the Major Analytical Instrumentation Center.

3.6.1 Cross Sectional Focused Ion Beam Sample Preparation

The focused ion beam is one of the most versatile methods of creating TEM lamella or foils. With FIB a beam of gallium ion is used to mill substrate material until a lamella of 100 nm or less is obtained. The focused ion bean is most often a combination FIB/SEM such that the progress can be monitored by the electron image. The focused ion beam is able to mill any materials and because of this it is one of the most versatile techniques for creating TEM foils.[203], [204] Any materials system can be milled into

electron transparent specimens but the time required to make an individual lamella is directly related to the hardened of a material. While soft materials such as InAs and stainless steel can be made very quickly, materials made with sapphire or diamond require much longer milling times.

This technique is also especially well suited for making lamella from specific regions of interest. It also cuts down considerably the number of steps required to make cross-sectional TEM samples. Cross sectional TEM samples are made using the ubiquitous h-bar technique. In which a protective layer of platinum and carbon is placed over the area of interest and sample material around this is removed such that a lamella thinner than 100 nm is obtained.

3.6.2 Plan-View Focused Ion Beam Sample Preparation

To create plan-view samples, an allied polishing multiprep tool was used to grind the samples down to thicknesses of 25 μm or less. The thinned sample was then glued with m-bond to a molybdenum support grid that was cut in half and the sample was then milled in the FIB using a one-sided h-bar technique making sure that the sample surface was never rotated into the ion bean such that damage of the surface could occur. This method does not result in large electron transparent areas like etching or conventional ion milling but it worked well for the limited amount of sample material available and is useful for materials that are not easily etched.

3.7 Hall Effect

Multiple methods exist to determine the resistivity or conductivity of given material but Hall effect is capable of determining the conductivity of a material as well as being able to separate out the individual components to conductivity such as the carrier concentration and mobility. It has the added benefit of also being able to determine the

carrier type. The ability to de-convolute the carrier concentration, carrier type and mobility make Hall effect by far the most versatile and information dense electrical measurement that can be performed on a sample.

In van der Pauw Hall effect the sheet resistance is calculated numerically with Eq. (3-3) based on the current application and voltage sensing geometry shown in Figure 3-2.

$$\mathrm{Exp}\left(\frac{-\pi R_{12,34}}{R_s}\right) + \mathrm{Exp}\left(\frac{-\pi R_{23,41}}{R_s}\right) = 1 \tag{3-3}$$

Hall effect makes use of the Lorentz force to deflect charged carrier perpendicular to the direction to the applied magnetic field (B) as shown in Eq. (3-4).

$$\mathrm{F} = qv \times B \tag{3-4}$$

The accumulation of carriers occurs on the bottom or top of the sample depending on whether carriers are holes with positive charge or electrons with a negative charge. The change in carriers across the sample results in a potential difference in measured voltage for an applied current when measured in the van der Pauw configuration shown in Figure 3-3.

In van der Pauw Hall effect the voltage from opposite corners is measured with the application of a constant current. The voltage is measured under positive and negative magnetic field and the potential difference between the positive and negative B-field measurements is the Hall voltage due to carrier deflection. Negative Hall voltages indicate that the carriers are predominately electrons while positive Hall voltages indicate that the carriers are predominantly holes.

The current flow direction is reversed and the average of all the Hall voltages is calculated for both sets of corners for a total of 8 voltage measurements. The current

reversal is important to removing concentrations from the Seebeck effect that occur when junctions between metals with different work functions are created. Knowing the applied current, and strength of the magnetic field and the hall voltage the sheet carrier concentration can be calculated with Eq. (3-5).

$$N_s = \frac{IB}{q|V_h|} \tag{3-5}$$

Mobility may then be calculated with the results of the sheet number and sheet resistance calculations with Eq. (3-6).

$$\mu = \frac{1}{qN_sR_s} \tag{3-6}$$

A Micro Miniature Refrigerators (MMR) variable temperature Hall effect tool was used to perform the Hall effect measurements in this work. Measurements were performed at a constant field of 3500 Gauss. All Hall measurements used the previously discussed van der Pauw geometry at room temperature on square samples at least 0.8 cm on a side with pressed on indium contacts in the corners. Ohmic contacts were verified by checking for linear, non-rectifying, I-V characteristics on a curve tracer.

3.8 Atomic Layer Deposition

Atomic layer deposition is not a characterization technique but rather a processing technique used extensively in this work. For all the samples in this work Al_2O_3 dielectric layers were formed by ALD prior to thermal treatment to prevent surface degradation. The high degree of uniformity and thin layers achieved were instrumental in forming layers with minimal amounts of pinholes and the thinness allowed samples to accommodate stress due to thermal expansion mismatch better than thicker layers. Early experiments and samples were capped with 50-100 nm of PECVD SiO_2 but comparison after thermal annealing at 850°C for 5 s showed that samples with ALD

caps exhibited fewer and less severe instances of pitting or surface degradation. Attempts to optimize the cap beyond the initial deposition of 15 nm of ALD Al_2O_3 were not made since XTEM studies showed that annealing at temperatures of 750°C resulted in no observable surface degradation. It is possible that the surface protection could be further optimized but this was outside the scope of this work.

The high level of uniformity in ALD is due to the uniform adsorption of reactive precursors. Oxides and nitrides can be easily formed by the introduction of a organometallic precursor such as tri-methyl-aluminum in a carrier gas that is then allowed to diffuse across the surface for a specified amount of time. The chamber is then purged with argon or some inert gas to leaving only un-reacted precursors attached to the surface. After this step, in the case of oxides, water vapor is introduced and in the case of nitrides, nitrogen plasma is reacted with the methyl precursors. The chamber is then purged again and the cycle repeats. Long precursor adsorption times allow very uniform coating of even high aspect ration trenches but the deposition rate of this process is much lower than PECVD or sputtering. This technique is very good for depositing many of the high-k dielectrics in production now because of the uniformity and small layer thickness that are easily achieved. It has also been shown in InGaAs that the tri-methyl aluminum precursor can be used in the ALD to perform in-situ surface cleaning of the native oxides and passivating surfaces before deposition of the gate dielectric.[205], [206]

ALD performed in this work was done in the cleanroom of the Nanoscale Research Facility at the University of Florida using the Cambridge Nanotech Fiji system. A exposure mode recipe was used to provide the best surface coverage and this mode

resulted in deposition rates of about 1.1 Å/cycle and a deposition time of 13 hours for a 15 nm thick layer. The exposure mode recipe used on this tool is included in Appendix B.2.

3.9 Ion Implantation

Christopher Hatem performed the ion implantation in this work. The tool used was a commercially available Applied Materials VIIsta Trident with Thermion. This particular implanter is a high current, ribbon beam implanter with the added feature of being able to do elevated temperature. The current used for the incident implanted ions in this work was 1.1 mA. All implants were performed at a 7° tilt and 25° rotation to further limit random channeling of implanted ions. The beam current and implant geometry was maintained for all of the implants in this work such that any comparison between dose, implant energy, implant species, or implant temperature in this work is self-consistent. A more thorough treatment of ion-implant as a means for doping is included previously in section 2.4.4

3.10 Thermal Annealing

All samples were encapsulated with 15 nm of ALD Al_2O_3 before annealing to prevent surface degradation. Two thermal annealing methods were used in this work. Tube-furnace anneals were performed in 2.5” Lindhard furnace with flowing Ar ambient at a rate of 5 l/m. Samples were placed surface of interest side down on piece of Si carrier wafer supported by a fused silica boat. Temperature calibration was performed by with a k-type thermocouple placed at the desired boat position along the length of the furnace prior to performing the annealing treatment.

Rapid thermal annealing (RTA) was performed using a AG Associates HeatPulse 4100 halogen-lamp RTA with a flowing Ar ambient. The ramp rate used in these

anneals reported in this work was set at a constant 60°C/s. Temperature during the anneal was measured by placing a type-k thermocouple between two Si carrier wafers. Samples annealed by RTA were also placed surface of interest side down on the Si carrier wafer as well ensuring as self-consistent as possible methodology between samples annealed in the tube furnace and the RTA.

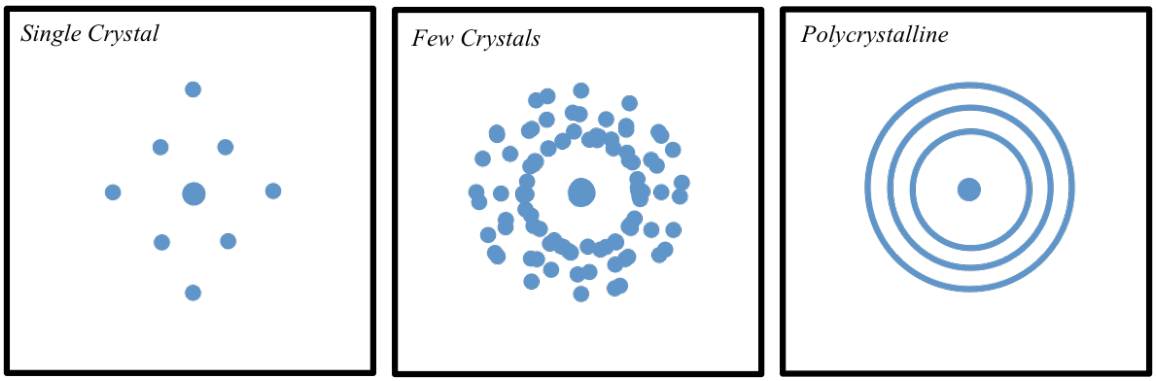

Figure 3-1. Schematic diagram showing the diffraction patters obtained by TEM. The patterns shown are for single crystal few crystals and polycrystalline materials.

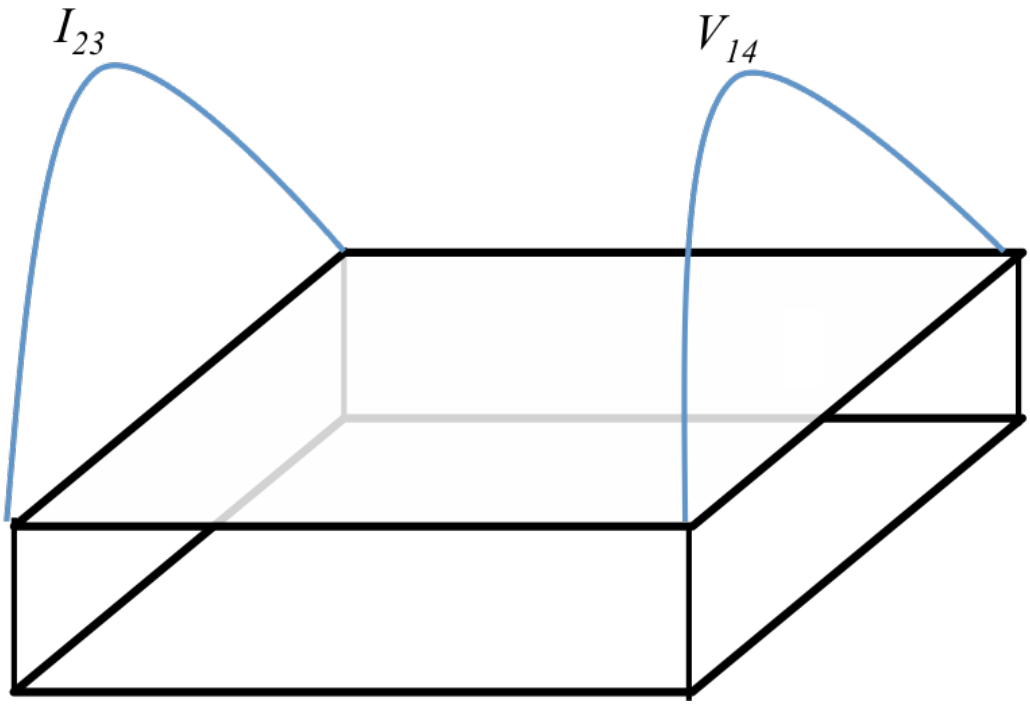

Figure 3-2. Schematic diagram showing the contacting scheme for sheet resistance measurements using the van der Pauw Hall geometry

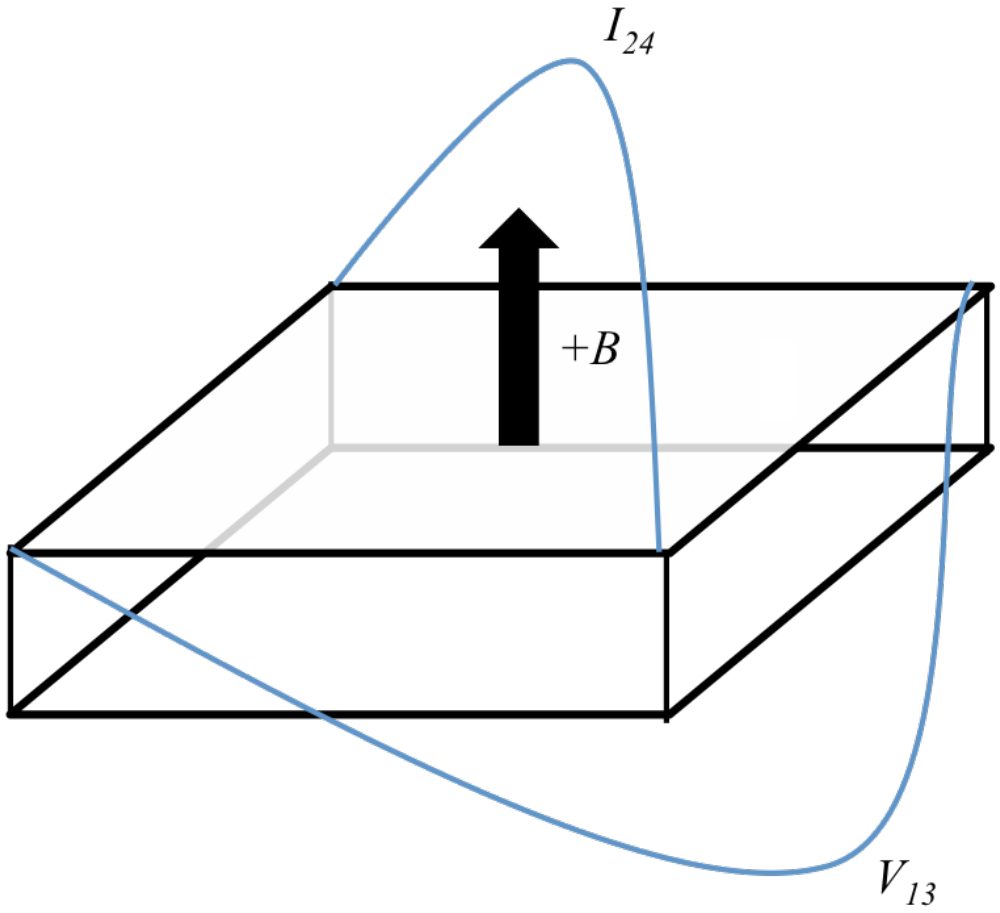

Figure 3-3. Schematic diagram showing the contacting scheme for Hall voltage measurements using the van der Pauw Hall geometry

CHAPTER 4
ACTIVATION AND DIFFUSION OF SI IMPLANTS INTO InGaAs AND InAs

Self-alignment and a reduction in etch and growth steps makes ion implantation more desirable than growth based doping techniques for formation of heavily doped source and drain regions in CMOS structures but the required active carrier concentrations in these regions may be difficult to obtain via implantation. Some estimates indicate that the required carrier concentrations for source and drain regions need to be in the range of 3-10×10^{19} cm^{-3} to achieve low enough contact resistances.[23], [27], [207] Growth doping is generally shown to result in higher active carrier concentrations than implant doping but it not known if optimizations of implant conditions can result in further enhancements in electrical activation. Accurate models for the diffusion of incorporated dopants are also necessary to generate accurate predictions necessary to design devices using the Si–$In_{x.}Ga_{1-x}As$ system.

4.1 Previous Implant Studies

Previous implant studies of Si implants have indicated that Si and Se seem to be the best candidates for n^+ dopants into $In_{0.53}Ga_{0.47}As$.[98], [115], [126], [127] A more significant body of work characterizing the electrical activation of Si, Se, and S implants into GaAs exists as well.[2], [93], [130], [132]-[134], [140], [208]-[213] All previous studies of implants into generally report active sheet numbers below the implanted dose and studies that calculate solubility also show that implanted dopants exhibit active concentrations in InGaAs of around 1×10^{19} cm^{-3} or less depending on the annealing methods and dielectric caps used. One serious limitation of the majority of these early studies is the lack of microstructural investigation along with electrical activation.

It has been shown that amorphization in III-V materials results in very defective regrowth and as a result it is desirable to avoid amorphization.[81], [214], [215] Many of these early studies use doses that are likely amorphizing and as such the active implanted Si profile exists over two distinct regions with very different mechanisms of dopant incorporation. Dopants beyond the amorphous crystalline interface exist in point defect rich regions whereas Si or other dopants that are in the amorphous regions are presumably incorporated into lattice sites upon regrowth however this mechanism is not well understood in III-V materials as dopants do not tend to show activation upon regrowth unlike Si.[216], [217] Many previous studies were also performed with very high implant energies that are unlikely to be technologically relevant for III-V integration into CMOS devices. The nature of the implant damage in these studies is also different, as most technologically relevant implants will be performed at energies below 20 keV where nuclear stopping will dominate for impurity implants into InGaAs and the recombination of interstitials and vacancies from the implant is likely to be much more efficient. The work of this dissertation is directed toward more technologically relevant implant conditions and also investigates the dependence of post-implant microstructure on electrical activation.

4.2 Effect of Implant Temperature on Si Activation in InGaAs

Previous studies in GaAs have used elevated implant temperatures to reduce implant damage by increasing the amount of dynamic annealing and these studies also report higher electrical activation for doses and energies that are likely non-amorphizing. The reason for the enhanced activation in these studies is unclear since they do not have corresponding microstructural observations or quantify the amount of post implant damage.[85], [127], [132], [218], [219] The required dose to amorphize III-V

materials can very considerably depending on dose rate, implantation temperature, and the mass of the implanted species but studies of Ga, Ar and O ions into InGaAs show that doses ranging from 8×10^{13} – 5×10^{14} cm^{-2} are capable of producing amorphous layers for implants performed at 300K and below.[64], [67], [199], [220], [221]

In order to determine the implantation temperature necessary to avoid amorphization a 20 keV, 6×10^{14} cm^{-2} Si^{+} implant was chosen implanted at 20, 80, 140, 200, and 300°C to determine at what temperature amorphization could be avoided using post-implant XTEM. A complete table of the experimental conditions for all of the samples detailed in section 4.2 is included in Appendix B in Table B-1. The post-implant XTEM is shown in Fig. 4-1a-e.

From Figure 4-1b it is seen that even implants performed at 80°C are capable of preventing amorphization for the 20 keV, 6×10^{14} cm^{-2} Si dose. The amorphous layer thickness of 20 nm in the room temperature implant is less than the projected range as predicted by SRIM which further indicates that amorphization by Si implant occurs from the surface down in InGaAs. Surface-down amorphization behavior is consistent with the amorphization behavior of other species that are considerably lighter than the target material such as B^{+} implants into Si. The presence of an amorphous layer is also confirmed in post-implant RBS/C measurements shown in Figure 4-2b but RBS/C also indicates that the 80°C sample has a higher amount of post-implant damage despite showing no obvious signs of increased post-implant damage in XTEM. Samples implanted at 140°C and above show no signs of amorphization and a similar trend in damage from the RBS results suggests that implant temperatures above 140°C allow

for enough dynamic annealing in the material that amorphization can be prevented completely.

SIMS of the elevated temperature implant samples, shown in Figure 4-2a, was also performed on these samples to observe how implant temperature affects the as-implanted profiles. The 20°C implant shows the least amount of channeling and this due to the creation of a surface amorphization layer. Implants performed at 140°C and above exhibit co-incident Si concentration profiles indicating the substrate temperature was not high enough to contribute to Si diffusion and that reductions in channeling due to damage were avoided for these temperatures. The implant performed at 80°C also shows a reduction in random channeling but in the absence of an amorphous layer it is unclear whether the reduced Si penetration is due to de-channeling from the increase in point defects in the material or from reduced radiation enhanced diffusion relative to implants performed at 140°C and higher.

For intermediate temperature implants, radiation enhanced diffusion may play a role in the observed implant profile. At low temperatures the limited mobility of atoms in the collision cascade results in the accumulation of point defects with very limited mobility. At intermediate implant temperatures the temperature is high enough to allow for increased mobility of the long-lived point defects in the collision cascade created during irradiation that result in diffusion of species at temperatures below what is required for thermally activated diffusion. At very high temperatures, the collapse of the collision cascade due to increased dynamic annealing results in minimal redistribution of dopants. Further study is required to determine if radiation enhanced diffusion can explain the observed Si profiles for these intermediate implant temperatures. Profile

broadening for elevated temperature implants due to radiation enhanced diffusion has been observed in Se implants into GaAs.[222]

The ion-implanted samples from this study were subsequently encapsulated with 15 nm of Al_2O_3 deposited by ALD before being annealing for 5 s at 750°C. XTEM of the post-anneal samples are shown in Fig. 4-1(f-j). Type II, end of range damage (EOR) is shown to form near the amorphous crystalline interface for the 20°C implant while the non-amorphizing implants all show a large amount of type I sub-threshold loops forming beyond the projected range.[79] Despite previous reports indicating that the regrowth of III-V amorphous layers is highly defective, there is not much evidence of micro twins or stacking fault in the regrown amorphous layer of the 20°C implant. This observation suggests that annealing conditions used were able to recover subsequent regrowth damage or that the regrowth of shallow amorphous layers results in less defective regrowth.

Electrical activation was measured by van der Pauw Hall effect after the encapsulating dielectric was removed in BOE. Sheet number data presented in Figure 4-3 indicates that elevated temperature implants that avoid amorphization result in higher activation upon annealing than the partially amorphizing implant. The intermediate implant temperature of 80°C shows the highest activation with an activation efficiency of approximately 15% of the implanted 6×10^{14} cm^{-2} Si^{+} dose. The electrical solubility of Si was estimated assuming limited Si diffusion as previous reports which have shown limited Si diffusion in InGaAs.[98], [115] The estimated electrical solubility of Si was found to be 9×10^{18} cm^{-3}, which agrees well with previous reports of the electrical solubility of implanted Si in InGaAs.[126], [127]

Based on these results, it was found that there is no benefit to using implant temperature higher than what is necessary to avoid amorphization. The results of the electrical measurements and RBS/C further suggest that Si activation for short anneals is actually enhanced by the presence of non-amorphizing damage. One possible reason for the increase activation at intermediate implant temperatures is that the higher number of vacancies resulting from the implant allow for a greater number of sites for Si atoms to move onto and become active which may be increasingly important for activation of Si with short anneal times.

A second experiment was performed on samples with the same 20 keV, 6×10^{14} cm^{-2} Si^{+} implant to monitor the activation of Si in InGaAs in for amorphizing implants and intermediate and high temperature implants. The same encapsulations and substrates were used but only implants performed at 20, 80 and 300°C were monitored. A series of 5 s RTA's were performed on these samples beginning at 400°C and going up to 750°C in 50°C increments. The samples underwent multiple anneals at the varying temperatures such that the activation numbers presented after annealing 750°C were due to the multiple annealing sequences used. Fig. 4-4 shows the results of the consecutive annealing for 20 keV, 6×10^{14} cm^{-2} Si^{+} implants InGaAs.

No appreciable activation is observed until annealing temperatures of 500-550°C. This behavior is consistent with the results of others who generally report poor activation of implants in III-V materials until annealing of 550°C or more.[223] Upon annealing at temperatures from 500-600°C implants performed at 80°C show higher sheet numbers with the 300°C implants performing the worst. When the samples are annealed at 600-650°C there is no significant difference in the active sheet numbers

between the three-implant temperatures. Intermediate implant temperatures do not show enhanced activation over partially amorphizing, 20°C implants or 300°C implants until annealing at 700-750°C. These results indicate that annealing temperatures above 700°C are ideal for activating Si implants into InGaAs so long as the encapsulation method used can prevent surface degradation at these temperatures and times. Figure 4-5 compares the activation of the consecutively annealed samples in Figure 4-4 with samples annealed for single 5s anneals shown in Figure 4-3. Samples implanted in an intermediate range from 50-140°C show more activation than other implants temperatures performed at 20°C or greater than 140°C. The increased activation from consecutive anneals also indicates that a single 5 s, 750°C anneal was not sufficient to saturate the activation of the 20 keV, 6×10^{14} cm^{-2} Si^{+} implant.

4.3 Dose Effects on Si Activation in InGaAs

Previous experimenters rarely report 100% activation for Si implants into InGaAs even at small doses that result in peak implanted concentrations below previously reported solubility limits for Si in InGaAs.[98], [115], [126], [145], [224] These authors generally attribute the low percent activation to the amphoteric nature of Si. For amphoteric compensation it is suggested that implanted Si results in 70% of the implanted Si acting as a donor and the other 30% acting as an acceptor for low doses and at higher doses Si becomes increasingly amphoteric with more and more of the implanted Si sitting on group V sites. This occurs until the Si becomes perfectly amphoteric and every Si donor is compensated by a Si acceptor. The reasons for this thinking have been mostly speculative. There is limited evidence of direct lattice site observations in InGaAs for Si_{As} acceptors. Instead, these arguments are mostly based

on electrical results where the measured activation is assumed to be a result of only two possible configurations for Si that of Si_{As} and Si_{III}. This assumption does not account for compensation from other compensation mechanisms or the possibility of clustering at high Si concentrations. Liquid phase epitaxy (LPE) experiments studying n-type dopant incorporation in GaAs also generally report sub-linear dopant incorporation and activation behavior at low concentrations.[225]

A dose study was performed on these samples to determine when serious compensation occurred in these samples. Samples were implanted at energies of 12 and 20 keV with a dose of 6×10^{14} cm^{-2} at the previously determined ideal implantation temperature of 80°C and annealed at 750°C for 5 s to maximize the activation for the observed conditions. A complete table of the implant and anneal conditions for samples detailed in section 4.3 in included in Table B-2 of Appendix B. Figure 4-6 shows the active dose as a function of implanted Si dose for a 12 and 20 keV Si implant into InGaAs after 750°C 5 s anneals.

The lowest doses of 3×10^{13} cm^{-2} show the highest percent activation of the studied doses with percent activations of 58% and 73% for the 12 keV and 20 keV energy implants respectively. The measured percent activation decreases with higher and higher doses and implant doses of 1×10^{15} cm^{-2} only result in activation efficiencies of 9.4%. These results agree with earlier studies that indicate that high Si doses are compensated but from the sheet number results of the dose study alone it is not possible to elucidate the nature of the observed compensation.

4.4 Energy Effects on Si Activation in InGaAs

The effects of implant energy were also investigated using the previously established ideal implant temperature of 80°C as well as a 20°C for a 20 keV 6×10^{14}

cm^{-2} Si^{+} implant. A complete table of the implant and anneal conditions for samples detailed in section 4.4 is included in Table B-3 in Appendix B. The plot of active sheet number vs. implant energy is shown in Figure 4-7a. It is apparent that higher implant energies show better activation for a fixed dose but the mobility of these implants is shown in Figure 4-7b to not depend significantly on the actual active sheet number. These results highlight one disadvantage to interpreting the electrical results presented so far in terms of active sheet number only. The constant mobility may indicate that the actual active Si concentration is not changing much for the observed implants and that the higher activation observed in these implants is do to the broadening of the implant profile under a given solubility as indicated by the as-implanted Si concentration profiles determined by SIMS in Figure 4-8.

4.5 Discussion of Active Sheet Number vs. Active Carrier Concentration

Direct comparison of activation via sheet number measurements can be complicated for implant profiles that are not coincident or nearly co-incident as is the case for differing implant energies or once potential post anneal diffusion is accounted for. If there is a solubility limit for a given dopant, only dopant concentrations up to that limit will be active in a material with the rest of the introduced dopant existing in inactive configurations in the material. Implants of higher doses have a higher standard deviation from the mean and could affect the amount of carriers in under that solubility limit. This same effect is even more pronounced with changes in implant energy as sheet number measurements have no depth resolution and can only give information about the number of carries normalized to a given unit area. Because of the differences in dopant distribution in low energy and high energy implants for a given dose the

reduced activation levels seen so far for low energy implants may not be unexpected if there is an upper solubility limit to Si incorporation in InGaAs.

In epitaxial layers where there is often a constant doping concentration over a given thickness, sheet number measurements can be easily transformed into active carrier concentrations but in the case of implants, the shape of the implanted profile must be known to calculate active concentration from sheet number. To solve this problem, this work relies heavily on a technique used by previous experimenters that assumes a solubility limit for a given dopant.[226] In order to convert measured sheet numbers from Hall effect to carrier concentrations this solubility limit is applied to the impurity profile and the area of the impurity distribution such that the integrated area under this curve is equal to the measured active sheet number. This technique is shown in Figure 4-9 on simulated SRIM profiles below and also shows schematically how differences in dose and energy will affect the amount of dopants under the solubility limit. Previous profiling measurements of activation for higher energy suggest that a plateau in active concentration measured by differential Hall or capacitance-voltage profiling exists for Si implanted to GaAs and InGaAs.[127], [227] Raman spectroscopic measurements of the L_+ phonon-plasmon coupled mode which are a measure of scattering that is directly proportional to free electron concentrations were also were also performed on some of the samples in this work. The measured activations from Raman spectroscopy are consistent with active carrier concentrations estimated by applying a solubility limit and integrating under the post-anneal SIMS profile.[162], [201], [228], [229] Using this technique, it is possible to re-interpret the previous results of active sheet number in terms of the electrical Si solubility by using the post-implant

SIMS if we assume that the implanted Si profiles have negligible amounts of diffusion. This assumption is likely valid based on previous reports of limited Si diffusion for short annealing times but a discussion of Si diffusion is reserved for the subsequent section.

By applying the solubility limited interpretation to the initial results looking at elevated implant temperatures of Si in InGaAs as shown in Figure 4-10a the calculated maximum carrier concentration is 9.48×10^{18} cm^{-3} for the 80°C implants with the elevated implant temperatures and room temperature implants showing similar levels of implant solubility. When this technique is applied to the sheet number results of the variable implant energy data we see a similar effect in that the implant energy has limited effect on actual Si solubility as shown in Figure 4-10b. One interesting result is that activation for all of these implants seems to be limited to approximately $1\text{-}1.5\times10^{19}$ cm^{-3}. This agrees well with previous estimates of peak implanted dopant solubility but from a technology standpoint the amount of activation is orders of magnitude less than what is commonly achieved for Si doping and still much less than what can be obtained from MBE doping of InGaAs. Fig. 4-10b further indicates that for the entire range of implant energies studied the non-amorphizing implants result in higher active concentrations after a 750°C 5s RTA when minimal profile redistribution is assumed despite no visible amorphous region for 20°C implants at energies below 4 keV. Higher energy implants result in lower electrical solubility and this may be due to increased separation of vacancies and interstitials occurring during implantation as vacancies from non-amorphizing damage are likely to promote Si activation based on the observations of activation from the intermediate implantation temperature results.

4.6 Thermal Stability of Si Activation in InGaAs

Short anneal times and limited thermal budgets are desirable for processing of components since thermal treatments can cause adverse chemical reactions and dopant deactivation. Back end processing regularly requires the samples to undergo extended period of annealing at temperatures of 450°C or less. In order to study the possibility of dopant deactivation or meta-stability in these materials 10 keV, 5×10^{14} cm^{-2} Si^{+} implants performed at 80°C into InGaAs were studied at various annealing times. Initial experiments were performed at 750°C for 5, 10, 20, and 40 s in the RTA to see how the activation behavior changed as a function of annealing time. Longer anneals were also performed in a tube furnace. A complete table of the experimental implant and anneal conditions for the samples detailed in section 4.6 is included in Table B-4 of Appendix B. The activation results of RTA annealing at 750°C for 5-40 s are shown in the Figure 4-11.

The implants used in this study show no sign of deactivation and that the activation is actually increased with higher annealing times. In all cases there is no sign of dopant deactivation and it is observed that the active sheet number tends to increase with annealing time. The results of this study suggested that Si diffusion of implanted dopants was likely contributing to the increase in measured sheet number despite previous reports regularly reporting limited Si diffusion.[98], [115], [145] Based on this observation, assumptions of limited diffusivity from the results of previous experimenters may not be valid for the longer annealing times and higher temperatures used in the time dependent activation study. In order to have a better estimate of active Si concentration, the post-anneal dopant profiles were measured using SIMS. It is

apparent form Figure 4-12 that for anneals over 5 s at 750°C there is a significant amount of diffusion occurring. This results in more of the dopant profile being under the previously established solubility limit, which results in the higher active sheet numbers with increased diffusion. Figure 4-13 shows the effect that annealing time has the post anneal Si active concentration for a 10 keV, 5×10^{14} cm^{-2} Si^{+} implant at 80°C calculated with the method detailed in section 4.5.

Figure 4-13 indicates that the measured carrier concentration for the Si implanted InGaAs was relatively constant as a function of annealing time and limited to approximately 1.5×10^{19} cm^{-3}. Similar to the 750°C 5 s annealing treatment used in 20 keV 6×10^{14} cm^{-2} Si^{+} implants at 80°C in this work. A second set of samples with the same 10 keV, 5×10^{14} cm^{-2} Si^{+} implant at 80°C were also annealed for much longer times in a tube furnace at temperatures ranging from 550°C to 750°C and the active Si concentration based on Hall effect and SIMS for these samples is shown in Figure 4-14. Active Si concentration is shown to be independent of annealing temperatures, unlike many implanted dopants. For many dopant-semiconductor systems the solubility of a dopant can be increased by annealing at higher temperatures but for the Si-InGaAs system it appears that the active carrier concentration behaves as a limit regardless of annealing temperature. As a result, there appears to be no evidence for metastable or temperature–dependent activation limits of ion implanted Si in InGaAs based on this preliminary study. Furthermore, the stable activation limit of $\approx1.5\times10^{19}$ cm^{-3} that is achieved is lower than what is commonly achieved with MBE doping.

4.7 Si Diffusion in InGaAs

The evidence of Si diffusion of ion implanted InGaAs in this work presents a large deviation from previous experiments looking at Si implants in InGaAs. Prior reports indicate that limited Si diffusion occurs in ion implanted InGaAs and experimenters have commonly assumed limited Si diffusion in these materials.[98], [115], [145] The focus of this work is in large part on the electrical activation behavior but because the active concentration in these implants is closely related to the amount of Si diffusion observed in these implants a discussion of the observed Si diffusion behavior is necessary.

It is quite obvious from the post anneal profiles shown in Figure 4-12 that the nature of the diffusion of Si in InGaAs is not Fickian. Fickian diffusion is governed by a constant diffusivity for all Si concentrations. Instead, the observed shouldering of the post anneal Si concentration profile is evidence of heavily concentration dependent diffusion where high Si concentrations diffuse much faster than low concentrations. Concentration dependent diffusion has been observed in other dopant-semiconductor systems but the experiments performed as part of this work are the first evidence of concentration dependent diffusion occurring for ion implanted Si in InGaAs.[230] In fact, from these profiles it is easy to see why previous implants may not show this diffusion given that previous studies have peak Si concentrations below the Si concentrations required for heavily concentration dependent diffusion.

For concentrations below 3×10^{19} cm^{-3} Si diffusion is shown to be negligible. But concentrations above this value it is shown that Si diffuses quite rapidly. The observed Si diffusion is similar to some of the concentration dependent behavior observed for As and P dopants in Si.[231] The diffusion results also illuminate some of the activation results. The plateau concentration of 3×10^{19} cm^{-3} is still higher than the active

concentration observed in these profiles but these results indicate that Si concentrations above 3×10^{19} cm^{-3} are mobile in InGaAs. The fact that Si is mobile at these high concentrations also suggests that the limited activation is not due to clustering. In general, clusters have limited diffusivity in a solid and often result in large peak concentrations that end up immobile for dopant concentrations high enough to exhibit clustering, as is the case of B in Si.

Any proposed electrical compensation mechanism must explain the observations of Si diffusion and activation of Si in InGaAs. One component of the activation/compensation is that the observed compensation occurs via a mobile yet inactive Si configuration. It is commonly assumed in Si that dopants that are mobile are active yet it is clear from these experiments that Si concentrations above 3×10^{19} cm^{-3} are inactive yet mobile. For concentrations between 3×10^{19} cm^{-3} and 1.5×10^{19} cm^{-3} it appears that the Si is compensated with a reduced diffusivity relative to Si concentrations above 3×10^{19} cm^{-3}. At concentrations below 1.5×10^{19} cm^{-3} Si is an active donor with limited diffusivity. One possible explanation for the observed behavior is the presence of negatively charges group III vacancies (V_{III}^{3-}). Previous DFT results have shown that at high n-type doping levels the energy required to create negatively charged vacancy defects drops significantly.[232], [233] This would also explain why a likely vacancy diffuser such as Si shows such concentration-dependent behavior. At high doping concentrations where the Fermi level is near or in the conduction band there will be a large number of vacancies present in the material that contribute the enhanced diffusion. As the Fermi levels shifts due to dopant diffusion the vacancy concentration decreases to the point that the Si diffusivity slows considerably.

Limited Si diffusivity for concentrations between 3×10^{19} cm^{-3} and 1.5×10^{19} cm^{-3} may indicate that Si is in a compensated defect configuration with a more limited mobility such as the Si-Si next nearest pair, Si_{As} occupation or that other point defects at this concentration which give rise to the observed diffusivity are constantly forming and recombining such that Si has no appreciable diffusivity. At concentrations below the activation limit Si exists on group III sites and is expected to have limited diffusivity relative to other Si configuration based on DFT results of Si in GaAs.

4.8 Stoichiometry Effects (Co-Implants) on Si Activation in InGaAs

4.8.1 Previous Co-Implant Experiments into III-V's

Si implants into InGaAs have thus far been shown to activate to maximum concentration of 1.5×10^{19} cm^{-3} independent of implant conditions and activating anneal conditions. Previous authors have concluded that the amphoteric nature of Si dopants may be part of this reason due to Si_{As} sites compensating Si_{III} sites or even the formation of Si-Si next nearest neighbor neutral pairs. Heckingbottom and Ambridge proposed the idea of co-implantation as a means to control the site stoichiometry of implanted dopants.[128], [234] Originally this idea was applied to group II and group VI dopants where excess group III or V dopants were also implanted to preserve the ratio of species occupying group III- to species occupying group V sites.[125], [208], [235]-[239] Eventually, more experimenters have applied this technique to amphoteric dopants such as C and Si in GaAs and InP. Most of these studies report some improvement in activation from the addition of a co-implant species. However, many of these studies fail to separate damage effects from chemical effects. This is obvious in the study done by Moll et al. in which co-implant species with carbon increased the activation of C in GaAs.[96], [143] Moll also showed that even inert gas implants had the

effect of increasing C activation suggesting that damage also played a role in increasing the C activation observed in co-implantation. Carbon is p-type in GaAs but it also shows relatively little activation. Studies of As co-implantation with Si in GaAs showed that saturation of Si activation occurred at a Si doping concentration of 2×10^{18} cm^{-3} [227] with Si despite other studies indicating that P co-implantation improves Si activation in GaAs.[240]-[242] Studies of P and Si and P and Ge co-implants into InP and InGaP have also showed improvements in activation of amphoteric dopants as well[243]-[246] but III-V phosphides commonly exhibit order of magnitude better n-type dopant activation than III-V arsenides.

There are a few ways to interpret the previous co-implant results into GaAs and InP. It is not surprising that p-type co-implants generally report better activation, as the increased damage from a co-implant is likely to increase the measured p-type activation for GaAs, and InP. Of the previously reported studies on n-type co-implants, only one reports that there is no effect on Si activation.[227] However, most of these studies cannot prove that there is indeed a chemical effect from co-implantation. Only one of these studies of Ge in InP shows enhanced activation of amphoteric dopants and a corresponding increase in group III lattice site occupation by germanium.[172] Furthermore, some studies also exhibit contradictory behavior to what is expected from a chemical effect.[247] More generally, these studies also fail to account for microstructural changes in the implanted substrates as some implant and co-implant doses move into the amorphizing regime and generally fail to explore the whole phenomenon of co-implantation and instead focus on either group III or group V co-implants.

4.8.2 Design of Co-Implant Experiments for this Study

In order to separate chemical effects from damage effects, the study devised for this works uses co-implants from multiple groups of the periodic table. Comparing group V, P co-implants to group III, Al co-implants tested the chemical effect of co-implants with Si implants into InGaAs. Damage effects were created by co-implanting Ar along with Si. The implantation of Si and S, which should provide a co-implant effect but also act as donors was performed to test if the maximum electrical solubility of dopants is an additive effect of individual dopant species active concentrations. The evidence of a chemical effect due to co-implantation should also be more pronounced by varying the dose of the co-implant whereas previous studies generally used a single co-implant dose. For this study a high dose Si^+ implant of 6×10^{14} cm^{-2} at 20 keV was used and additional Ar^+, P^+, and Al^+, and S^+ co-implants at varying doses from 3×10^{13} cm^{-2} - 1×10^{15} cm^{-2} were performed along with controls of 20 keV, 6×10^{14} cm^{-2} at Si^+ and S^+ implants with no co-implant dose. Co-implant energies were chosen such that the peak of the co-implant as predicted by SRIM was co-incident with the peak of the implanted Si profile as shown in Figure 4-15. In the case of Al^+, P^+, and S^+ co-implants, an implant energy of 20 keV was used however in the case of the Ar^+ implants, a co-implant energy of 27 keV was used. All of these implants were performed at 100°C as well to prevent any amorphization such that the comparison between all of these samples was for strictly non-amorphizing conditions. Two sets of anneals were also performed for the samples used in these experiments. Short, 5 s RTA anneals at 750°C anneals which have been shown to limit diffusion and prove good activation were compared with longer annealing times at 750°C in order to cause significant diffusion of Si. Table B-5 in

Appendix B includes a complete listing of the implant and annealing conditions for all of the co-implant samples detailed in section 4.8.

4.8.3 Al^+, P^+ and S^+ Co-Implants with Si^+

The active sheet number of varying co-implant dose of Al^+, P^+, and S^+ with a fixed 6×10^{14} cm^{-2} Si^+ implant dose are shown after a 750°C 5 s RTA in Figure 4-16. Short, 5 s RTA anneals of P^+ co implants are shown to result in no significant increase in post anneal sheet activation numbers above those of Si alone. For 5 s anneals at 750°C, Al^+ implants are shown to exhibit the expected co-implant or damage behavior with increasing Al co-implant dose resulting in reductions in active sheet number. Activation of S and Si implants and P and S similarly show no increase in activation from co-implantation. This result is especially surprising given that both Si and S are n-type dopants and it may suggest that the active concentrations of two different dopants is not additive in the implanted material. Ten minute furnace anneals were also performed on similar sets of implanted samples and the activation of these samples is shown in Figure 4-17.

After annealing for 10 minutes, the electrical activation trends for S^+ and P^+ co-implanted samples are the same as observed after 5 s anneals at 750°C although the active sheet numbers are much higher presumably due to diffusion of Si into the InGaAs bulk, which will be discussed in subsequent sections. Al^+ and Si^+ co-implants exhibit similar behavior to P^+ and Si^+ co implants after 10 minute anneals and as a result these longer anneals contrast the earlier evidence for short anneal times of a co-implant effect. There are a few possible explanations for the observed behavior of Al^+, P^+ and Si^+ co-implants at short and long annealing times. One possible explanation is that in

the case of Si^+ and P^+ implants any damage effect is perfectly compensated by an enhancement in activation. This damage limited activation interpretation also seems unlikely given that damage would be perfectly compensated over such a large dose range but also because Si^+ and S^+ co-implants are limited to the exact same activations despite S increasing the implant damage but also being an n-type dopant in InGaAs. The results of intermediate temperature implantation of Si alone also indicate that non-amorphizing damage also promotes Si activation in InGaAs. A second, more plausible, explanation is that the excess implanted aluminum prefers to occupy group III sites and in the process prevents Si from moving onto group III sites to become active. Previous work also indicates that cation vacancies (V_{III}) might be the important diffusing species in InGaAs. As such, the reduction in group III vacancies available to Si due to Al co-implants will prevent Si from moving onto lattice sites and activating and may inhibit diffusion of Al or Si for short anneal times. As more of the Al finds a way onto group III lattice sites, Si dopants have less competition and can move onto lattice sites which will result in activation and diffusion. This results in Si incorporation to the same maximum sheet number once Si diffusion occurs. In the case of P and S there is no site competition since Si prefers the group III site and the activation saturates for the short anneals. P^+ implants, which are expected to contribute to enhanced activation due to a chemical effect, show no significant improvement in activation over the dose range studied for both high dose and low dose Si^+ implants. Al^+ implants however seem to exhibit a chemical effect with increasing Al co-implant dose resulting in reduces activation post anneal for the previously stated reason it seems unlikely that the reason for reduced activation in Al^+ implanted samples is due to a damage effect. But for the

reason mentioned above but it is still unclear what effect, if any, implant damage from co-implant species has on Si activation since Si^+ implants with P^+ and S^+ thus far have all resulted in maximized carrier concentrations regardless of co-implant dose for long and short anneal times.

4.8.4 Ar^+ Co-Implants with Si^+

Electrically inactive Ar^+ implants, which should not have a site preference or become substitutional, were expected to show how ion damage alone affects Si activation in InGaAs. It is immediately obvious from Fig. 4-18 that Ar implants reduced Si activation in both cases even after longer furnace annealing times. For the 5 s RTA anneal at 750°C Ar^+ and Al^+ implants behave with similar trends but after longer furnace annealing time of 10 minutes Si activation in Ar^+ implanted samples exhibits reduced activation unlike any other co-implant species tested. This might suggest that there is to some extent a damage effect that reduces Si activation but other possible explanations exist as well. One possibility is that Ar is significantly reducing the diffusion of Si at long and short anneal times and the diffusion of Si in the presence of Ar is explored more thoroughly in section 4.8.7.

4.8.5 Al^+ and P^+ Co-Implants with S^+

In order to better replicate the original co-implant proposals by Ambridge and Heckingbottom similar experiments were performed with Al^+ and P^+ co-implants with S^+ dopants. S was chosen since it a group VI dopant with a mass close to that of Si to reduce possible difference in implant behavior that could arise form damage effects. The previous study of S^+ implants and Si^+ implants alone indicated that S^+ implants alone result in lower active sheet carrier numbers and would potentially be more susceptible to increases in activation from co-implant because of this. Figure 4-19

shows the result of 10 m furnaces anneals at 750°C for 20 keV Al^+ and P^+ co-implants with at fixed 20 keV 6×10^{14} cm^{-2} S^+ implant. These results are consistent with previous results of so-implants in Si indicating that co-implantation of both Al^+ and P^+ has no discernable effect on increasing the n-type doping of S^+ implants into InGaAs

4.8.6 Summary of Co-Implant Activation Behavior

Despite many previous experimenters suggesting that co-implantation is a viable route to achieved enhanced activation of dopants into III-V's there is limited evidence to suggest that this technique will be successful in creating more heavily doped junctions in InGaAs based on the experiments performed in this work. The results of this experiment most closely emulate the results of Banwell et al. who observed maximized activation of Si implants into GaAs not far from what is generally reported at the implanted active carrier limit in GaAs.[227] There are a few possible interpretations for the deviation of the results in this work with much of the previous results of co-implantation in III-V materials.

In the case of C, co-implants into GaAs and InAlAs and InGaAs have shown to increase activation of C but unlike Si, C is p-type and generally shows very limited activation in these materials.[144], [248] C implants generally show percent activations an order of magnitude lower than that of Si in these same materials for similar implant conditions and annealing times. This result suggest that C dopants are more amphoteric in the studied materials systems. InP and InGaP materials exhibit more gains in n-type activation from co-implantation than has been observed in the III-V arsenides. However, it is well known that the n-type solubilities of dopants in III-P materials are an order of magnitude higher in the 10^{20} cm^{-3} range in contrast to III-As which generally exhibit maximum carrier activation in the 10^{19} cm^{-3} range. In this case, it may be possible to

achieve enhanced activation from co-implants because the studied conditions were farther away from the maximum activation limit. This may suggest that intrinsic limitations in in maximum doping in these materials are due to thermodynamic limits and not limitation in site stoichiometry due to the amphoteric nature of Si dopants themselves. As a result co-implantation will become decreasingly effective as the carrier concentrations move closer and closer to the maximum thermodynamic limits of Si incorporation. The Si^+ doses used in this study already exhibit a large amount of compensation suggesting that the thermodynamic limit is easily reached by a single, high dose Si^+ implant. From a technological standpoint, it stands to reason that co-implants are probably not worth the effort even if lower Si doses that were not already heavily self-compensated had a more pronounced co-implant effect since Si^+ implants alone can already activate to the maximum activation levels of Si^+ and P^+ and Si^+ and S^+ co-implants.

4.8.7 Co-Implant Diffusion

Previous co-implant results generally only report activation numbers and do not take into consideration the possible effects that co-implantation may have on diffusion. Up to this point only sheet activation has been considered since post anneal diffusion results are required to make an estimate of carrier concentration once negligible diffusion can no longer be assumed. The observation of diffusion in the Si-InGaAs system also has important ramifications on the usefulness of previous co-implant studies which never monitored diffusion.

Figure 4-20 compares the post anneal diffusion of the highest dose 6×10^{14} cm^{-2} Al^+ and P^+ implanted samples after a 5 s RTA at 750°C. Comparison of the Al^+ and P^+ co-implants shows that Al^+ co-implants are impeding the diffusion of Si relative to P^+

implants which is consistent with the previous interpretation of the resultant reduction in activation from Al^+ co-implantation being due site competition between Al and Si for group III-vacancies. In the case of Al^+ implantation after annealing for 5 s there appears to be no discernable drop in profile peak whereas P^+ implants show the onset of the previously observed shouldering behavior. This may suggest that the excess Al are preferentially substituting on group III lattice sites which may prevent Si diffusion and result in the lower active sheet numbers observed in Figure 4-16.

Figure 4-21 shows the post anneal SIMS for the 10 m, 750°C furnace anneals of 6×10^{14} cm^{-2} Al^+, P^+ co-implants with Si^+ as well as the diffusion of Si alone. It is shown that Si implants alone actually exhibit slightly more diffusion than of Al^+ and P^+ co-implanted Si, which show similar amounts of diffusion. One possible reason for this is that increased damage from the co-implant results in a higher number of interstitials that interact with diffusing Si-V complexes and impedes diffusion of Si in InGaAs which supports previous results that indicate Si diffuses via a vacancy mechanism. There is no obvious enhancement to diffusion from a co-implant suggesting that any co-implant effect that may exist is not strong enough to significantly alter the concentration dependent diffusion behavior of Si in InGaAs for very heavily Si-doped substrates. Based on the post anneal SIMS and sheet number measured by Hall effect, the maximum active carrier concentration for the Al^+ and P^+ co-implants is limited to 1.6×10^{19} cm^{-3}. As a result, it appears that co-implantation in these materials is either an ineffective means of changing site stoichiometry or that compensation at very high Si concentrations is not well explained by amphoteric site selection of Si in InGaAs.

Figure 4-22a shows the post 10 m anneal SIMS for Si in Ar^+ co-implanted InGaAs. It is immediately obvious that Ar is impeding Si motion even with extended anneal times which were shown to cause significant diffusion from 6×10^{14} cm^{-2} Al^+ and P^+ co-implants. Ar^+ implants should be more damaging than those of Al^+ and P^+ given that the atomic mass of Ar is 39 compared to Al and P with atomic masses of 27 and 31. The increase in atomic mass is seemingly too small to create such a large discrepancy between the diffusion of Al^+ and P^+ co-implanted samples and Ar^+ co-implanted samples. This result seems to suggest that Ar^+ implants, while chemically inert, may have some interaction with diffusing Si dopants or Si defect complexes. It is well established that inert gas implants tend to cause bubbling upon annealing but the doses required for this are usually in the range of 1×10^{15} cm^{-2} to 1×10^{16} cm^{-2}. Ar^+ implant doses for this experiment were limited to 6×10^{14} cm^{-2} to preclude the possibility of bubbles affecting the InGaAs microstructure and subsequent activation or diffusion results. Furthermore, inert gasses are unable to become substitutional and prevent Si diffusion by occupying sites necessary for Si diffusion. Further study is required to know exactly what is occurring in the case of Si^+ and Ar^+ co-implantation but it is apparent from activation results in Figure 4-22b that the reduction in diffusion results in reductions in maximum carrier concentration. Other implants systems such as C in Si have been used to reduce diffusion of B or other dopants but in the case of Si implants into InGaAs it seems that the large reduction in activation limits the usefulness of the observed effect but it is an interesting result no-less. In this case, it is likely fair to say that inert dopants might not be great analogs to approximate the effect of damage alone on activation as was assumed in this experiment and by other experiments.

Unfortunately, III- V materials lack good analogs such as Si or Ge implants into Si. It seems that experiments wishing to more carefully introduce damage into a lattice without a chemical effect should choose equal doses of constituent group III and V atoms in this material.

4.8.8 Discussion of Co-Implant Results

Direct observation of lattice site location would be the best evidence for the presence of a co-implant effect but the challenges associated with observing lattice site location of dopants in this system as discussed in section 2.6.4 limit the ability to determine the efficacy of co-implants at changing site location. Most previous studies also lack any sort of direct site evidence in a co-implant scenario and instead report back sheet numbers. There are a few possible reasons for the discrepancies in activation in this study and previous co-implant studies that generally report that co-implantation can improve the n or p-type activation of implanted dopants into III-V materials. One possibility is that the actual co-implant could change the diffusion behavior of the implanted dopants. In the case of Be dopants with P co-implants, the additional implant of P will create more interstitials and Be is known the be an interstitial diffuser.[235], [237] In this case, the increasing flux of interstitials may contribute to enhanced Be diffusion. The increased diffusion leads to more broadening of the profile compared to the single implant case and results in higher measured sheet numbers. Another possibility is that the implanted doses result in different compensation regimes. For low doses with peaks below the implant solubility, co-implantation may be of some benefit to change site stoichiometry but these implanted doping concentrations are not heavily compensated. As a result co-implantation may be useful in achieving increased activation of Si at low Si doses but higher activation in implanted regions could be easily

achieved by just implanting larger Si does in these cases such that the implant peak is near the electrical activation limit of 1.5×10^{19} cm^{-3}.

The lack of direct site evidence of Si occupation makes it impossible rule out the presence of a stoichiometry effect in this study but it is obvious that co-implantation cannot result in higher active concentrations than $\approx1.5\times10^{19}$ cm^{-3} and that any stoichiometry effects are compensated by another mechanism. The evidence for this is especially apparent in the Si^+ and S^+ co-implants. S^+ implants alone show an active carrier concentration of 5×10^{18} cm^{-3} in InGaAs once diffusion is accounted for, but the summation of the Si and InGaAs is still limited to the Si solubility of 1.5×10^{19} cm^{-3}. Furthermore, it would be quite serendipitous, in the case of Si and P implants, that implant damage from P would exactly cancel out any subsequent co-implant effect. These results suggest that co implants are unable to influence site stoichiometry at high doping levels or that the observed compensation of dopants is not due to site selection issues but is instead governed by a thermodynamic limit for Si dopant incorporation in InGaAs.

4.9 Electrical Activation of Si Implants into InAs Characterized by Raman

There are limited accounts literature of quantitative measurements of activation of shallow Si implants into InAs. Van der Pauw Hall effect measurements are frequently used to measure the active dose of implanted semiconducting materials after thermal treatment but Van der Pauw Hall effect measurements of shallow implants into bulk InAs performed in this work and in previous work[249] showed no discernable activation beyond the background p-type doping of the sample presumably due to junction leakage.[250] Other reports of surface inversion layers of InAs have resulted in

measurement complications for InAs heterostructures as well.[251] The attempts to measure activation in this work via Hall effect resulted in no observation of Si activation, consistent with attempts by previous experimenters.[249] The reported complications of measuring electrical activation of implanted dopants into InAs via Hall effect may explain the lack of previous reports of dopant activation despite n-type implants being performed in earlier works. For this reason, non-contact optical methods of carrier determination were used to measure how Si activation proceeds over a range of annealing times and temperatures.

Previous authors have used Raman scattering to measure free carrier concentrations making use of the fact that LO phonons will readily couple with the plasma oscillations of free carriers in InAs and other polar, III-V materials. [200], [201], [221], [228], [229], [252]-[255] The L_+ phonon-plasmon coupled mode is especially sensitive to changes in the carrier concentration at high n-type carrier concentrations in InAs where shifts towards higher wavenumbers correspond to increasing free electron concentrations.

20 keV, Si^+ over a range of doses from 1×10^{13} -1×10^{15} cm^{-2} were implanted into lightly doped (001) p-type InAs. Additionally, the implants were performed at 100°C to prevent amorphization. A table detailing the complete implant and anneal conditions for all of the samples presented in the work included in section 4.9 is given in table B-6 of Appendix B. Figure 4-23 shows the post implant microstructure observed in cross sectional transmission electron microscopy indicating that the crystallinity of the InAs was preserved. This result is consistent with other reports that the threshold dose for amorphization of InAs is above 1×10^{15} cm^{-2}.[67], [68] The stopping range of ions in

matter (SRIM) was used to estimate the peak Si concentrations for the variable dose, 20 keV Si implants and is shown in Figure 4-23b. All samples were encapsulated with 15 nm of Al_2O_3 deposited at 250°C via atomic layer deposition (ALD) after ion implantation to prevent surface degradation upon subsequent annealing treatments. Halogen lamp rapid thermal annealing at temperatures ranging from 400-700°C and annealing times of 1-90 s were used to activate the implanted Si. Raman spectroscopy for this study was performed with a 532 nm laser. The probing depth at this wavelength (1/2α) was calculated to be 21.4 nm based on the data for InAs collected by Aspnes et al. [256] The projected range of the implant is calculated to be 26 nm such that the probing depth of the laser is in the heavily doped, ion-implanted region and not the bulk of the implanted material. Correlation of the peak shift of a L_+ phonon-plasmon mode to active carrier concentrations measured by Hall effect on MBE grown n-InAs on GaAs by Li et al.[255] was used to estimate the maximum active carrier concentration for the implants of Si into bulk InAs in this work

Figure 4-24a shows the Raman scattering intensity as a function of wavenumber for the L_+ coupled mode for 30 s anneals ranging from 400-700°C for the 20 keV 1×10^{15} Si^+ implants. The L_+ phonon-coupling mode is shown to shift towards higher wavenumbers with increasing annealing temperature. Figure 4-24b more clearly shows the peak shift of L_- and LO modes with increasing annealing temperature. Annealing temperatures below 500°C result in no significant L_+ peak shift over that of the as implanted or as grown wafer indicating that temperatures of 500°C or more are required to result in significant activation of the implanted dopants. There is a peak shift of the L_- mode indicating that temperatures as low as 400°C will result in activation of implanted

dopants. While the L_+ mode is more sensitive at high carrier concentrations the measured intensity of the L_- and LO modes is generally 10 times that of the L_+ peak for the obtained spectra.

The measured peak shift of the L_+ coupled mode for the 30 s anneal at 700°C is shown to be approximately 1660 cm^{-1}. The estimated active carrier concentrations in these samples based on the results by Li et al. are shown in Figure 4-25. The highest annealing temperature of 700°C resulted in an estimated peak concentration of 4.9×10^{19} cm^{-3}. Figure 4-26a and Figure 4-26b show the effect of implanted Si dose on electrical activation for a 30 s, 700°C RTA. The L_+ peak shift is shown to move toward higher wavenumbers with increasing implant dose indicating that higher implant doses resulted in higher active carrier concentrations. The lowest dose, 1×10^{13} cm^{-2} implant, shows no evidence of n-type activation but this result is unsurprising given that the peak Si concentration in this case is roughly 2.3×10^{18} cm^{-3} but the background p-type concentration of the InAs is 3×10^{17} cm^{-3}. This result indicates that a 30 s RTA was insufficient to activate enough of the implanted dopants to overcome the background p-type doping. The estimated carrier concentration for the variable dose implants annealed at 700°C for 30 s is shown in Figure 4-27. An isothermal annealing experiment with times ranging from 1-90s was also performed for varying anneal temperatures for the 1×10^{15} cm^{-2} dose implant and the L_+ peak shifts as a function of annealing time of this study are shown in Figure 4-28. The longest annealing time of 90 s resulting in a peak shift of 1720 cm^{-1} which corresponds to an active carrier concentration > 5×10^{19} cm^{-3} based on the results of Li et al. The estimated active carrier concentration for the isochronal annealing from 1-90 s is shown in Figure 4-29 and

increasing annealing times at 700°C are shown to steadily increase the free carrier concentration.

Activation of implants with annealing temperatures above 400°C are consistent with reports that these annealing temperatures are required to recover damage due to ion implantation and cause subsequent movement of dopants onto lattice sites.[57] Previous studies have indicated that anneals above 600°C result in conversion from n-type activation of Ge and Si implants to p-type in InAs[249] based on photoluminescence results. These earlier results seem suspect given that no type conversion was observed based on the Raman shift in this work and may indicate that at high annealing temperatures surface degradation or some other effect may have lead to the observed peak shift in the photoluminescence spectra.

The maximum reported activation for growth-doped InAs substrates is reported to be 6-12×10^{19} cm^{-3} [257], [258] and the activation of 20 keV, 1×10^{15} cm^{-2} after a 90 s, 700°C RTA is shown in this work to activate to 5×10^{19} cm^{-3} or more based on the calibrations in the report by Li et al. The observation of decreased activation for implanted material relative to growth-doped material by other experimenters is consistent with the observation of Si implants into InGaAs and implants of dopants into III-V's.

Prior MBE experiments report that the background Si doping in InAs was >1×10^{20} to create layers with active carrier concentrations of 6×10^{19} cm^{-3} indicating the presence of a large amount of inactive Si.[257] The peak concentration for the various implant doses in this work were estimated using SRIM and are shown in Figure 4-23. The highest implant dose of 1×10^{15} cm^{-2} results in a peak Si concentration of 2.3×10^{20} cm^{-3},

which is much higher than the observed Si activation level of ≈ 5×10^{19}. If minimal Si redistribution upon annealing is assumed, the large difference in active concentration and the implanted peak concentration suggests that a large amount of Si is inactive after implantation and annealing similar to the observed behavior for Si^+ implants into InGaAs. The activation levels observed in this report are is still significantly higher than the activation levels achieved by previous S monolayer doping experiments which resulted in a estimated carrier concentration of 8×10^{18} cm^{-3} [259] suggesting implantation is an effective means to create heavily doped InAs.

The electrical activation results of Si in InAs are consistent with the behavior observed for Si implants into InGaAs with large portions of implanted dopants likely remaining inactive. In general, it seems Si dopant behavior in the III-arsenides is consistent despite each material having slightly different maximum activation levels. No discussion of Si diffusion in InAs is presented in this work so it is not possible to compare the diffusion behavior of Si in InAs to that of Si in InGaAs but the parallels in the activation behavior suggest that the fundamental limiting mechanisms in InGaAs are the same limiting mechanisms in GaAs and InAs.

4.10 Summary and Discussion of Electrical Activation of Si implants in InGaAs and InAs

Any attempt to explain the maximum electrically active Si concentrations in InGaAs must take into account some of the experimental observations in this work related to diffusion and maximum activation of Si. Historically, there have been a number of explanations for the low achievable active carrier concentrations in implanted GaAs and InGaAs relative to Si but the holistic nature of this study allows us to examine many of the previously advanced theories in light of the experiments performed in this

work. In the case of amphoteric dopants such as Si, the low active concentrations are generally attributed to the self-compensation of these dopants by previous experimenters.

For amphoteric limited activation, Si occupation on donor sites would saturate to a point that Si incorporation onto acceptor sites began to take over. Previous experimenters have shown that it may be possible to cause amphoteric dopants to preferentially occupy group III or group V sites with co-implantation in some III-V systems[172], [173] but direct evidence of this is this difficult, if not impossible to verify experimentally in the Si-InGaAs system. Instead, there is only indirect evidence of electrical activation. Co-implantation in this study did not result in any increased activation, however. One potential reason for the observed activation is that co-implants are completely ineffective at changing site selection. This interpretation does not seem likely given that the comparison of Al^+ and P^+ co-implants result in different activation numbers for short anneal times and this may suggest that there is competition between Si and Al for group III sites. A second interpretation is that damage effects are causing a reduction in activation that is equal to the increase in activation from co-implantation. This interpretation is also seemingly unlikely since if this were the case it would be highly coincidental that Al implants would contribute damage and a co-implant effect resulting in deactivation, but P implants result in a co-implant effect that is perfectly compensated by the increase in damage over a wide range of co-implant doses. Similarly, increasing non-amorphizing damage was shown to actually improve Si activation for intermediate temperature anneals. Ar^+ implants may be the best evidence to suggest that damage can limit activation but the drastic effect that Ar^+ implants have

on Si diffusion and activation are not commensurate with the increase in atomic mass relative to damage occurring from Al^+ and P^+ implantation. This discrepancy may suggest that Ar^+ implants are not as “inert” as previously thought and that Ar may be fundamentally changing a given dopant’s diffusion in this system due to a more complex interaction with Si or the point defect species which modulate Si diffusion in InGaAs. A third possibility is that there is limited chemical solubility at high Si concentrations that result in some form of dopant clustering or interstitial Si configuration becoming preferential. Si clustering is also seemingly unlikely given that classic signs of chemical solubility including increased solubility with increased annealing temperatures or the presence of immobile dopants in diffusion studies are not observed. In fact, Si is shown to be most mobile when heavily compensated and RBS/PIXE studies of Si in GaAs have indicated that Si is mostly substitutional.[159]

Of the previously advanced theories only one remains and it also seems the most likely given the deficiencies of the amphoteric limited, solubility limited and damage limited activation interpretations in explaining the observed activation and diffusion behavior of the studied dopants in InGaAs. The presence of large concentrations of point defects can explain more of the observed n-type activation limits and diffusion behavior of Si implants in InGaAs. One important observation is the prevalence of concentration dependent diffusion of Si in InGaAs. Theoretical predictions indicate that at very high doping levels the formation energy of group III vacancies becomes smaller and smaller in most III-V systems.[260]-[262] The presence of these vacancies more readily explains the enhanced diffusion of Si at high concentrations, and the fact that Si is mobile, yet inactive for chemical concentrations above 3×10^{19} cm^{-}

^{3}. In the point-defect limited case it may be expected that a co-implant effect could become ineffective at high doping concentrations since the creation of more Si donors would be immediately compensated by the simultaneous creation of more electrically compensating defects. This limiting mechanism also agrees well with the non-additive nature of Si and S implants since the creation of compensating defects is related to the background electrical activation and not a dopant specific limit. A similar application of this interpretation to the P co-implant result would be that even though Si and S are both active as dopants and may presumably have a co-implant effect as well as additional donor effect, the creation of more negatively cation vacancies which readily complex with positively charged donor configurations of dopants results in limited activation in the material in the presence of Si and S due to a crystalline thermodynamic limit.

The question still remains as to whether it is possible to improve the electrical activation of Si in InGaAs given that MBE doped InGaAs often show much higher electrical activations than implanted InGaAs. From the arguments above it seems unlikely that the reason for this difference is due to damage from implantation but rather it is due to a thermodynamic limit to dopant activation. It is well established that MBE can be used to perform non-equilibrium dopant incorporation and this fact is easily illustrated by studies which have made p-n junctions in GaAs using only Si as a dopant but studies of Si implants result in consistent observation of n-type behavior. As a result, it appears that incorporation method may have a large role in determining the final active carrier concentrations for given dopants. Implantation of dopants into a semiconductor crystal is decidedly non-equilibrium and non-conservative in nature but

the atomic process by which dopants move onto lattice sites in the case non-amorphizing implants is requires equilibrium diffusion from some sort of activating anneal.

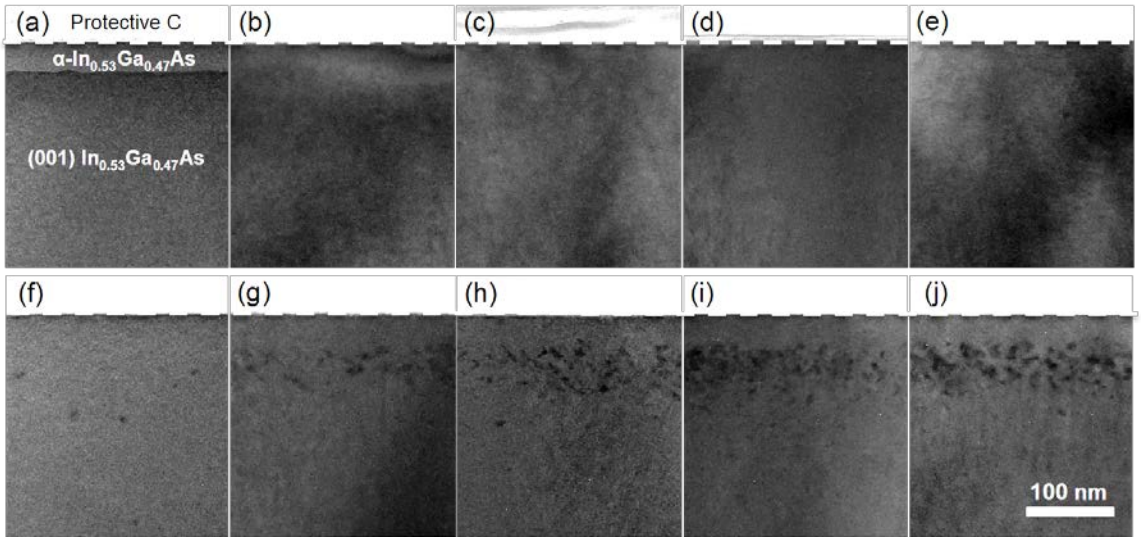

Figure 4-1. Micrographs showing the effect of implant temperature on amorphization threshold and defect evolution. Micrographs are of post-implant XTEM of as-implanted 20 keV, 6×10^{14} cm^{-2} Si^{+} at implant temperatures of (a) 20°C, (b) 80°C, (c) 140°C and (d) 200°C and (e) 300°C. as well as post 750°C 5s RTA of 20 keV, 6×10^{14} cm^{-2} Si^{+} at implant temperatures of (f) 20°C, (g) 80°C°, (h) 140°C and (i) 200°C and (j) 300°C. These micrographs indicate that implantation at 80°C is sufficient to avoid amorphization for the 20 keV, 6×10^{14} cm^{-2} Si^{+} implant. Post anneal micrographs show that these implants result in a large number of loop defects in the non-amorphizing case.

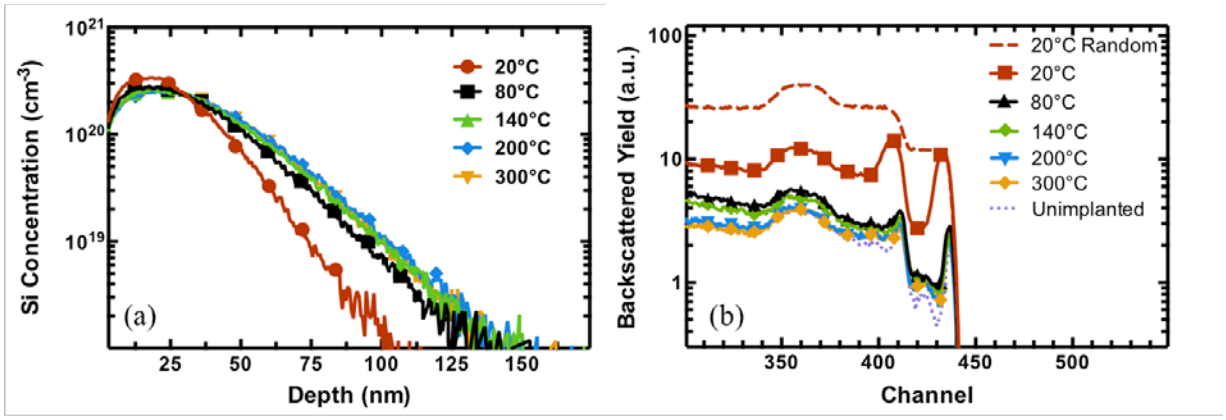

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Figure 4-2. As-implanted SIMS and RBS channeling for variable temperature Si implants into InGaAs. As-implanted SIMS(a) and (b) RBS/C(b) for 20 keV, 6×10^{14} cm^{-2} Si^{+} implanted at temperatures of 20°C, 80°C, 140°C, 200°C and 300°C indicate that implant temperatures above 80°C are sufficient to prevent amorphization.

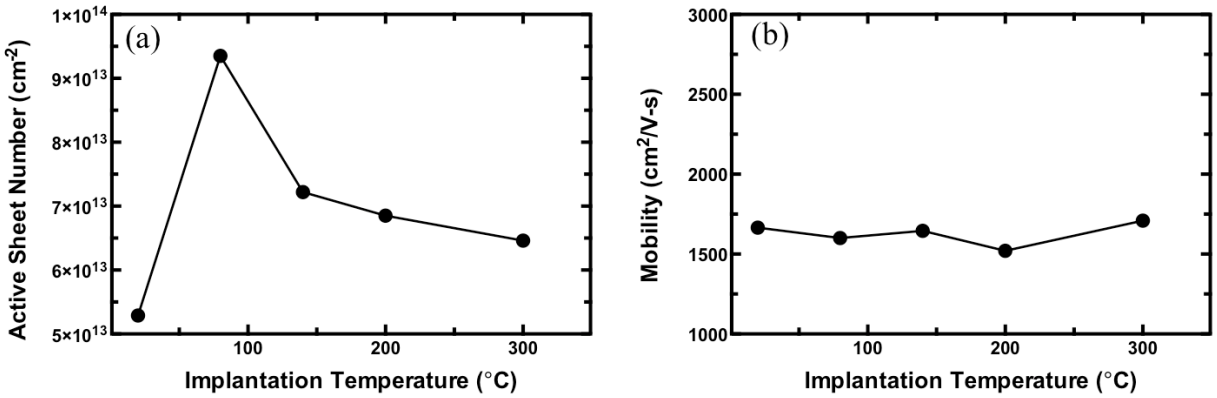

Figure 4-3. Plots of activation and mobility as a function of implant temperature. Measured values of (a) sheet number and (b) mobility are for a 20 keV, 6×10^{14} cm^{-2} Si$^+$ implant as a function of implantation temperature after annealing at 750°C for 5 s

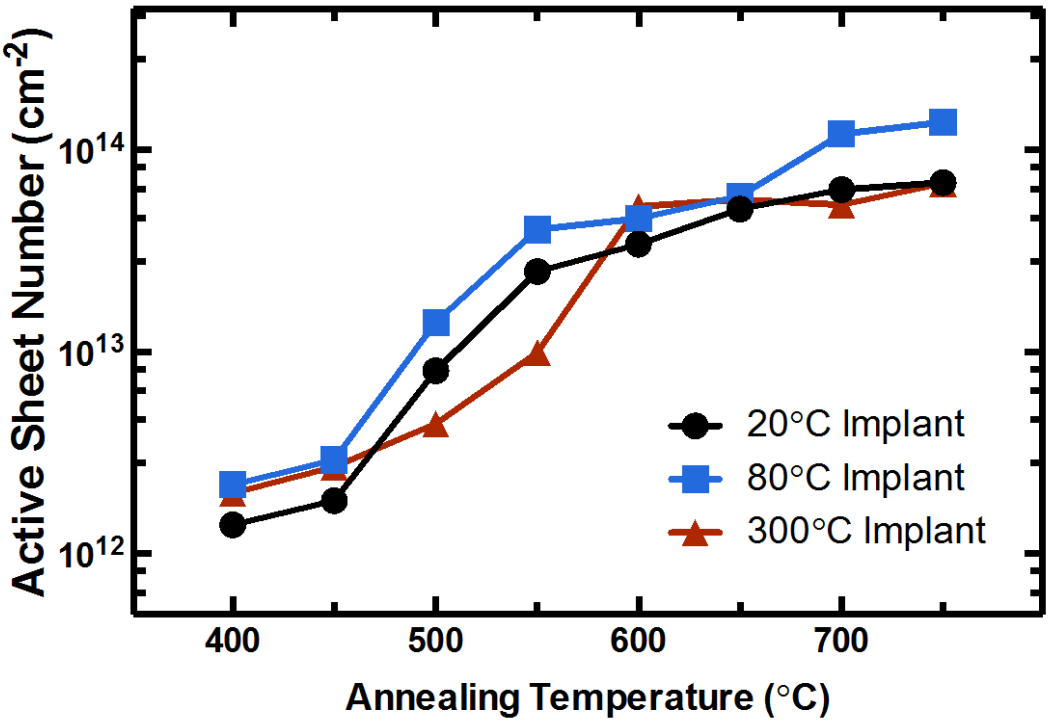

Figure 4-4. Measured sheet number as a function of 5 s RTA temperature. Series on the plot are for 20 keV, 6×10^{14} cm^{-2} Si$^+$ implants performed at 20°C, 80°C, and 300°C.

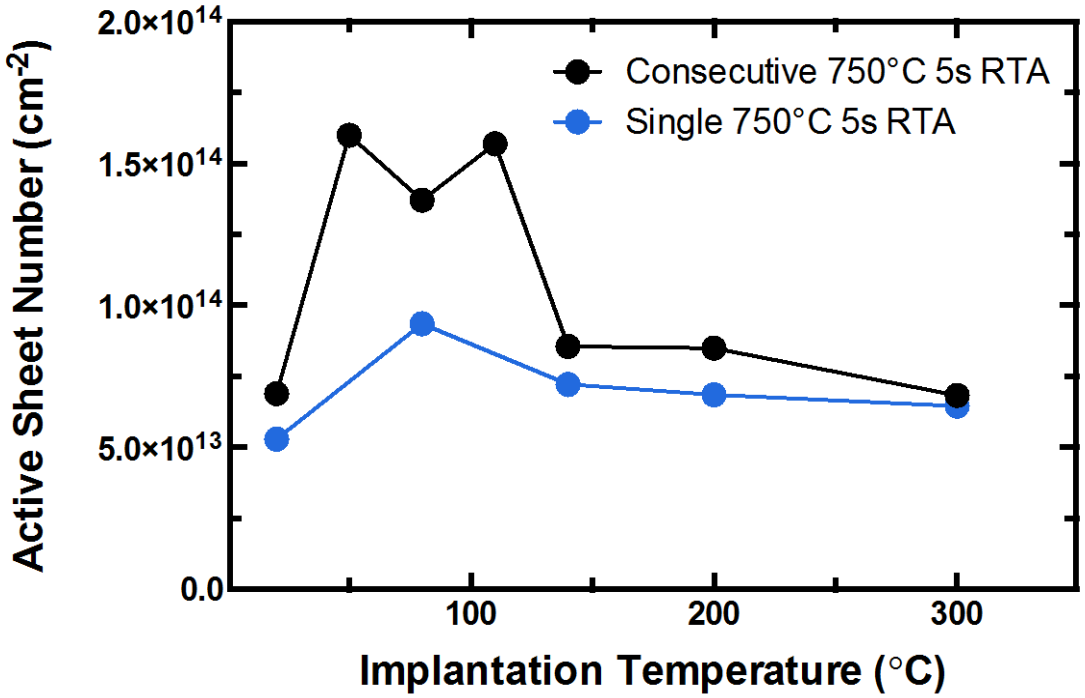

Figure 4-5. Measured sheet number as a function of implantation temperature and annealing treatment. The results are for 20 keV, 6×10^{14} cm^{-2} Si^{+} implants for a single 750°C 5s RTA and consecutive 5 s RTA up to 750°C.

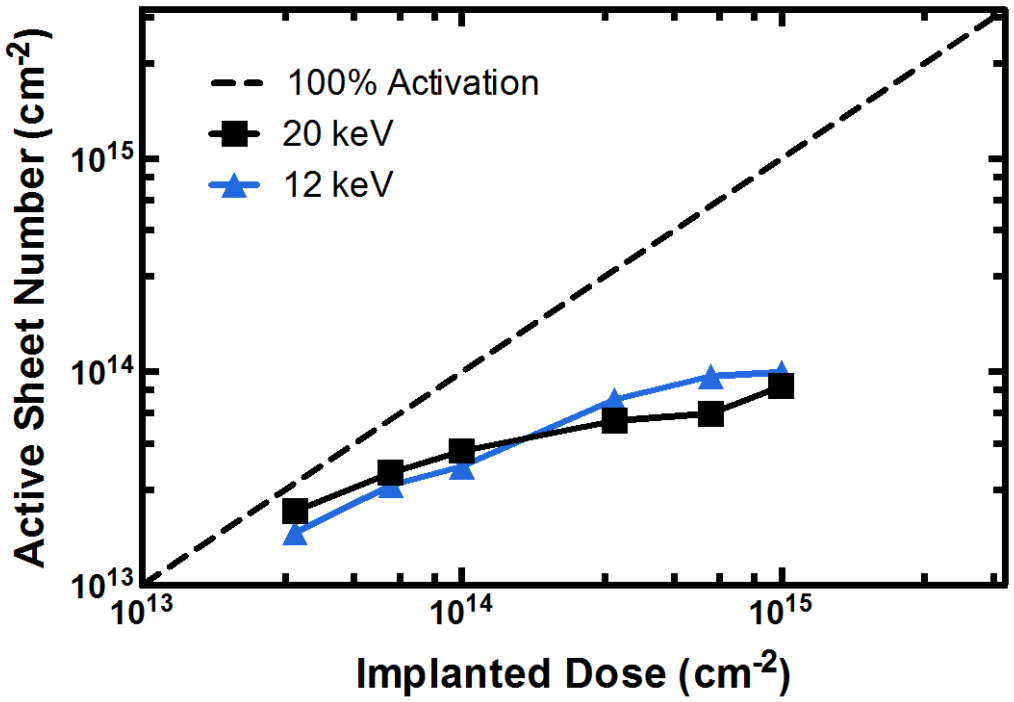

Figure 4-6. Measured sheet number as a function of implanted dose. Measured values are after 750°C 5 s RTA for 12 and 20 keV Si^{+} implants performed at 80°C.

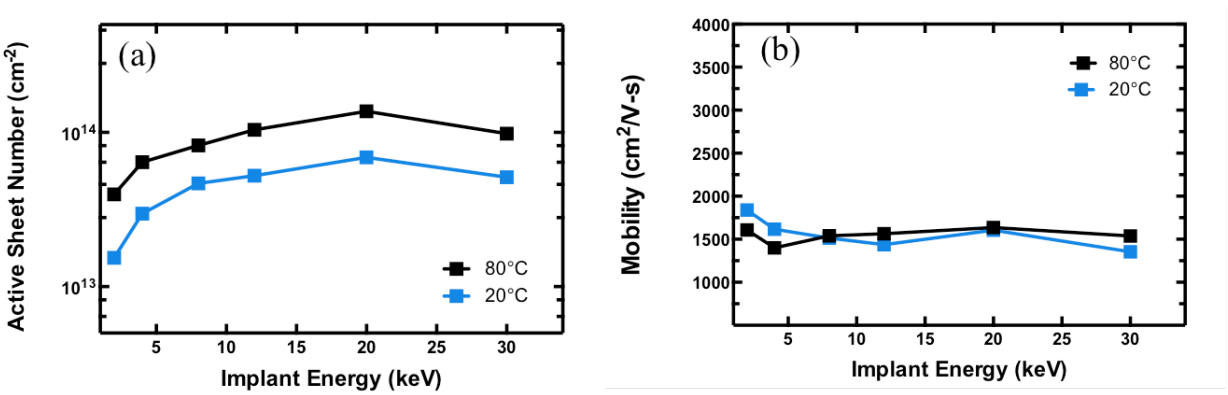

Figure 4-7. Active sheet number and mobility as a function of Si implant energy. Active sheet number (a) improves with energy and carrier mobility (b) is constant as a function of implant energy for 20°C and 80°C, 6×10^{14} cm^{-2} Si^{+} implants after 750°C 5s RTA.

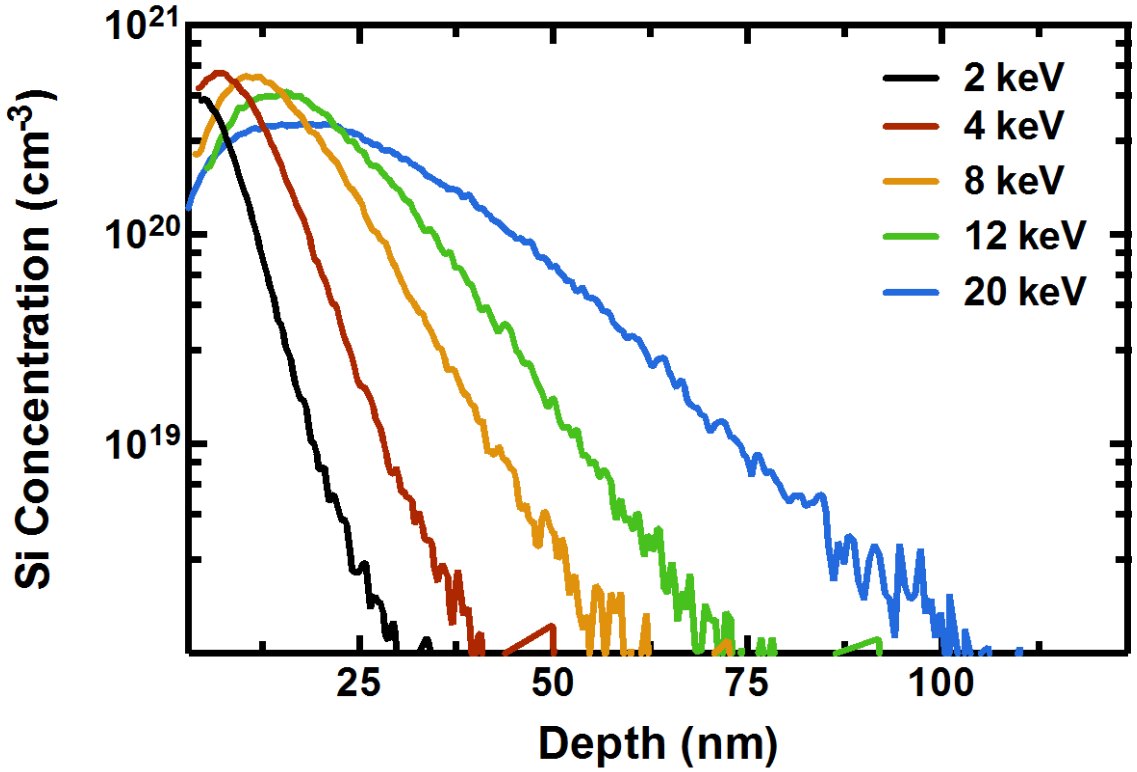

Figure 4-8. SIMS of as-implanted 6×10^{14} cm^{-2} Si^{+} implants performed at 80°C for energies ranging from 2 keV to 20 keV.

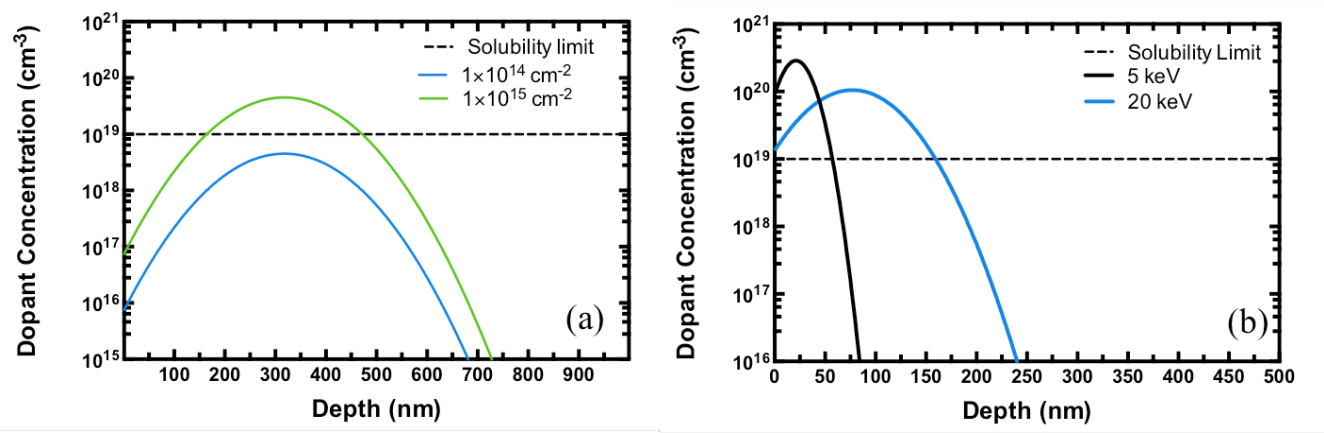

Figure 4-9. Schematic diagrams highlighting the limitation of comparing sheet number and percent activation of implants. Implants with peak concentrations below the chemical/electrical solubility limit will show higher percent activations but can say nothing of the actual chemical solubility unless the profile shape is known (a). Similarly, implants with peak concentrations above the chemical solubility but at higher energies at a fixed dose will exhibit higher active sheet numbers despite having no obvious differences in chemical solubility as show in (b).

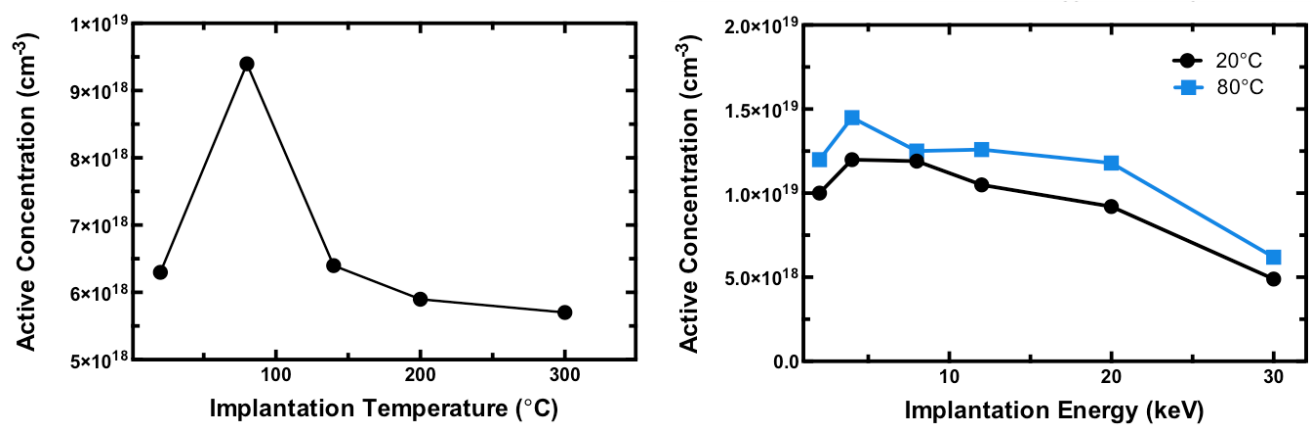

Figure 4-10. Active concentration for previous implantation temperature and energy experiments. The active carrier concentration as a function of implantation temperature (a) is for a 20 keV, 6×10^{14} cm^{-2} Si^{+} implant after a single 750°C 5s RTA. The active carrier concentration as a function of implantation energy (b) is for 20°C and 80°C, 6×10^{14} cm^{-2} Si^{+} with a single 750°C 5s RTA

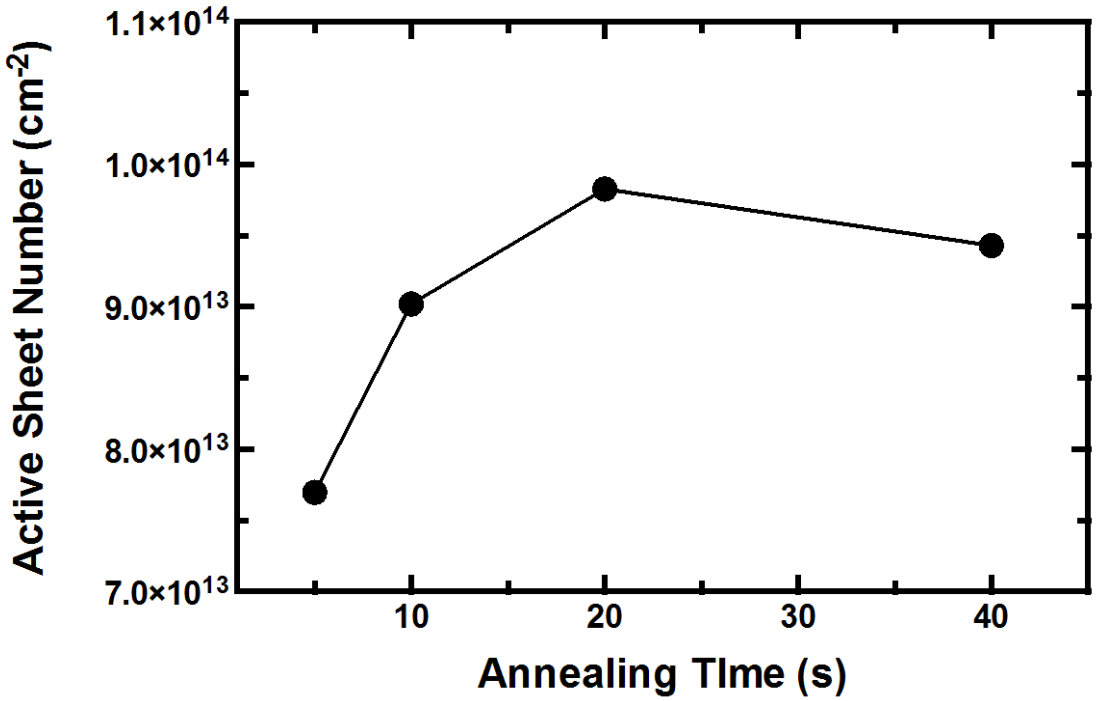

Figure 4-11. Active sheet number as a function of 750°C RTA time for a 10 keV, 5×10^{14} cm^{-2} Si^{+} implant at 80°C.

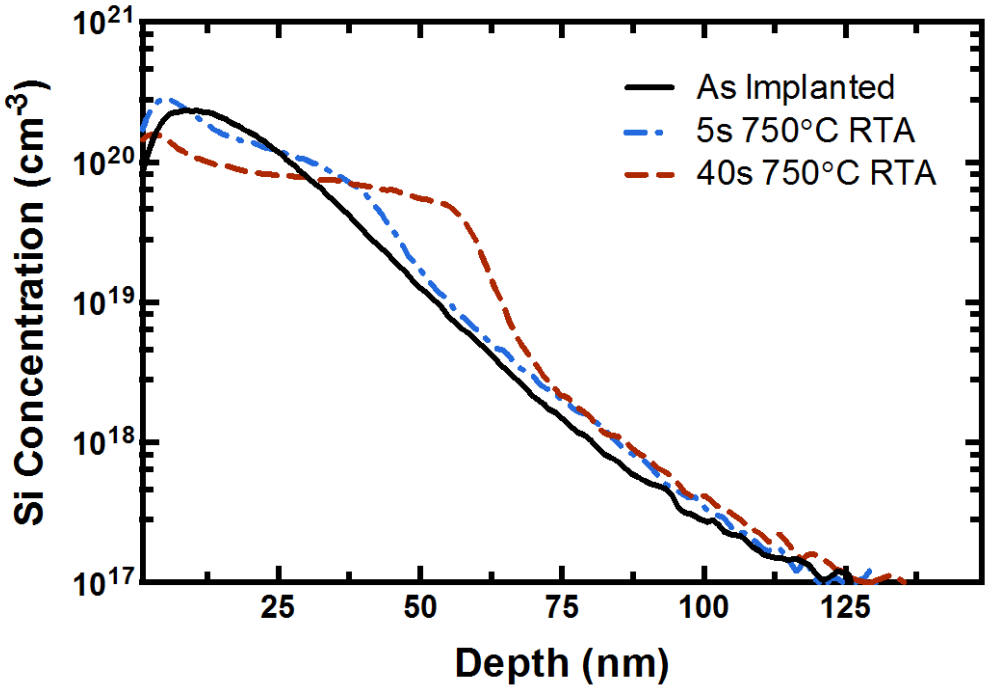

Figure 4-12. Si concentration as a function of depth as determined by SIMS. Concentration profiles are for a 10 keV, 5×10^{14} cm^{-2} Si^{+} implant at 80°C in the as-implanted state and annealing at 750°C for 5 s and 40 s.

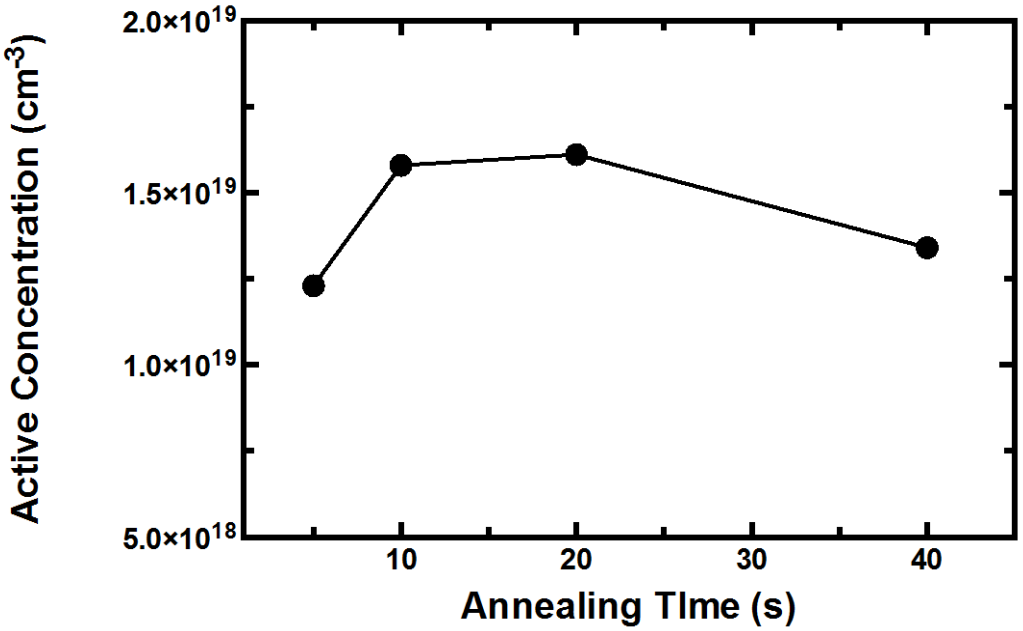

Figure 4-13. Active carrier concentration as determined from active sheet number and post-anneal SIMS as a function of 750°C RTA time. Activation is for a 10 keV, 5×10^{14} cm^{-2} Si^{+} implant at 80°C.

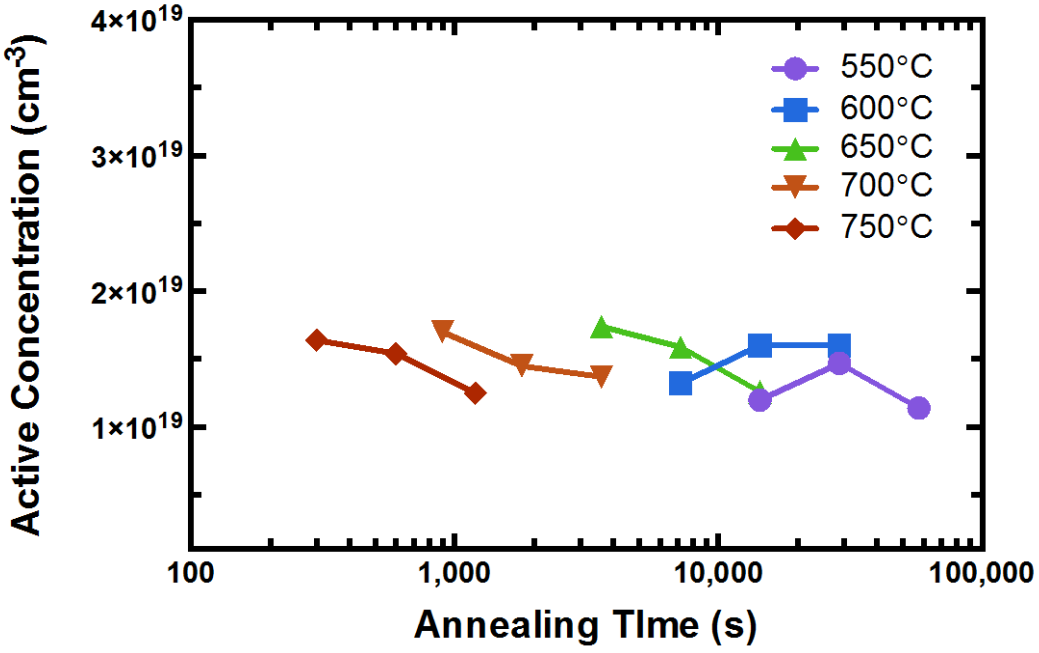

Figure 4-14. Active carrier concentration as a function of annealing time and temperature. Measurements are for a 10 keV, 5×10^{14} cm^{-2} Si^{+} implant at 80°C. This result indicates that electrical solubility of Si is independent of annealing temperature and that Si activation saturates at a maximum concentration around $1.5\times10^{19}cm^{-3}$.

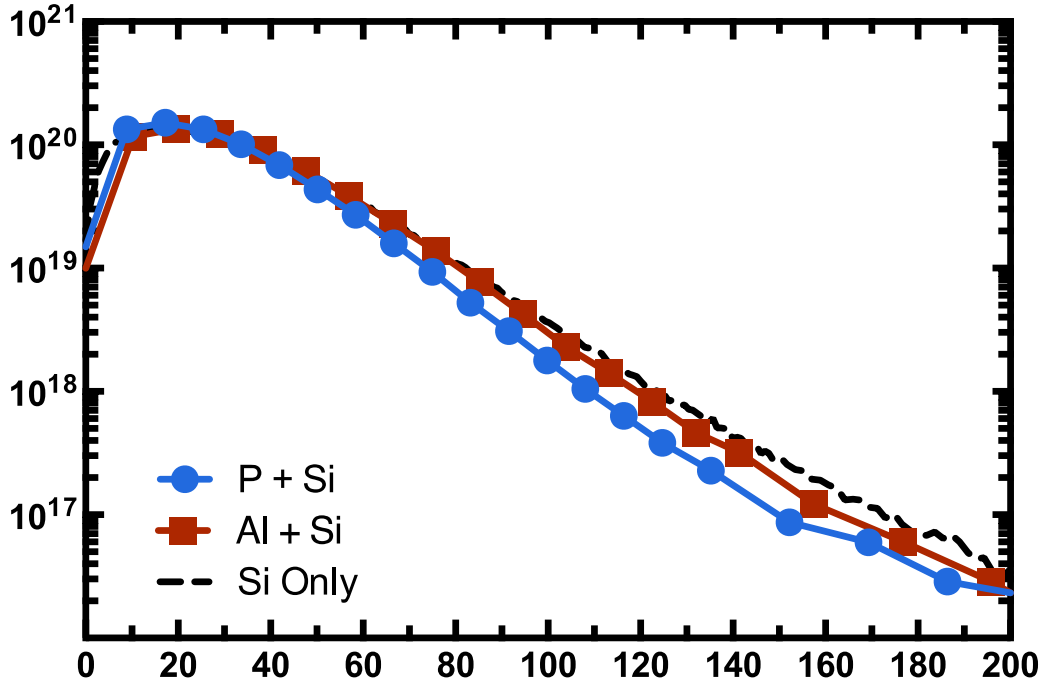

Figure 4-15. As-implanted Si concentration as a function of depth as determined by SIMS. Concentration profiles are for a single 20 keV, 6×10^{14} cm^{-2} Si^{+} implant and for a 20 keV, 6×10^{14} cm^{-2} Si^{+} implant with a 20 keV, 6×10^{14} cm^{-2} P^{+} and 20 keV, 6×10^{14} cm^{-2} Al^{+} implants. The peaks of all implanted species are co-incident but it is observed that co-implantation reduces random channeling in the tail region presumably due to increased damage as heavier P^{+} implants are shown to results in slightly more channeling than Al^{+} implants and single Si^{+} implants have the lease amount of random channeling.

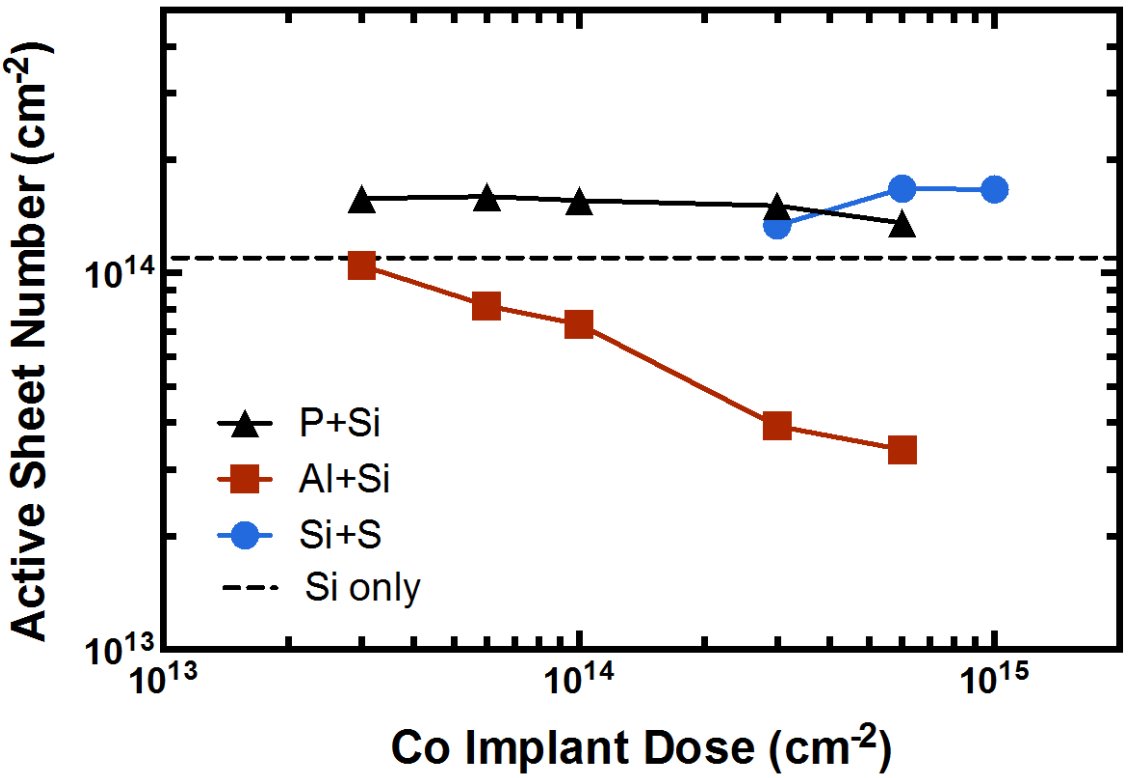

Figure 4-16. Co-implant activation as a function of co-implant dose for after a 750°C 5s RTA. Active sheet number is plotted as a function of 20 keV, 100°C co-implant dose of Al^+, P^+ and S^+ with a 20 keV, 6×10^{14} cm^{-2} Si^+ implant at 100°C. Al^+ co-implants are shown to reduce the active sheet number but S^+ and P^+ implants do not result in enhanced activation contrary to the co-implantation hypothesis. Activation of Si^+ and S^+ implants are not additive.

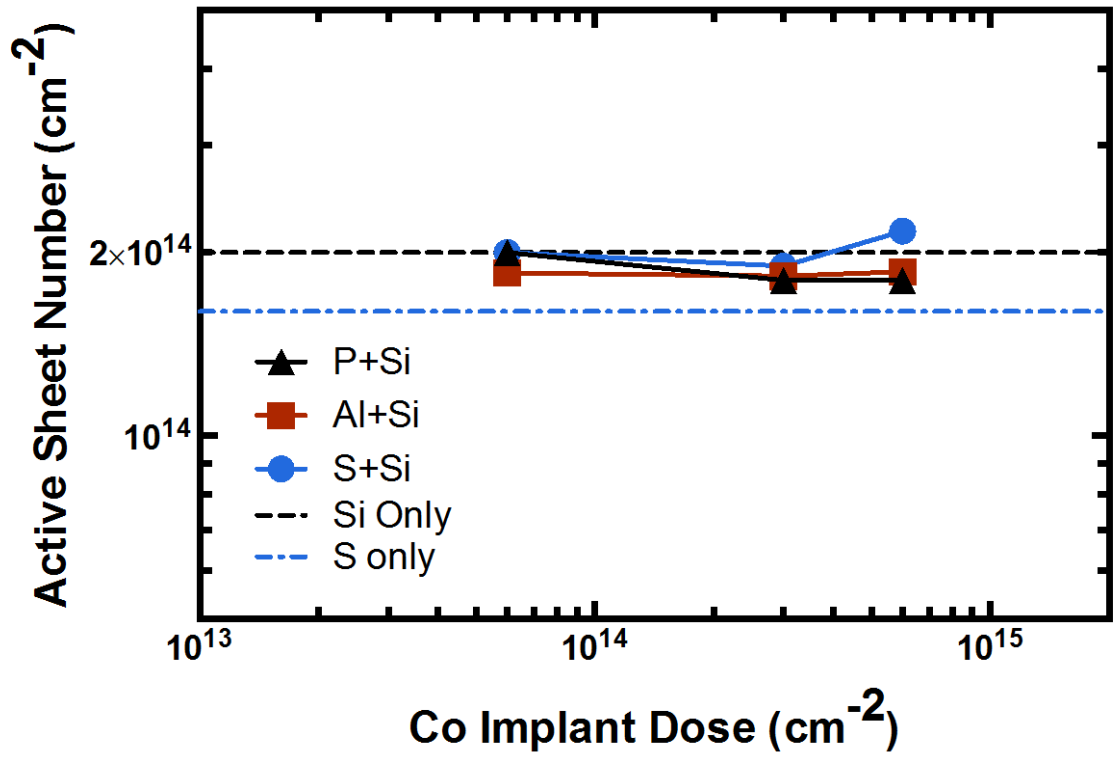

Figure 4-17. Co-implant activation as a function of co-implant dose for after a 750°C 10m furnace anneal. Active sheet number is plotted as a function of 20 keV, 100°C co-implant dose of Al^+, P^+ and S^+ with a 20 keV, 6×10^{14} cm^{-2} Si^+ implant at 100°C. For longer anneal times that result in significant Si diffusion, there is no difference active sheet number for P^+, Al^+ or S^+ co-implant species.

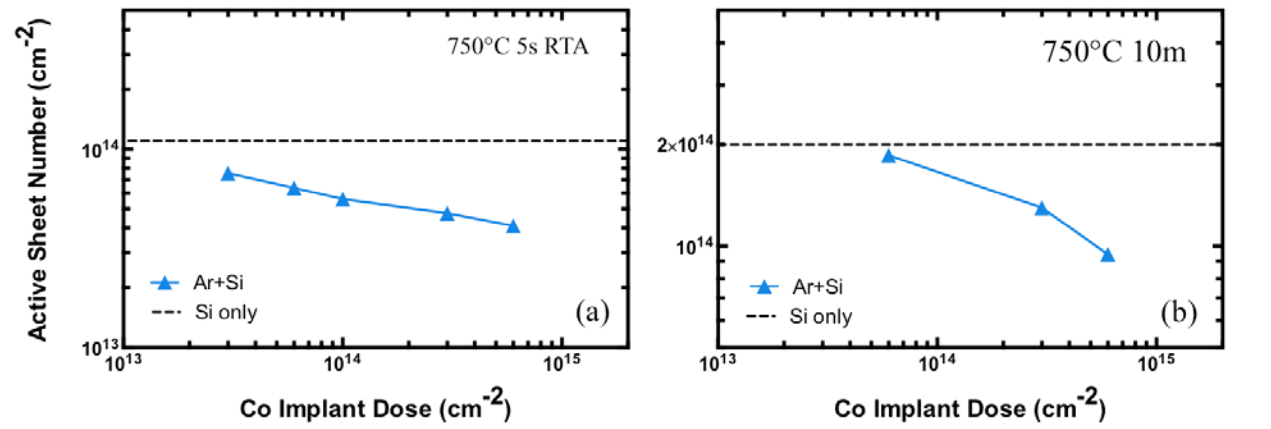

Figure 4-18. Plot of activation effects of argon co-implant on Si activation. Active sheet number as a function of 27 keV, 100°C co-implant dose of Ar^+ with a 20 keV, 6×10^{14} cm^{-2} Si^+ implant at 100°C is shown after (a) 750°C 5 s RTA and (b) 750°C 10 m anneal.

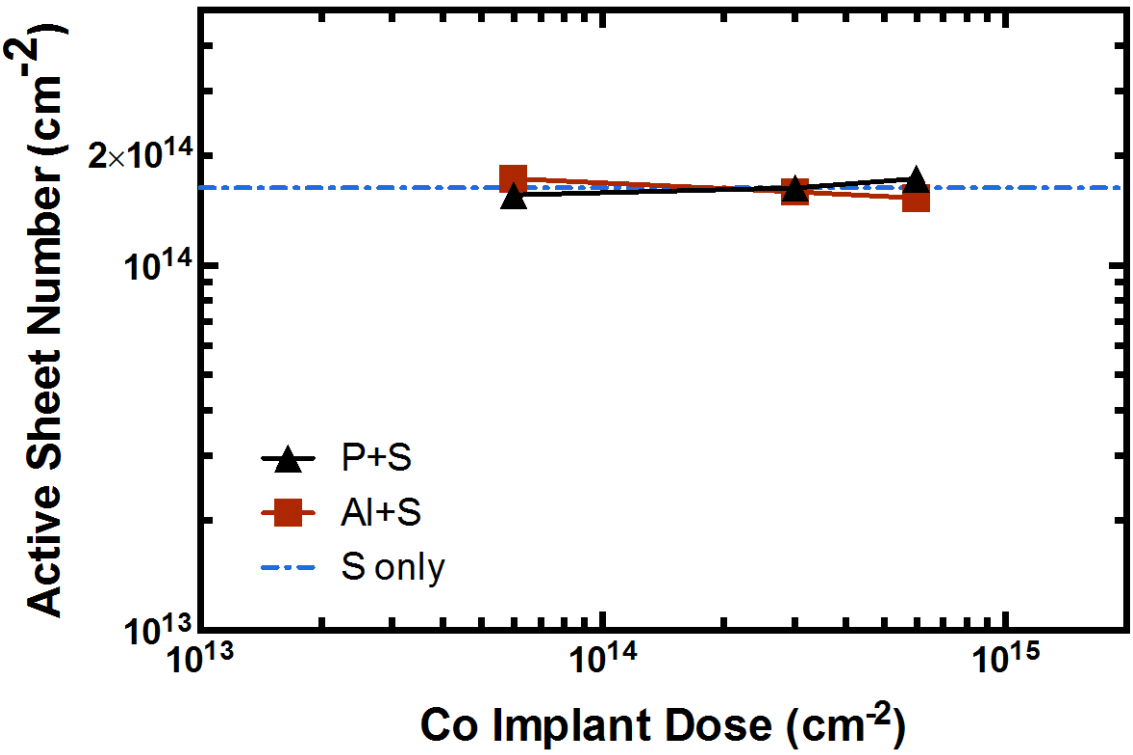

Figure 4-19. Active sheet number as a function of 20 keV, 100°C co-implant dose of Al^+, P^+. Activation is after 10 m 750°C anneal of a 20 keV, 6×10^{14} cm^{-2} S^+ implant at 100°C.

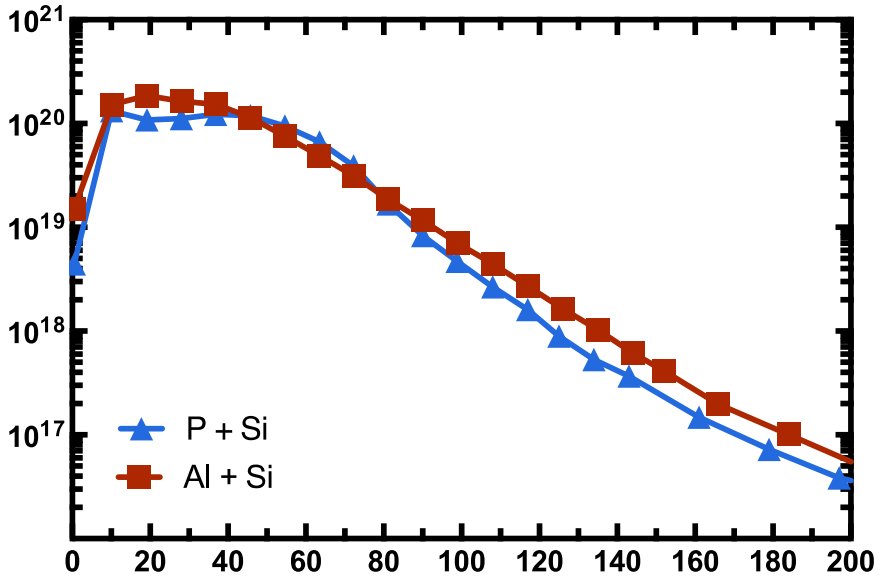

Figure 4-20. As-implanted Si concentration as a function of depth as determined by SIMS. Concentration profiles are for a 20 keV, 6×10^{14} cm^{-2} Si^{+} implant with a 20 keV, 6×10^{14} cm^{-2} P^{+} and 20 keV, 6×10^{14} cm^{-2} Al^{+} implants after 750°C 5 s RTA.

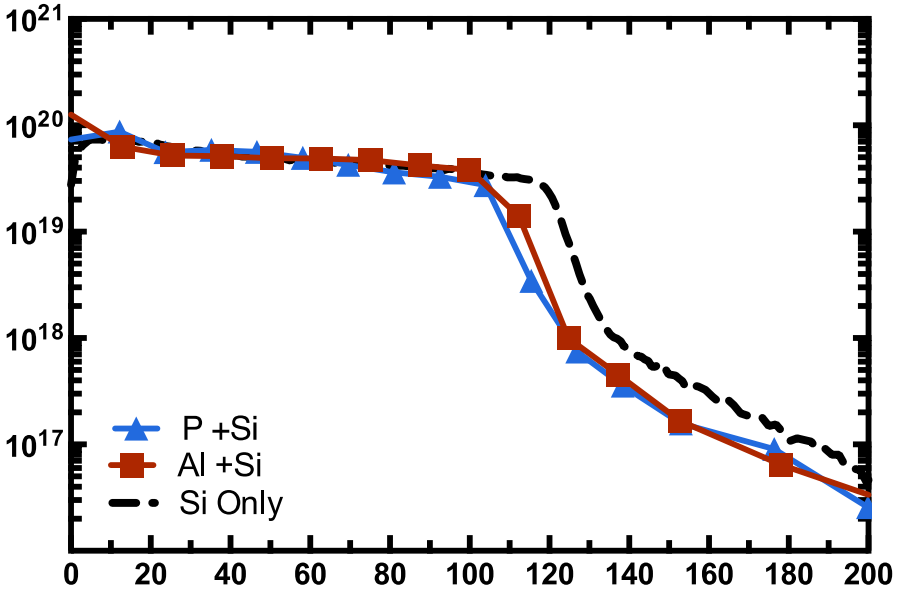

Figure 4-21. Post anneal Si concentration as a function of depth as determined by SIMS. Concentration profiles are for a single 20 keV, 6×10^{14} cm^{-2} Si^{+} implant and for a 20 keV, 6×10^{14} cm^{-2} Si^{+} implant with a 20 keV, 6×10^{14} cm^{-2} P^{+} and 20 keV, 6×10^{14} cm^{-2} Al^{+} implants after 750°C 10m anneal.

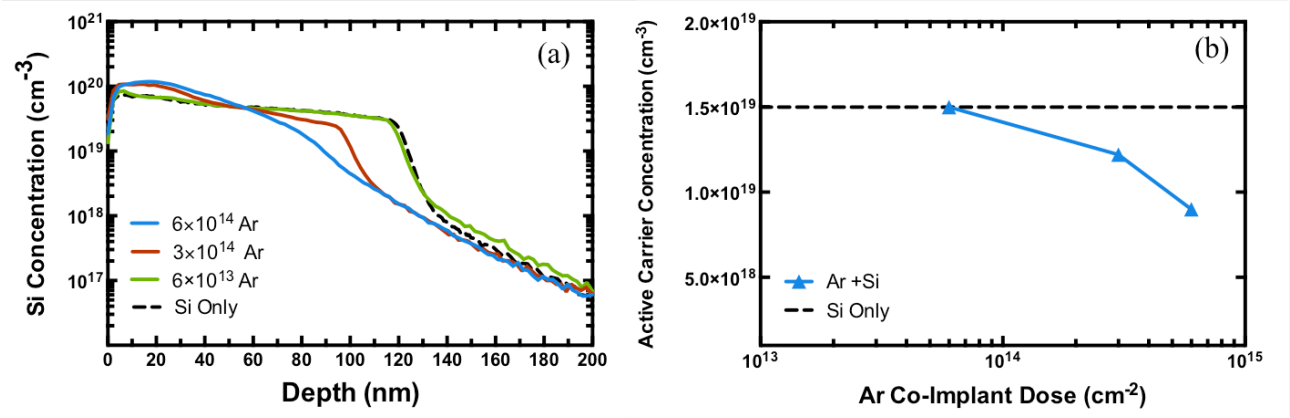

Figure 4-22. Post-anneal Si diffusion and activation for varying Ar co-implant doses. Si concentration as a function of depth as determined by SIMS is shown in (a) for a 20 keV, 6×10^{14} cm^{-2} Si^{+} implant with a 27 keV, Ar^{+} implanted at 100°C at varying doses after 750°C 10 m anneal. Active carrier concentrations is shown in (b) for the same implant and anneal conditions.

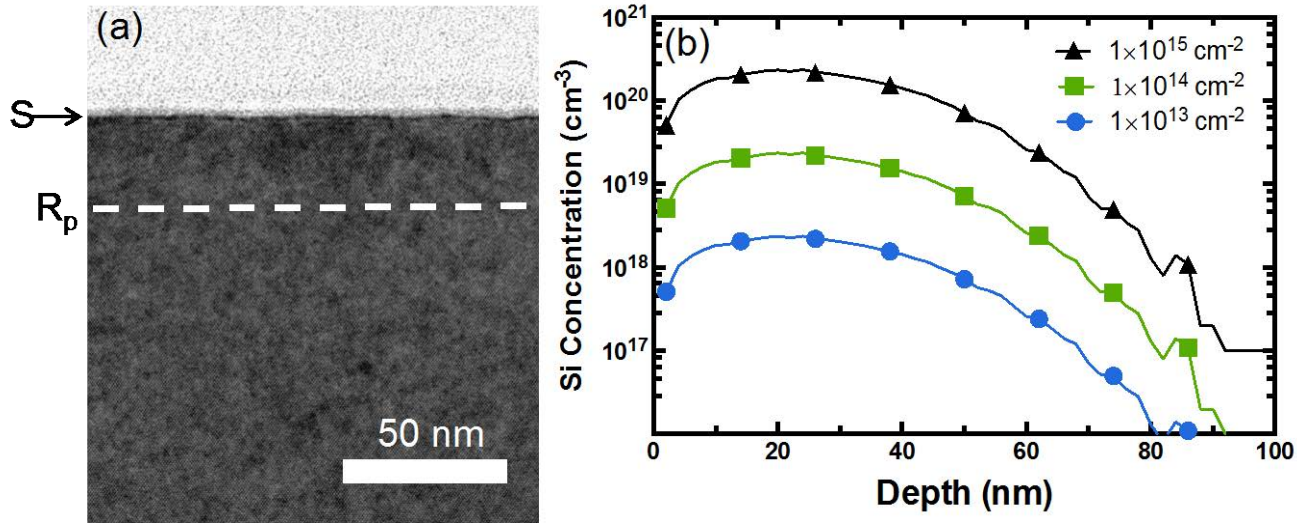

Figure 4-23. Post implant micrographs of Si implanted InAs and corresponding Si concentrations profiles. Post-implant XTEM of 20 keV, 1×10^{15} cm^{-2} Si^{+} implant performed at 100°C is shown in (a). The calculated Si concentration profiles for 20 keV Si^{+} implant at varying implant doses is shown in (b).

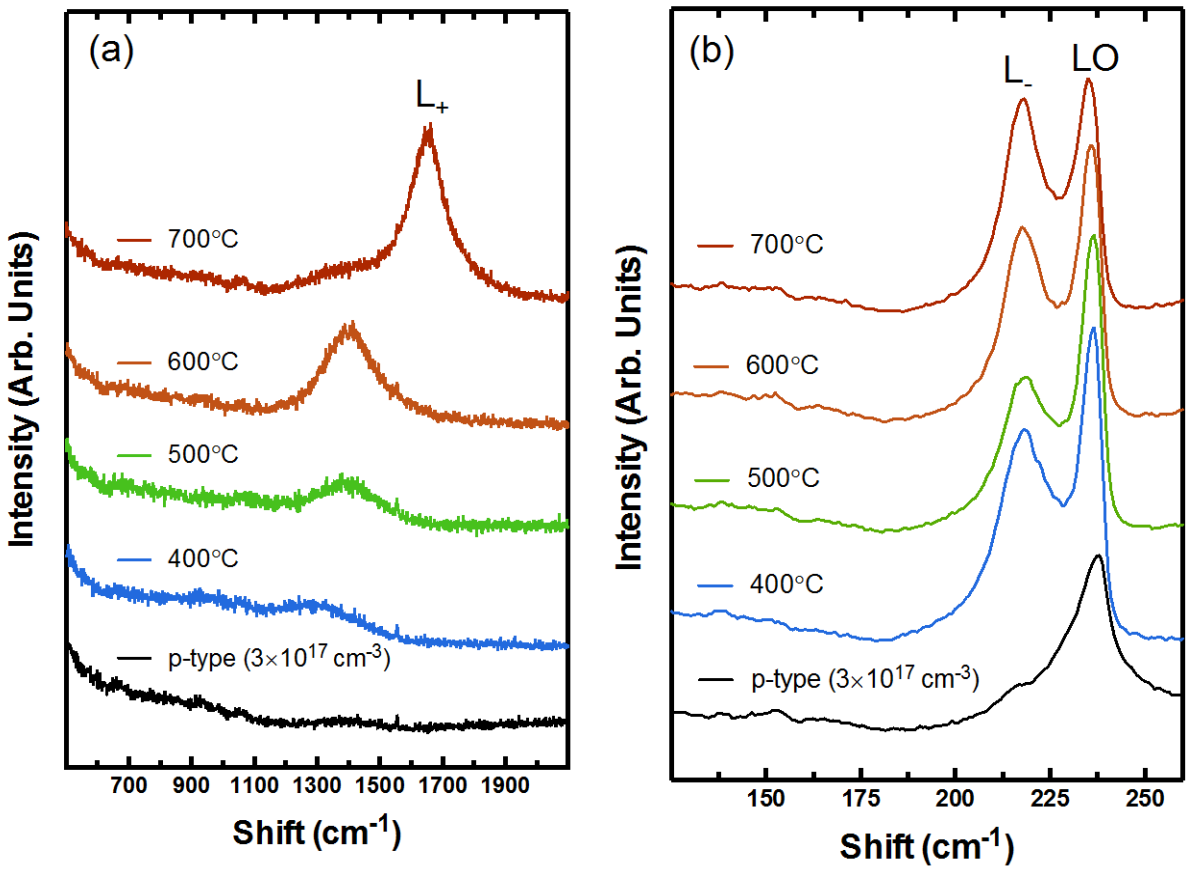

Figure 4-24. Intensity as a function of frequency shift for InAs after varying anneal temperatures. Measured intensity is from a 20 keV, 1×10^{15} cm^{-2} Si^{+} implant performed at 100°C after annealing for 30 s at various temperatures from 400-700°C from (a) 125-260 cm^{-1} emphasizing the L_{-} and LO modes and (b) 500-2000 cm^{-1} emphasizing the L_{+} mode.

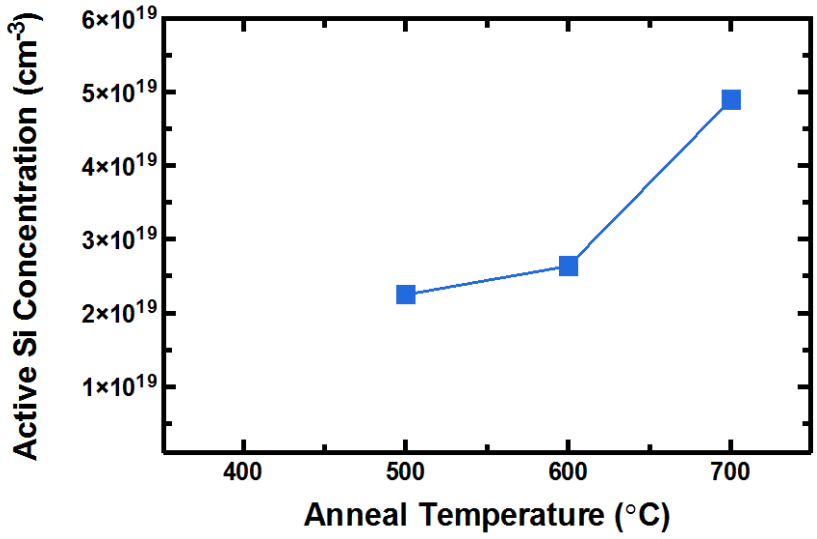

Figure 4-25. Active Si concentration as a function of annealing temperature for a 30 s RTA for a 20 keV, 1×10^{15} cm^{-2} Si^+ implant performed at 100°C

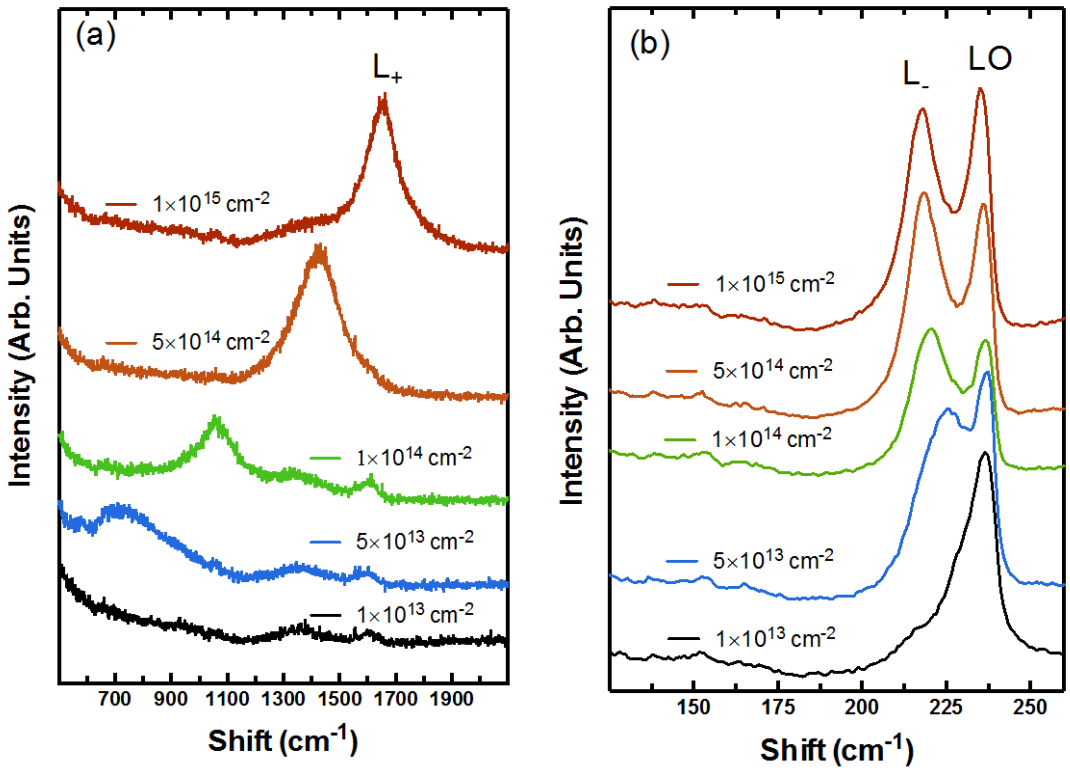

Figure 4-26. Intensity as a function of frequency shift for InAs for various implant doses. Measured intensity is from a 20 keV, Si^+ implant performed at 100°C after annealing at 700°C for 30 s for doses ranging from 1×10^{13} cm^{-2} to 1×10^{15} cm^{-2} from (a) 500-2100 cm^{-1} highlighting the L_+ mode and (b) the L_- and LO modes from 125-260 cm^{-1}

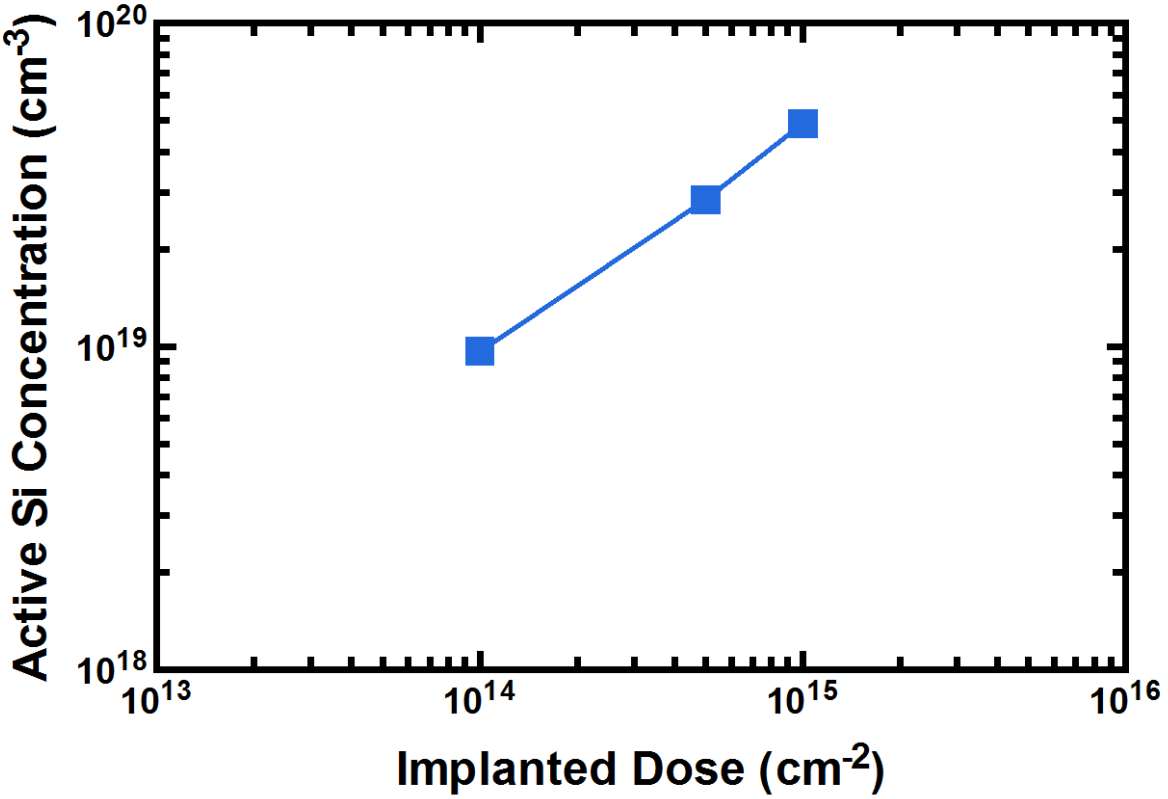

Figure 4-27. Active Si concentration as a function of implanted dose in InAs. Measurements are for a 700°C, 30 s RTA for a 20 keV, 5×10^{13} -1×10^{15} cm^{-2} Si^{+} implants performed at 100°C.

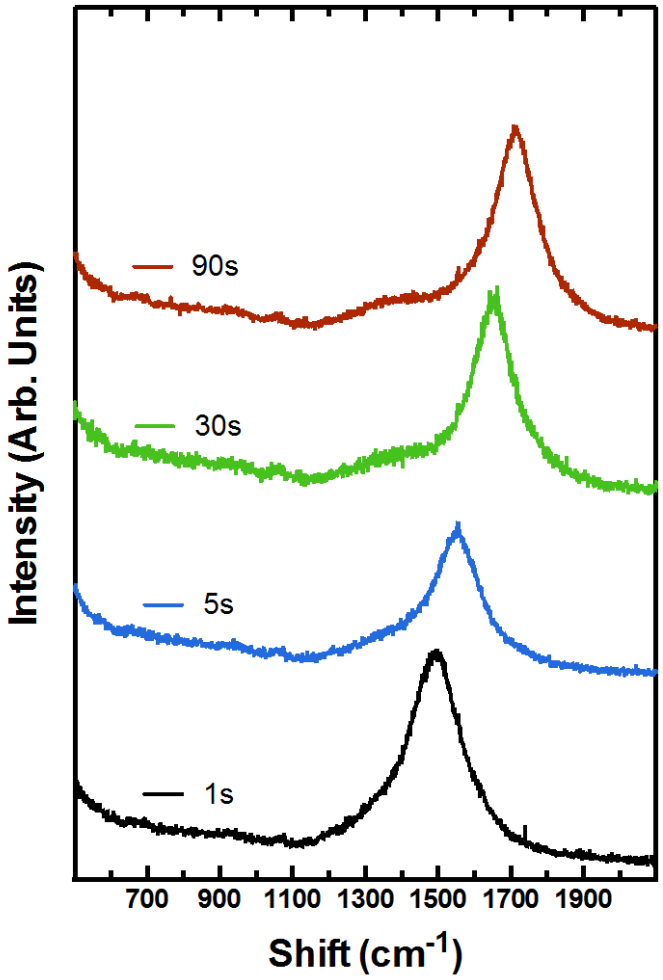

Figure 4-28. Intensity as a function of frequency shift for InAs for varying anneal times. InAs was implanted with a 20 keV, 1×10^{15} cm^{-2} Si^{+} implant performed at 100°C after annealing at 700°C.

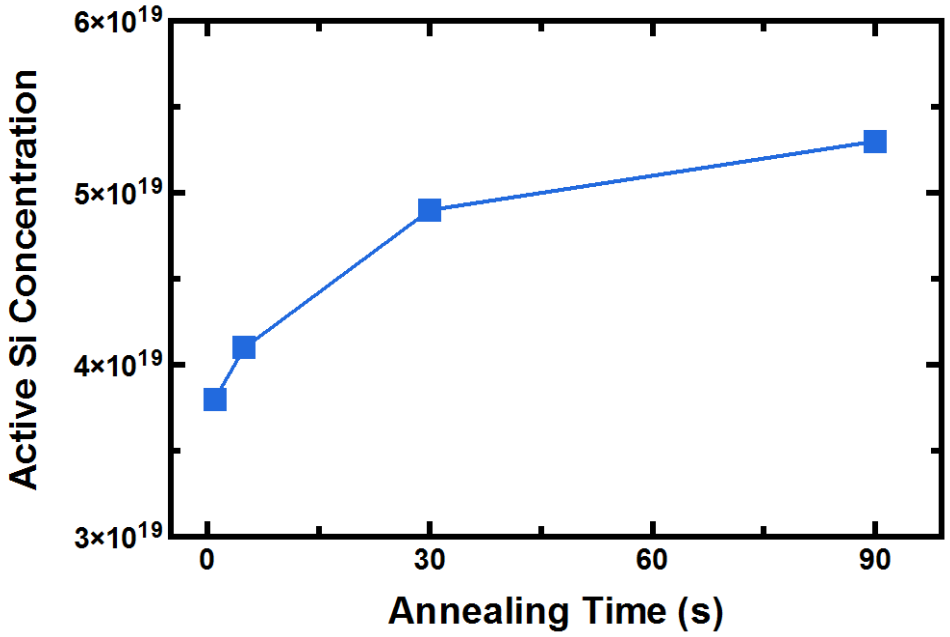

Figure 4-29. Active Si concentration as a function of annealing time at 700°C. The plot is for InAs with a 20 keV, 1×10^{15} cm^{-2} Si^{+} implant performed at 100°C after annealing at 700°C for various times from 1-90 s.

CHAPTER 5
COMPARISON OF SOLUBILITY LIMITS AND DIFFUSION OF GROWN-IN AND ION IMPLANTED SI IN InGaAs

5.1 Background

Previous implant studies including the studies in this work have yet to show any evidence of electrically active Si concentrations in excess of 1.5×10^{19} cm^{-3} despite studies with grown in Si regularly exhibiting concentrations of $3\text{-}6\times10^{19}$ cm^{-3}. [49], [50], [263], [264] Ideally, it would be possible to dope source and drain regions with even higher active concentrations to further reduce contact resistivity but the evidence so far points at an intrinsic limitation to the donor solubility of ion implanted Si.

Given the lack of evidence of active dopant incorporations above $6\times10^{19}cm^{-3}$ for implanted substrates it is fair to ask what is the limiting factor in dopant incorporation in these materials and why is there a discrepancy between ion implanted dopant activate concentrations and those obtained in MBE. Previous experiments have suggested that residual implant damage leads to the differences in active concentrations obtained by growth doping and implantation methods but the experiments in this work with co-implants and elevated temperature implants suggest that damage alone does not explain the regularly achieved active solubility limit.

Most growth process for III-V materials occurs at temperature between 400 and 600°C to which are necessary to break down organic precursors and promote epitaxial layer by layer growth and these samples are then compared with active doping concentrations from implants requiring annealing treatments of 750°C or more to move dopants onto lattice sites. Previous researchers have observed deactivation in heavily Si-doped InGaAs grown on InP but the resultant deactivation has been attributed to diffusion of carriers into the underlying semi-insulating substrate but no explanation of Si

deactivation below temperatures required for diffusion is given.[265] The purpose of this experiment was to determine the stability of growth doped Si concentrations above the previously established limit for ion implanted Si InGaAs.

5.2 Experimental Procedure

Two substrates were used to compare the stability of Si activation in growth doped InGaAs to that of ion implanted InGaAs. 300 nm of MOCVD grown InGaAs on InP substrates were implanted with a 10 keV, 5×10^{14} cm^{-2} Si^{+}. A second InGaAs substrate with a heavily doped 60 nm surface InGaAs and 320 nm nominally undoped InGaAs layer was grown by MBE on semi-insulating InP. The active peak Si concentration was calculated to be 2.86×10^{19} cm^{-3} and a chemical peak Si concentration of 7×10^{19} cm^{-3} was measured by SIMS. Even from initial electrical measurements it is obvious that there is a large portion of Si that is compensated in the growth doped sample. Samples consisting of both substrate types were annealed side by side for 10 minutes in a tube furnace in Ar ambient at temperatures from 450 to 750°C. Both samples used the Al_2O_3 dielectric encapsulation used in previous experiments to prevent surface degradation. After annealing, the dielectric encapsulation was removed with buffered oxide etch and electrical characterization was performed with van der Pauw Hall effect. SIMS of the post anneal samples was also performed to allow for calculation of solubility limits that accounted for Si diffusion. Tables containing the experimental implant and anneal conditions for all of the Si doped samples detailed in Chapter 5 is included in Table B-7 of Appendix B.

5.3 Activation and Deactivation of Si in InGaAs

Figure 5-1 shows the active sheet number as a function of annealing time for both growth-doped and implanted substrates. It is immediately obvious that the growth-

doped substrates exhibit deactivation and then activation behavior whereas the implanted samples show continual improvements in activation with increasing annealing temperature, consistent with observations of stable doping limits of Si implanted InGaAs in the previous chapters.

Post-anneal SIMS in Figure 5-2 shows that well before Si diffusion is observed there is also measureable decrease in active sheet number. The SIMS also explains the increase in activation of the MBE grown samples as with higher anneal temperatures since the diffusion of Si continues into the bulk such that higher active sheet numbers are reported after the initial decrease. Significant Si diffusion in ion implanted samples is only observed upon annealing at 750°C. Furthermore, both doping methods show similar concentration depended diffusion behavior with shouldering occurring at the previously observed 3×10^{19} cm^{-3} Si concentration.

Figure 5-3 shows carrier concentration calculated from the sheet number and SIMS measurements. In the case of grown in Si, the active carrier concentration is shown to steadily decrease to a stable active carrier concentration of 1.5×10^{19} cm^{-3}. Additionally, this deactivation is shown to occur well before the onset of diffusion in the case of growth doped InGaAs. Previous observations of deactivation attributed the deactivation of the InGaAs substrate to diffusion of dopants into the underlying substrate[265], but the results of this work indicate that diffusion related deactivation is not the likely cause since the Si diffusion occurs completely in the InGaAs layer. Once significant diffusion is observed in the growth doped samples the active carrier concentration stabilizes to an active carrier concentration of 1.5×10^{19} cm^{-3}. This observation parallels the behavior in ion implanted InGaAs where profiles which exhibit

diffusion result in maximized active concentrations of 1.5×10^{19} cm^{-3}. The common activation limits in these two substrates is informative for a couple of reasons.

Firstly, it is obvious that active concentrations above 1.5×10^{19} cm^{-3} obtained by MBE are metastable. While previous experiments attributed deactivation to diffusion into the underlying substrate, the design and annealing of the substrates in this experiment do not allow for diffusion of the active species into the semi insulating InP substrate. As a result, it is possible to say conclusively that the previous report of deactivation due to movement of dopant into the semi-insulating substrate cannot fully explain all of the observed deactivation behavior. Secondly, it is obvious that the limiting mechanism of activation is not specific to dopant incorporation method. Previous suggestions that implant damage results in the lower achievable activate concentrations relative to MBE no longer make sense once it is observed that similar thermal treatments of implanted and growth doped substrate that result in significant Si diffusion also result in the same maximum active carrier concentration. This result in particular suggests that the low achievable active concentrations in InGaAs are due to a crystalline thermodynamic limit that is intrinsic to InGaAs, consistent with the co-implant results in the previous section, and not due to activation reductions from the implant damage in the case of ion implanted Si into InGaAs. Another interesting observation is that the diffusivity of MBE incorporated Si is higher than that of implanted Si.

The increased diffusion of Si in MBE substrates relative to implanted substrates may be explained by two possible phenomena. One possibility is that the higher active Si concentration necessarily results in higher diffusion from concentration effects. Another possibility is that the vacancy mechanism by which Si is thought to diffuse may

interact with excess interstitials from the implantation process such that the re-combination of interstitials and Si vacancy complexes is retarded until the excess interstitials are consumed. More precise experiments would need to be performed to separate out concentration effects from damage effects in the observed diffusivity.

Despite both substrates having differences in diffusivities, the characteristics of the diffused profiles are similar as each substrate shows a plateau concentration of 3×10^{19} cm^{-3}, under which Si diffusion is much slower for a given annealing temperature. In the case of Si doping in InGaAs it is shown that any amount of annealing that is sufficient to cause Si diffusion will result in limited activation of 1.5×10^{19} cm^{-3} regardless of whether dopants were incorporated during MBE growth or ion implantation.

5.4 Deactivation of Grown-In Te Dopants in InGaAs

Heavily Te doped InGaAs on InP and Si grown by Tommaso Orzali at SEMATECH were also obtained and used in a similar deactivation experiment to the previous Si deactivation study. Detailed conditions of the growth of these samples are given by Orzali et al.[51] After growth, samples were capped with 15 nm of ALD Al_2O_3 before subsequent 10 m deactivating anneals between 550-750°C. For these samples, negligible Te diffusion was assumed in the 100 nm thick Te doped layer to convert measured sheet number to carrier concentration. Figure 5-4 shows the reduction in carrier concentration of the two substrates.

Te is shown to exhibit similar deactivation behavior to that of Si doped substrates where the majority of the deactivation of the tested anneals occurs at temperatures that are not far removed form the growth temperatures. For anneals of 650°C or more, the maximum activation level is measured to be around 8×10^{18} cm^{-3} indicating that Te shows stable activation at levels even lower than that of Si in InGaAs. Deactivation of

group VI dopants has also been observed before in Se doped InGaAs but the experimenters in this work did not continue the deactivation for temperatures far beyond the growth temperature and the activation of the incorporated Se was only reported relative the initial post-growth activation.[129] This result indicates that group VI dopants which cannot self-compensate also exhibit metastable n-type dopant activation suggesting that the observed compensation of n-type dopants in InGaAs is common to both group IV and group VI dopants.

5.5 Discussion of Doping Techniques for Si Incorporation into InGaAs

MOCVD growth is preferred over MBE for most large-scale production operations due to the higher process pressures and throughput of MOCVD. The very high required vacuum for MBE and associated maintenance for MBE systems makes them decidedly less desirable for large operations. MOCVD and MBE have been able to introduce high carrier concentrations above 5×10^{19} cm^{-3} in InGaAs but after annealing at 650°C has not been shown to exceed 1.5×10^{19} cm^{-3} in the case of Si doping in this work. This result suggests that MOCVD and implant strategies might face similar dopant incorporation limits due to thermodynamic effects that are likely limiting implanted Si dopant incorporation in InGaAs.

Monolayer doping is a more recently developed technique that mimics source diffusion of dopants but from the experiment performed in this work it seems obvious that monolayer doping will be unable to result in higher achievable carrier concentrations than implantation or growth doping. Monolayer doping also relies on equilibrium dopant diffusion from the sample surface into the bulk which has been shown in this work to result in a maximum active carrier concentration around 1.5×10^{19}

cm^{-3}. Monolayer doping could potentially be advantageous over implantation for 3-D finFET structures given the conformal nature of dopant introduction whereas implants will likely be affected by shadowing at small enough gate pitches. Growth techniques require an extra etch and growth step to place heavily doped source and drain regions next to the lightly doped channel material.

The deactivation of growth doped substrates at annealing temperatures above the growth temperature also sets an upper limit on back end thermal processing that will be allowable in device design. Any thermal treatment of growth-doped samples with Si or Te incorporation above the thermodynamic stability limit is likely to undergo deactivation.

5.6 Overview of the Role of Point Defects on Activation and Diffusion of Si and Te in InGaAs

There is a preponderance of evidence so far suggesting that the equilibrium concentration of active carriers is limited in large part by the presence of native dopant defect complexes and that the maximum carrier concentration in this case is likely the result of a crystalline thermodynamic limit rather than an artifact of dopant incorporation method or the result of changes in site occupation with increasing Si doping concentrations. Any suitable explanation for the underlying mechanisms that result in the observed doping method independent limits must then take into account other observed behavior of heavily Si doped InGaAs such as the heavily concentration dependent diffusion.

Early experimenters sought to explain the heavy compensation of group IV donors in GaAs and InGaAs by increasing propensity of dopants to occupy group III and group V sites due to the amphoteric nature of these dopants but there is limited direct

evidence for increases in the amphoteric behavior of these dopants being the main determinant for deactivation or saturation. This interpretation has been further complicated by the fact that some group VI dopants such as Se show similar activation limits to Sn and Si in GaAs and InGaAs despite group VI dopants being unable to self compensate[127], [131] and in this work Te was shown to have a lower stable activation limit than Si. For the case of group VI dopants the upper activation limits cannot be attributed to the amphoteric site occupation but must attributed to other mechanisms such as clustering. Both clustering and amphoteric limited activation explanations have limited amounts of direct evidence to support these claims but it also seem highly coincidental that two completely different mechanisms of compensation (clustering/solubility limitations and amphoteric substitution) would result in nearly identical n-type doping limits in InGaAs or GaAs for Si, S, Se, and Te.

Most of these previously advanced explanations of compensation also regularly fail to predict relevant properties of diffusion in group III-As systems. It is not expected that Si-Si next nearest pairs would have high diffusivity in GaAs and InGaAs based on theoretical calculations[233] for amphoteric compensation. Instead the best explanation of the observed activation limits for co-implanted samples and MBE and implanted samples, as well as the heavily concentration dependent diffusion observed in this work are all readily explained and even predicted by the amphoteric defect model developed by Walukiewicz.[262], [266] More thorough treatments of this model are presented in the papers authored by Walukiewicz but a brief explanation of underlying mechanisms is warranted in this work as it relates to the observed n-type activation limits of group IV and group VI dopants as well as the concentration dependent diffusion of Si in InGaAs.

In the case of heavy n-type doping, the Fermi level of the semiconductor will be shifted further and further towards the conduction band. The shifting of the Fermi energy towards the conduction band will results in a reduction in the enthalpy of formation for certain native defects and in the case of group III-As semiconductors this preferred defect is the group III vacancy. Theoretical calculations by Walukiewicz show that for heavily doped semiconductors where the Fermi levels is pushed into the conductions and subsequently no longer be described by non-degenerate carrier statistics the concentration of compensating group III vacancies can increase exponentially.[267] This exponential rise in negatively charged group III vacancies is able to readily compensate additional donors with the formation of vacancy-dopant complexes.

As a result, this model predicts that maximum n-type doping will be limited by shifts in Fermi level rather than dopant specific site occupation. Any dopant that is able to activate to a high enough carrier concentration to push the Fermi energy into the conduction band will necessarily result in the same or very similar activation limit as is observed experimentally for Si, and Te dopants in InGaAs and GaAs. This effect does not preclude the potential for co-implant effects to exist but it would anticipate that co-implants would be rendered ineffective for increasing the doping above concentrations sufficient to result in the onset of degenerate carrier statistics which lead to large numbers of vacancies being formed. The presence of large numbers of group III vacancies will also manifest itself in the diffusion characteristics of dopant species that diffuse through a group III vacancy mechanism. DFT calculations suggest that Si diffusion in GaAs is mediated by group III vacancies and the presence of a large

amount of group III vacancies caused by shift in the Fermi level provide a consistent explanation for the heavily concentration dependent diffusion of Si in InGaAs for incorporated Si concentrations above 3×10^{19} cm^{-3}.[233] While there are no previous reports of heavily concentration dependent diffusion of Si in InGaAs prior to the results outlined in this work there has been evidence of drastic increases quantum well intermixing of group III species in heavily n-type doped materials that can be explained by the presence of group III vacancy defects.[177], [181], [183] Considerable effort at this point has gone into identification of dopant-vacancy complexes to explain the maximum activation limits in Si and Te-doped GaAs and InAs grown from the liquid phase[139], [268]-[271] but literature on vapor phase epitaxy and ion implantation often prefers the explanation of amphoteric behavior. Experimentally, evidence for increased vacancy populations and vacancy defect complexes has been obtained using positron annihilation spectroscopy[272]-[278] and STM[279]-[281] but theoretical calculations also predict that n-type dopants will significantly decrease the energy for group III vacancy formation.[232], [233], [282], [283] The charge state and nature of the cation vacancy defects in heavily doped GaAs is still an ongoing topic of debate with experimental work often preferring charge states of -1, -2, or -3 however most ab-initio studies indicate that charge states of -3 are energetically favorable at high n-type doping concentrations.[232], [260], [284]-[287]

The amphoteric native defect model proposed by Walukiewicz has had other successes of explaining and predicting some of the other observed behavior in III-V materials. One prediction of the amphoteric defect model indicates that the onset of degenerate carrier statistics for p-type doping occurring at much higher doping levels

due the increased effective mass of holes in III-V materials. While saturation of n-type dopants in III-V materials is regularly limited to the range of a 1-5×10^{19} cm^{-3}, doping densities as high as 1-2×10^{20} cm^{-3} are regularly achieved for p-type dopants in GaAs. Based on this understanding it was realized that changes in the electron or hole effective masses and band structure could result in large changes in achievable carrier concentrations.[288], [289] Experiments with dilute III-V nitrides have shown that the incorporation of 1-5 atomic percent nitrogen can dramatically change the conduction band structure of these materials. This structure change results in higher electron effective masses, and higher achievable density of states and subsequent delay of the onset of degenerate carrier statistics at high doping levels and thereby increase the achievable n-type carrier concentration by an order of magnitude over systems without nitrogen incorporation.[239], [290], [291]

5.7 Summary of Si Activation Limits and Diffusion Behavior in InGaAs

Of the available explanations for the observed behavior of Si activation and diffusion in InGaAs the amphoteric defect and vacancy complexing models proposed by Walukiewicz and Hurle offer the most comprehensive explanation of the observed phenomena in this work. Based on the defect-limited activation model some conclusions about the limits of doping and diffusion behavior of Si in InGaAs can be made.

Firstly, the upper activation limits for Si in InGaAs is almost certainly an intrinsic limitation to InGaAs. Any doping process performed at thermal equilibrium is likely to result in similar activation limits as has been observed in the case of co-implantation, the temperature independent carrier activation of Si in InGaAs and the common activation limits it MBE and ion implant Si doped InGaAs. Increases in the maximum Si carrier concentration limit are likely to only be realized with the introduction of dopants

via non-equilibrium methods such that the creation of compensating defects can be mitigated or through changes in the electronic band structure of a given material as has been experimentally observed in the case of dilute nitrides.

Secondly, high n-type doping in InGaAs is expected to greatly enhance the diffusivity of species that diffuse via group III vacancy mechanisms. This effect is observed in the diffusion of Si in InGaAs but it is also expected that other n-type dopants will also enhance the diffusivity of Si or group III species in III-V materials. As a result, heavy n-type doping from either group IV or group VI dopants in III-V heterostructure could result in increased intermixing of group III constituents as observed by previous experimenters.

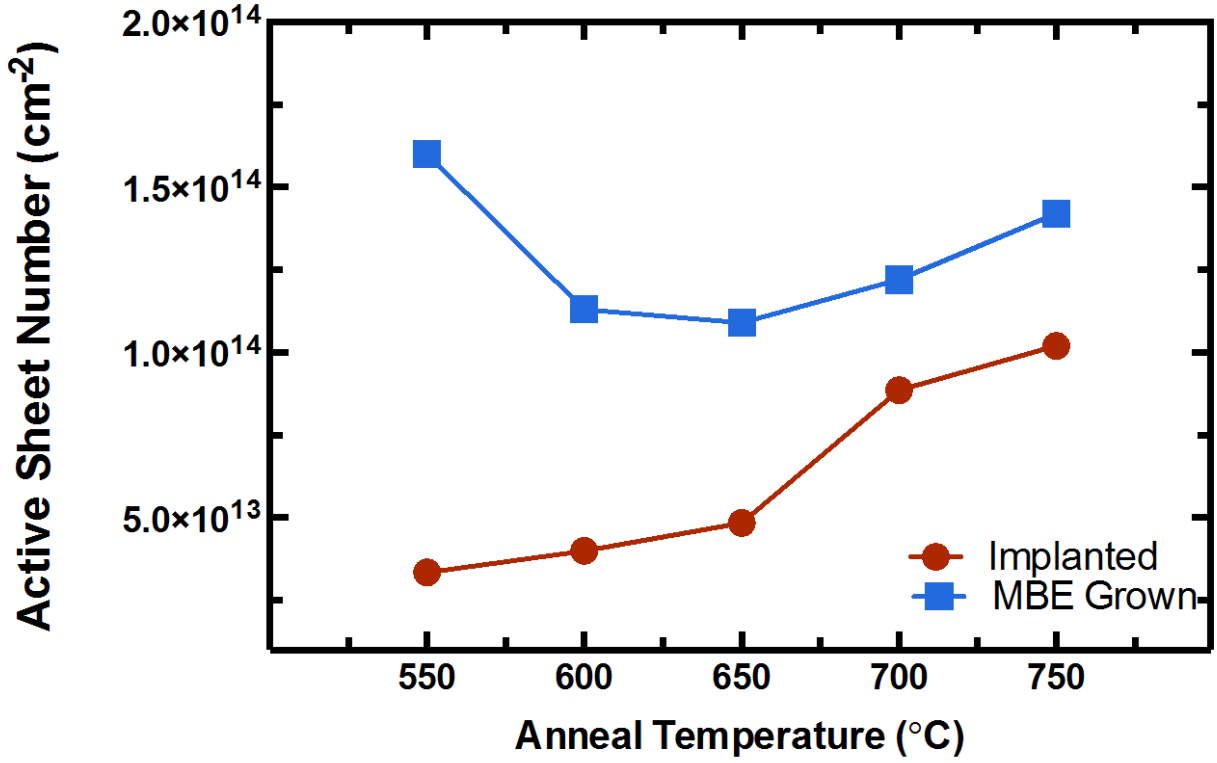

Figure 5-1. Active sheet number of as a function of annealing temperature. Active sheet number is measured for a 10 keV, 5×10^{14} cm^{-2} Si^{+} at implant into InGaAs and MBE grown Si doped InGaAs after 10 m anneals.

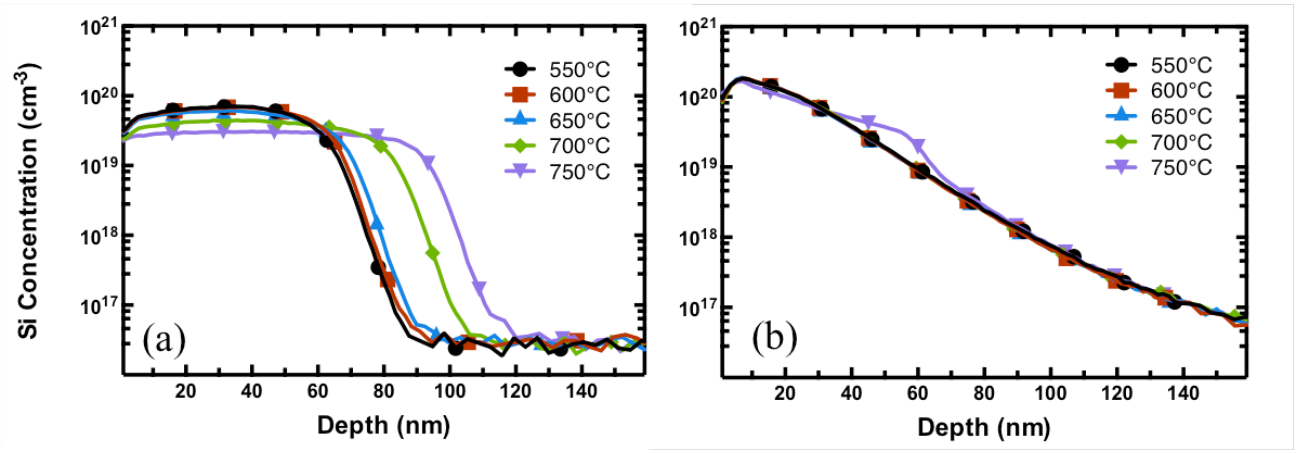

Figure 5-2. Post 10 m anneal Si concentration as a function of depth as determined from SIMS. SIMS profiles are for (a) MBE grown Si doped InGaAs and (b) Si implanted InGaAs.

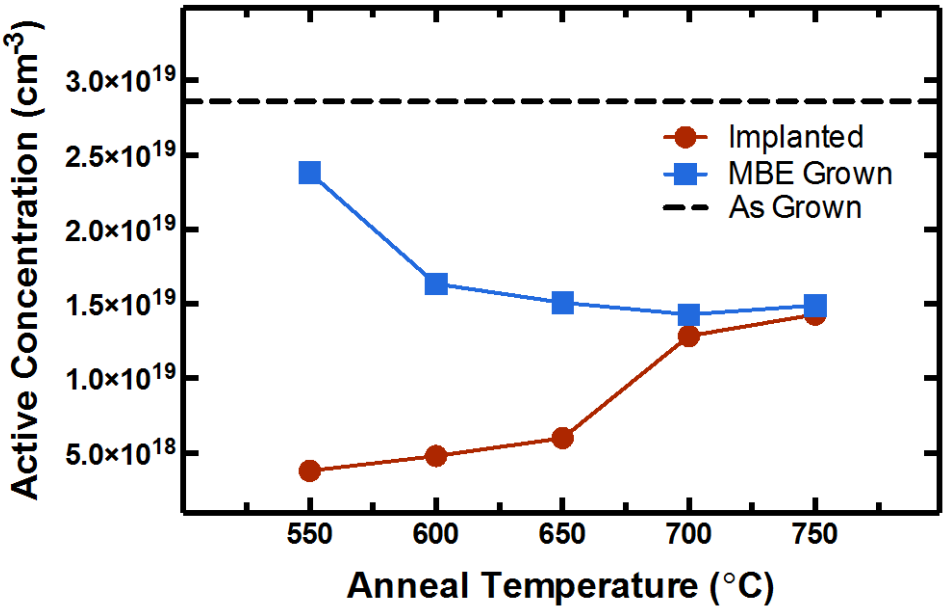

Figure 5-3. Active carrier concentration of as a function of annealing temperature. Values are calculated for 10 keV, 5×10^{14} cm^{-2} Si^{+} at implant into InGaAs and MBE grown Si doped InGaAs after 10 m anneals. This result indicates that active MBE concentrations above the previously established 1.5×10^{19} cm^{-3} active carrier concentration for implants are metastable.

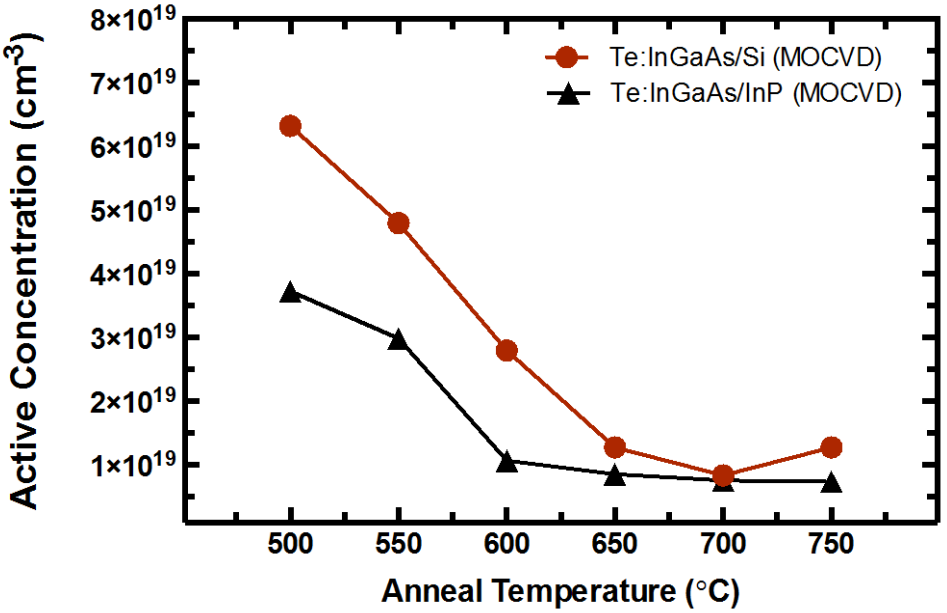

Figure 5-4. Active carrier concentrations as a function of annealing temperature for Te doped InGaAs on Si and InP substrates after 10 m anneals.

CHAPTER 6
MICROSCOPIC INVESTIGATION OF AMORPHIZING AND NON-AMORPHIZING IMPLANT DAMAGE IN InGaAs

6.1 Ion Beam Damage in Solids

The violent nature of the ion implantation process inevitably results in large increases in the number of point defects in ion-irradiated materials. In doping applications, the resultant ion beam damage must be annealed by a thermal treatment step to cause dopant atoms to occupy lattice sites and result in dopant ionization. This rearrangement of atoms also will often result in the formation of extended defects if the concentration of point defects in the implanted materials is high enough. The formation of these dislocations upon annealing of amorphized and non-amorphized regions of implanted substrates is often evident in transmission electron microscopy with high enough defect concentrations. In the case of amorphization, the point defect concentration reaches a critical threshold such that a first order phase transformation from a crystalline structure with long-range order to a solid with no long-range order results. Annealing of amorphized substrates will result in regrowth of the amorphous material beginning at the amorphous/crystalline interface in the implanted substrate but extended defects often result in the regrown layers due to imperfect regrowth. Dislocation loops due to excess interstitials are the predominant defect observed in non-amorphizing implants. Jones et al. outline a more thorough treatment of the possible types of resultant damage in ion-implanted materials and the reader is directed there for a more holistic picture of implant damage in semiconductors.[79]

6.2 Amorphization and Regrowth of InGaAs

The ability to use ion beams to amorphize ion implanted substrates has proven especially useful in Si technologies for a two reasons. Amorphous layers reduce the

amount of channeling in implanted substrates, which allows for the creation of more abrupt implant profiles and amorphization is also critical for solid phase epitaxial growth or SPEG. Solid phase epitaxy or solid phase regrowth or solid phase epitaxial regrowth occurs when the crystalline lattice is recovered beginning at the interface of the amorphous and crystalline regions upon thermal annealing. In Si, SPEG allows for the non-equilibrium incorporation of dopants onto lattice sites during the regrowth process.[292] This regrowth process occurs at a fraction of the melting temperature and in Si often results in virtually defect-free regrown layers.

Amorphization and subsequent regrowth of amorphized layers are largely similar in Si and III-V materials but III-V materials generally result in more defective regrowth and to date there is little evidence that dopants in III-V materials activate upon regrowth.[81], [84], [155], [214], [217], [293] Because of these differences, there is no real technological advantage to the creation of amorphous layers in III-V materials including InGaAs since the reduction in channeling is not worth the problems associated with regrowth. The implant doses required to amorphize III-V materials vary widely and in some cases these materials are nearly impossible to amorphize. AlN is nearly impossible to amorphize even with dose of 1×10^{16} cm^{-2} or more while InAs and GaAs need doses of around $0.5\text{-}1\times10^{15}$ cm^{-2} to cause amorphization. This behavior is due in large part to a materials ability to undergo dynamic annealing and the differences in interatomic bond strength in a given compound. Experiments have shown that InGaAs has a lower amorphization threshold than InAs or GaAs due to the bond length ordering in these solids.[67]

III-V materials exhibit disappointing performance relative to Si with respect to dopant incorporation and regrowth behavior but future transistors devices using 3D structures of Si will also have to avoid amorphization. More recent work studying the SPEG of amorphized Si fins has shown that these structures are prone to regrowth related defects.[294]-[296] This is because the regrowth rates of Si are direction dependent and defective regrowth can occur from an amorphized fin much in the same way that mask-edge defects in amorphized Si and Ge are shown to form. Close pack planes have higher regrowth rates and as a result the regrowth of amorphized fins will result in a higher incidence of regrowth related defects that are easily avoided during SPEG in planar devices.

6.3 Activation of Implanted Si^+ in Amorphous and Crystalline InGaAs

Regrowth of amorphized layers is of limited technological relevance in III-V materials due to the limited activation upon regrowth and reports of poor regrowth but previous studies of Si and Be implants into pre-amorphized GaAs have shown that Be dopants achieve high levels of activation whereas Si shows no appreciable levels of activation and instead forms precipitates.[155], [217] Previous work has shown elevated implant temperatures, which are likely not amorphizing, exhibit better activation than implants that are partially amorphizing. This result may be be caused by a reduction in activation for implanted dopants in the amorphous regime relative to the non-amorphized regime. For this reason, a study was designed compare the activation of Si in amorphous InGaAs to Si in crystalline InGaAs.

A 220 nm thick amorphous region was formed in an InGaAs substrate by the combination of a 220 keV 3×10^{14} cm^{-2} As^+ implant with the 20 keV, 6×10^{14} cm^{-2} Si^+ implant performed at 20°C. For the non-amorphizing case the same 20 keV 6×10^{14} cm^{-2}

Si implant was performed at 250°C to prevent amorphization. Table B-8, located in Appendix B, details the complete implant and annealing conditions for samples used in the experiment outlined in section 6.3. Figure 6-1 shows the as-implanted microstructure of the two substrates used in this work indicating that the amorphized substrate formed a 220 nm thick amorphous layer. Figure 6-1c also indicates that the ALD encapsulation process performed at 250°C is sufficient to cause regrowth of the amorphous layer. Figure 6-2 indicates that upon annealing at 750°C for 5 s in the case of non-amorphizing implants loops defects are present while pre-amorphization results in regrown material that is highly defective with a large number of stacking faults and micro twins, consistent with previous observations of highly defective regrowth.

Figure 6-3 shows the as-implanted SIMS of the two substrates. It is obvious from the SIMS profiles that amorphization results in more abrupt profiles and a higher peak as expected with pre-amorphization. After implantation and SIMS, samples of the two substrates were encapsulated with 15 nm of the Al_2O_3 dielectric to prevent surface degradation upon annealing. Samples were annealed for 5 s at temperatures between 450 and 750°C. Figure 6-4 shows the post-anneal sheet number measurements for the crystalline and amorphous InGaAs substrates.

The activation in the pre-amorphized substrate is higher than that observed in the crystalline implant condition for 5 s anneal at 450°C suggesting that SPE might incorporate some dopants onto lattice sites but the amount of dopant incorporation is far from what is achieved for dopants in SPE of silicon. Upon annealing at increasing temperatures the pre-amorphized substrates exhibit steady improvements in active sheet number over the range of temperatures studied. Si implants in crystalline InGaAs

have the greatest change in activation once annealed at 550°C, which is consistent with previous reports of implants into III-V materials requiring annealing temperatures of at least 550°C to recover implant damage and move dopants onto lattice sites. The activation behavior of Si implants into crystalline substrates also shows steady improvements and a slightly higher active sheet number than implants into the pre-amorphized substrates.

The mobility in the pre-amorphized substrates is much lower than that of implants into crystalline substrates for all annealing temperatures. The likely reason for this large mobility difference is evidenced in the XTEM presented in Figure 6-2 of the pre-amorphized and crystalline substrates after annealing at 750°C for 5 s. After annealing at 750°C for 5 s the pre-amorphized InGaAs substrates still have a large number of stacking faults and microtwins. These stacking faults and micro twins likely contribute to increased scattering and a subsequent reduction in mobility. For crystalline InGaAs, there is a large drop in mobility after annealing at 550°C due the increase in scattering due to ionized impurities as inferred from the sheet number results of annealing at 550°C. The increases in mobility for the pre-amorphized substrate may indicate that more of the regrowth related damage is being annealed out but it is clear that lattice scattering and not impurity scattering as in the case of Si implants into crystalline InGaAs limit the mobility. Reductions in mobility result in the large deviation in sheet resistances for the amorphous and crystalline InGaAs substrates across the entire annealing range. Using the method outlined before, the post-anneal active Si concentration was calculated assuming limited diffusion. The result of this estimation is that the pre-amorphized Si actually exhibits slightly higher active concentration 1.0×10^{19}

cm^{-3} compared to the 0.9×10^{19} cm^{-3} in the amorphized substrate. This result is in sharp contrast to the previous result performed in GaAs that indicates Si shows no activation in amorphized material.[155]

There is limited usefulness of amorphization in processing of III-V devices but the results of this experiment are still instructive. This result gives provides convincing evidence for implant damage not being the reason for the observed limits of Si incorporation in ion implanted InGaAs. Amorphized substrates are clearly much more defective but the activation limit in these two materials is nearly identical which is still more consistent with point defect limited activation for the high Si^+ doses. The results of the pre-amorphization experiment are also consistent with previous conclusions from the co-implant study that indicate damage-related defects do no explain the activation limits of implanted Si in InGaAs. The similar activation levels further indicate that vacancy complexing is likely present in both amorphous and crystalline substrates upon thermal annealing. The electrical activation in amorphized InGaAs result is also a large deviation from previous work in GaAs which showed no activation of implanted Si dopants. The results of this study, which show the same limiting activation level for crystalline and amorphous substrates, are more consistent with activation being limited by a fundamental crystalline thermodynamic limit such as the case of Fermi-level dependent Si-V complexing.

6.4 Formation of Sub-Threshold Loop defects in Non-Amorphizing Implants in InGaAs

It is desirable to avoid amorphization in III-V semiconductors for reasons articulated previously as they are prone to exhibit highly defective regrowth which can result in extended defects and reduction in carrier mobility due to increased phonon

scattering. For ballistic limited transport, bulk mobility is likely to be less important than the materials effective mass but shorting of devices resulting from regrowth related defects could also pose a problem.

In non-amorphizing implants the non-conservative nature of implantation results in a large number of excess interstitials that coalesce into larger platelets of extended defect loops near the projected range of the incident ion and the peak of the interstitial population upon annealing. The calculated distribution of interstitials and vacancies for a 20 keV 6×10^{14} cm^{-2} Si^{+} implant into InGaAs is shown below in Figure 6-6 with an overlaid profile of as-implanted Si ions.

The subtrheshold defects are shown clearly in the XTEM in Figure 6-2a and Figure 6-7a. Annealing studies on these samples show in in Figure 6-7b-d have further shown that the defect loops are unstable and dissolve upon annealing at 750°C for times greater than 10 s.[297] The dissolution of subthrehold defects is interesting since this indicates that the excess interstitials occuring from implantation are being consumed or migrating to a free surface if the loop defects are to dissolve. In Si subthreshold and end of range defect loops are generally reported to be stable upon annealing and often times vacancy enegineering is performed to remove these defects.

HR-XTEM of a subthreshold loop defect is shown in Figure 6-8 and Fourier filtering more clearly that the defects are extrinsic stacking faults situated on close-pack planes. More specifically these defects are positive frank partials with b = a/3 <111> based on the Burgers circuit analysis. The nucleation of these defects was studied as function of annealing temperatures and implantation temperature in subsequent studies on species effects on defect dissolution.

6.5 Doping Effects on Sub-Threshold Defect Dissolution

In the case of Si^+ implanted materials it was noticed that subthreshold defects were unstable and showed limited growth prior to dissolving completely. The defects appeared to dissolving from the surface down based on the depth of the defect band forming beyond the projected range for anneals at 750°C. Implants of electrically active Si^+ were compared with isoelectronic P^+ implants in order to study the effect that electrical activity has on defect formation. P^+ implants were chosen since they have similar mass and range statistics to Si to aid in comparison. 80°C, 20 keV, 6×10^{14} cm^{-2} P^+ and Si^+ implants were implanted into InGaAs before being encapsulated with 15 nm of ALD Al_2O_3. Isothermal anneals were performed at 650°C using a RTA with anneal times ranging from 5 s to 600 s. A complete table of the samples used in the work in section 6.5 and section 6.6 is included in Table B-9 of Appendix B. SIMS of the as-implanted Si^+ and P^+ profiles used in this study are shown in Figure 6-9 indicating that the species have a co-incident projected range but it appears that the MOCVD substrates used in this work have a background P concentration of around 1×10^{19} cm^{-3}.

Figure 6-10a-b show XTEM of anneals performed at 550°C for 5 s on samples implanted at 80°C with a 20 keV 6×10^{14} cm^{-2} P^+ and Si^+ implant respectively. For anneals of 550°C there is no clear evidence in XTEM of loops forming but at 650°C the same implants begin to show a large number of loop defects forming at the projected range as shown in Figure 6-10c, d. Upon annealing at 750°C in Fig. 6-10e-f the defect loops are shown to coarsen for both P^+ and Si^+ implants but the top of the defect band in Si-implanted material is shown to move away from the surface whereas the P implant defect band is relatively unmoved from the projected range. Si implants after annealing

at 750°C also shown the formation of defects well beyond the projected range which is consistent with previous micrographs showing sub-threshold defects in Figure 6-2a and Figure 4-1. This study indicates that defect loops formed by Si implants do form at the projected range but the instability of defect loops upon annealing at 750°C for 5s is due to movement of observed band of defects beyond the projected range in the case of Si implants. These results suggest that the formation of dissolution of Si implant damage in InGaAs is unlike that of P implant damage.

From previous electrical activation results it was observed that dopant activation was limited until annealing at temperatures above 550°C and the lack of extended defect formation suggests that 5 s anneals at temperatures of 550°C or below are just on the edge of what is necessary to begin the recovery of damage in the implanted crystal. Based on these results, it was concluded that annealing temperatures of 650°C would be ideal to study the growth and dissolution of sub threshold defects in InGaAs as a function of annealing time.

Figure 6-11 shows XTEM of Si^+ and P^+ implants after annealing for 5, 40, 320 and 900 s. Defect loops for P implants (Figure 6-11a-d) appear to be larger in size and are shown to be located near the projected range after annealing. Loop type defects formed from Si implants (Figure 6-11e-f) appear to be smaller in than those of P implants and fail to grow. Upon annealing at 900 s at 650°C Si loops are shown to be much less numerous than those of P implants indicating that implant damage from Si implants are dissolving quicker than those occurring from P damage.

Plan-view specimens were also made to more accurately quantify the number of defects for each annealing conditions so that the number of interstitials in defect loops

could be calculated. Plan view TEM of the same samples in Figure 6-11(a-h) are shown in Figure 6-12(a-h).

Figure 6-13 shows the calculated number of interstitials contained in defect loops for P^+ and Si^+ implanted material as a function of annealing time. Since the loops were shown to be positive frank partials on the {111} plane, the {111} planar density of a diamond cubic lattice of InGaAs ($d_{\{111\}}$=1.34×10^{15} cm^{-2}) was used to calculate the number of interstitials bound by loops. The planar density value was multiplied by the total loop area and multiplied again by a factor of two since the loop defects consist of two extra planes that preserve the close pack spacing in the diamond cubic cell. Figure 6-14 clearly shows that a large number of interstitials is consumed in the annealing process of Si implants before a steady interstitial loop population is achieved. Short anneal times result in similar aerial interstitial densities for Si^+ and P^+ implants. The maximum number of interstitial in loops is less than the implanted dose for both implant species. In the case of Si, the number of interstitials bound by loops is shown to be 0.5×10^{14} cm^{-2} while the total interstitial population in loops for P implants is nearly 3 times higher around 1.5×10^{14} cm^{-2}. Previous experimenters have explained loop dissolution by invoking surfaces as interstitial sinks, but the projected range and co-incident profiles of Si and P implants as shown in Figure 6-10 indicate that the faster dissolution of Si implant related defect cannot be due to surface effects since P implants do not reduce in interstitial population. The results of this study suggest that Fermi level effects play a role in defect evolution, so a second experiment using only isoelectronic P^+ implants into electrically active n-type and nominally un-doped InGaAs was performed.

6.6 Isoelectronic implants into Heavily Si-doped and Unintentionally Doped InGaAs Substrates

For this experiment, a P implant was performed into a nominally un-doped MOCVD structure as well as a heavily Si doped structure grown by MBE used in the previous deactivation experiments in chapter 5. SIMS of the implanted P profile is shown in Figure 6-14 and is overlaid on the as-grown Si concentration indicating that the peak of the P implant is centered in heavily Si doped region. Figure 6-15 shows the XTEM of the 80°C, 20 keV, 6×10^{14} cm^{-2} P^{+} implant into the (a) nominally un-doped and (b) heavily doped substrates as well as PTEM of the (c) nominally un-doped and (d) heavily doped substrates after annealing at 650°C for 300s. PTEM images of the same samples in Figure 6-15c and Figure 6-15d indicate that the unintentionally doped MOCVD films have 1.5×10^{14} cm^{-2} interstitials bound by loops while the heavily doped MBE films resulted in 1.5×10^{13} cm^{-2} interstitials bound by loops. From this experiment it is clear that background doping with Si has an effect on the evolution of interstitial loops formed by implantation.

6.7 Discussion of Fermi Level Effects on Extended Defect Dissolution

The evidence presented so far clearly indicates that extended defect growth and evolution in Si implanted is much different than what is observed for P implanted InGaAs. Previous studies of Si^{+} implants into GaAs have also been shown to be unstable but these results were never compared systematically to isoelectronic implants that create similar damage and co-incident profiles.[80], [180], [210], [298] Si clearly plays a role in formation behavior of loops due to excess interstitials based on implants of P into undoped and heavily Si doped InGaAs. This result is consistent with previous

observations that the addition of electrically active Si might be creating vacancies which are capable of combining with the excess interstitials and dissolving the loops.

From previous experiments in this work it was hypothesized that group III vacancies $(V_{III})^{3-}$ provide a more concise explanation for the common doping limits of Si and S co-implanted materials as well as provide an explanation for the heavily concentration dependent diffusion observed for high doping concentrations of Si. Similarly, the high implanted concentrations for the Si implants used in this defect study will also result in a large number amount of compensated Si based on the previous electrical measurements for the same implant and annealing conditions. In previous studies of electrical activation and diffusion there is no direct evidence of these vacancies being present but the defect dissolution behavior observed for Si implants as well as P implants into heavily Si doped material provide the best indirect evidence so far of high vacancy concentrations in heavily n-type, Si doped InGaAs. Positron annihilation studies also indicate that heavy n-type doping leads to a large number of vacancy defects in GaAs that could influence the evolution of interstitial loops formed by isoelectronic P implants.[137], [273], [299], [300] Enhanced defect dissolution in n-type materials due to Frenkel pair formation is seemingly consistent with the amphoteric native defect model proposed by Walukiewicz and other experimenters have also reported on defects formed by isoelectronic Al implants into GaAs being more stable in p-type GaAs than nominally un-doped GaAs.[71] Previous experiments may also elucidate the observed motion of the defect band in Si implanted InGaAs. Studies of heavily Si doped InGaAs sub-collectors in heterojunction bipolar transistors have indicated that the formation of group III Frenkel pairs ($V_{III} + i_{III}$) in the heavily doped

subcollector act as a source of interstitials which enhance Zn diffusion in the base region.[301] The injection of interstitials from the formation of Frenkel pairs in heavily Si-doped, vacancy-rich, region near the projected range in the Si implanted film may result in interstitials being continually injected beyond the vacancy rich region. The injection of interstitials out of the heavily n-type region gradually moves the defect band beyond the projected range. The formation of larger defects well beyond the projected range in the case of Si^+ implantation may be due to either the increased stability of interstitial loops to grow in the nominally un-doped region beyond the Si profile or the gettering of interstitials at impurities in the MOCVD substrate. There was no evidence from XTEM of these larger defects forming beyond the projected range in the case of isoelectronic, P^+ implantation, presumably due to a lack of interstitial injection occurring from Frenkel pair formation in the case of isoelectronic implants.

In conclusion, the observed difference in defect evolution of P^+ and Si^+ implanted substrates is likely due to Fermi level effects which result in high vacancy concentrations with heavy n-type doping. Frenkel pair formation in heavily n-type materials can explain the enhanced extended defect dissolution in n-type substrates as well as the difference in defect stability of P implants and Si implants. Interstitial injection due to Frenkel pair formation can also explain the creation of the defect band beyond the projected range and the formation of loop defects well beyond the projected range in the case of Si implants. Large increases in vacancy defects are also consistent with the other reports of concentration dependent diffusion, and compensated activation observed in heavily Si doped substrates in previous sections of this work.

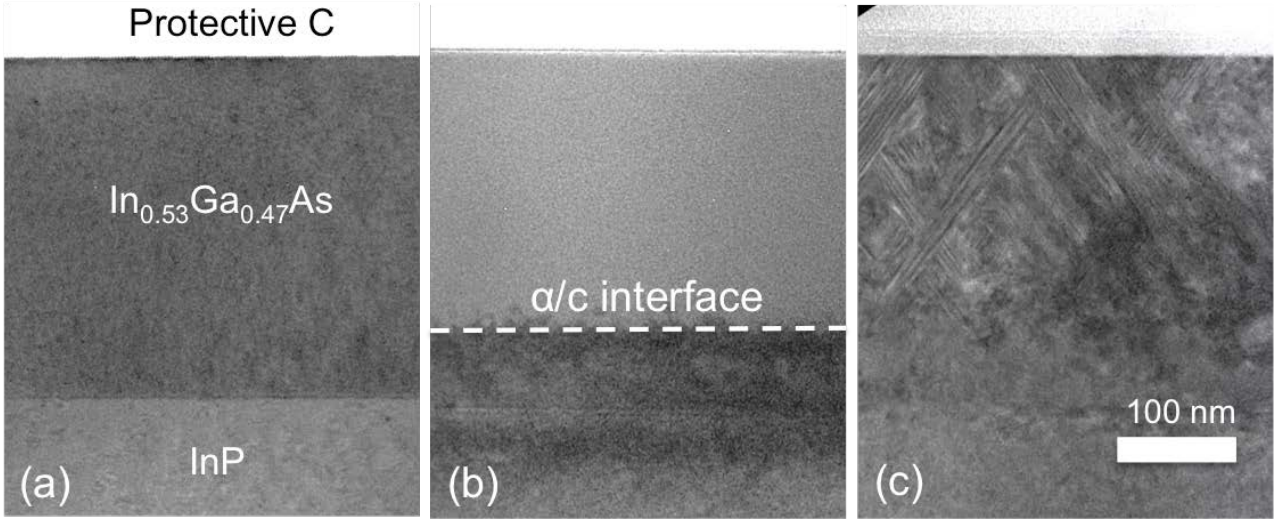

Figure 6-1. Post implant and post capping XTEM for non-amorphizing and amorphizing implants into InGaAs. Micrographs correspond to (a) as-implanted 20 keV, 6×10^{14} cm^{-2} Si^{+} at 250°C, (b) as-implanted 220 keV 3×10^{14} cm^{-2} As^{+} and 20 keV, 6×10^{14} cm^{-2} Si^{+} at 20°C and (c) 220 keV 3×10^{14} cm^{-2} As^{+} and 20 keV, 6×10^{14} cm^{-2} Si^{+} at 20°C after ALD dielectric encapsulation at 250°C indicating amorphous InGaAs can regrow at temperatures of 250°C.

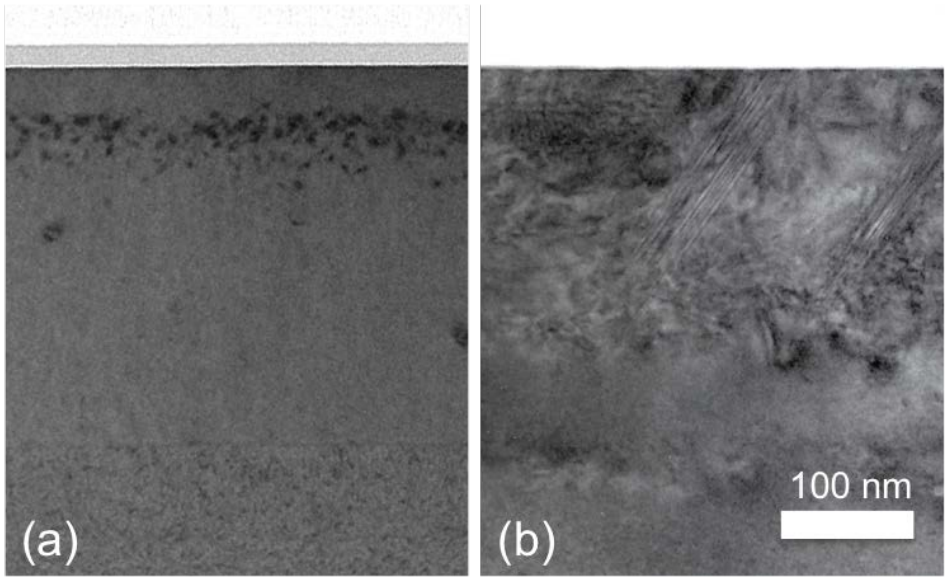

Figure 6-2. Post anneal XTEM of non-amorphizing and amorphizing implants into InGaAs. Micrographs correspond to a post 750°C 5 s RTA XTEM of (a) 20 keV, 6×10^{14} cm^{-2} Si^{+} at 250°C, (b) 220 keV 3×10^{14} cm^{-2} As^{+} and 20 keV, 6×10^{14} cm^{-2} Si^{+} at 20°C. The pre-amorphized substrate in (b) shows a large amount of regrowth related defects even after undergoing high annealing temperatures.

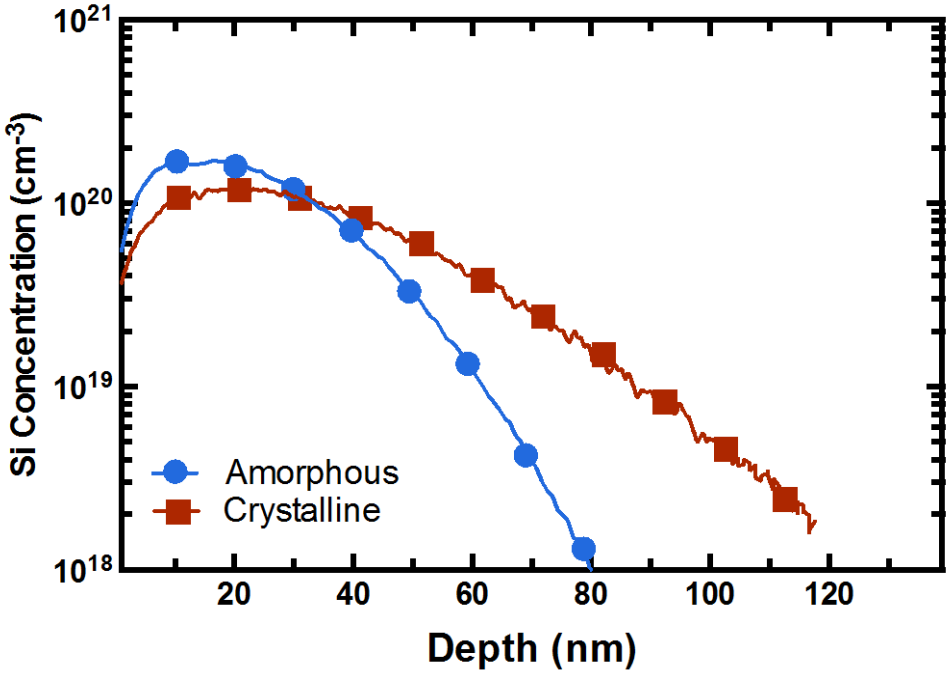

Figure 6-3. Si concentration as a function of depth as determined by SIMS. Concentration profile is for a 20 keV, 6×10^{14} cm^{-2} Si^{+} at 250°C (non-amorphizing) implant and for a pre-amorphized 220 keV 3×10^{14} cm^{-2} As^{+} and 20 keV, 6×10^{14} cm^{-2} Si^{+} at 20°C. Pre amorphization results in significant reductions in random channeling.

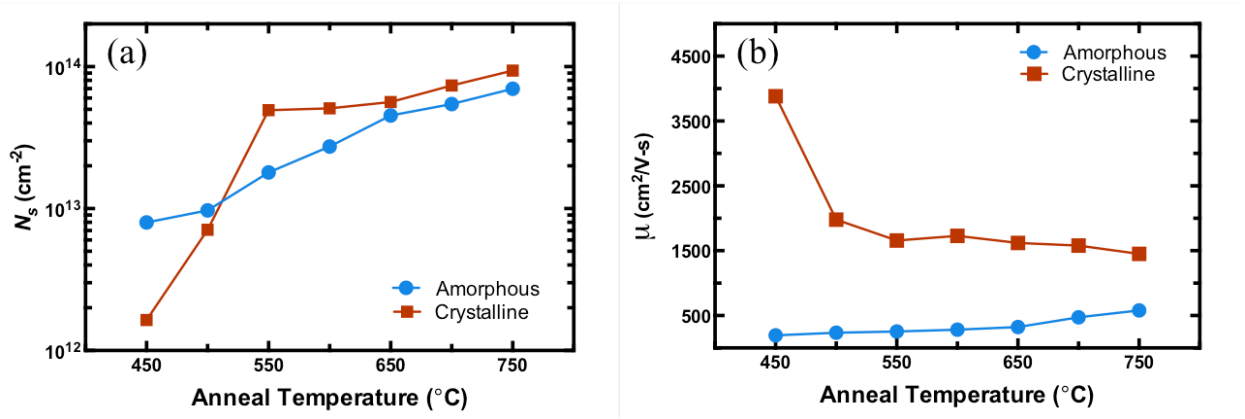

Figure 6-4. Active sheet number and mobility as a function of annealing temperature for non-amorphizing and amorphizing implants. Active sheet number (a) and mobility (b) for a 20 keV, 6×10^{14} cm^{-2} Si^{+} at 250°C non-amorphizing implant and for a pre-amorphized 220 keV 3×10^{14} cm^{-2} As^{+} and 20 keV, 6×10^{14} cm^{-2} Si^{+} at 20°C as a function of annealing temperature are shown.

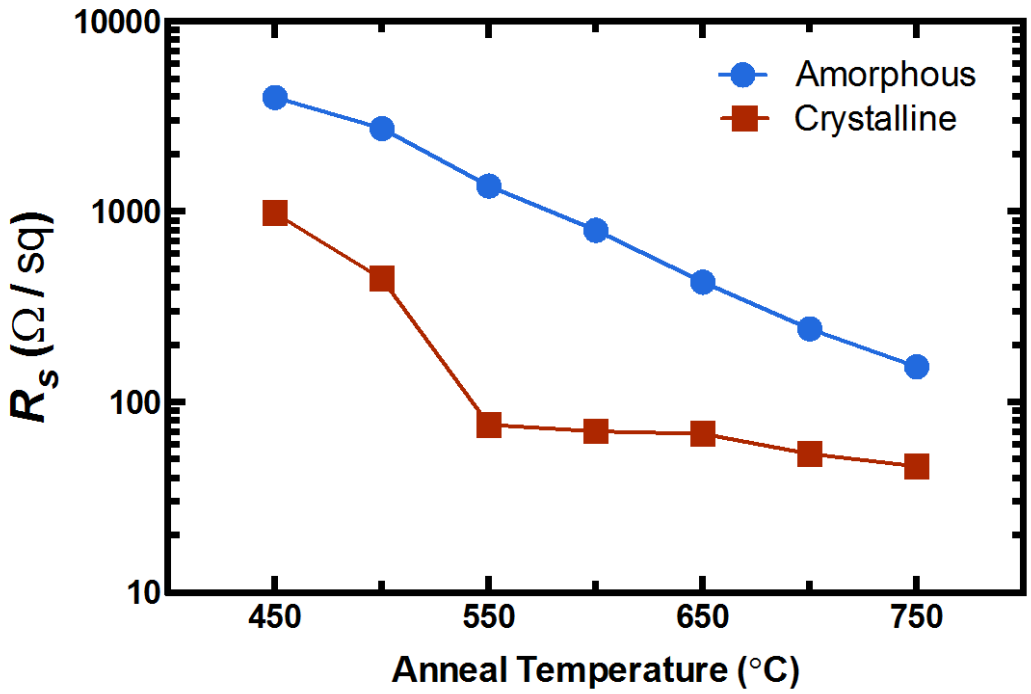

Figure 6-5. Sheet resistance as a function of annealing temperature for amorphous and crystalline substrates. Measurements are for 5 s RTA for 20 keV, 6×10^{14} cm^{-2} Si^{+} at 250°C non-amorphizing implant and for a pre-amorphized 220 keV 3×10^{14} cm^{-2} As^{+} and 20 keV, 6×10^{14} cm^{-2} Si^{+} at 20°C.

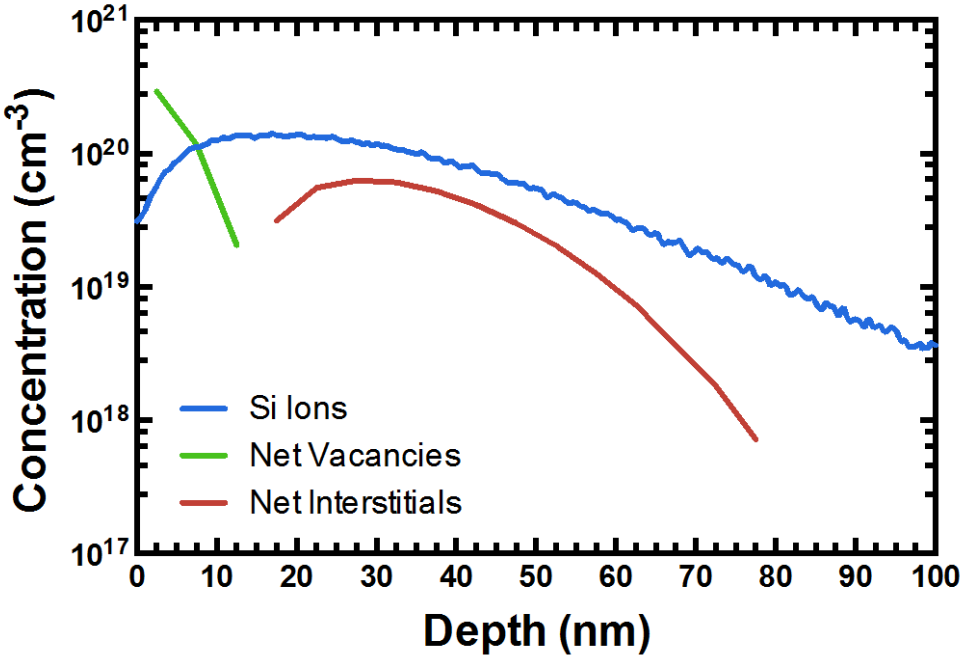

Figure 6-6. Calculated concentration of Si, net vacancies, and net interstitials. Calculation is for a 20 keV, 6×10^{14} cm^{-2} Si^{+} implant in to InGaAs using the Boltzmann transport equations.

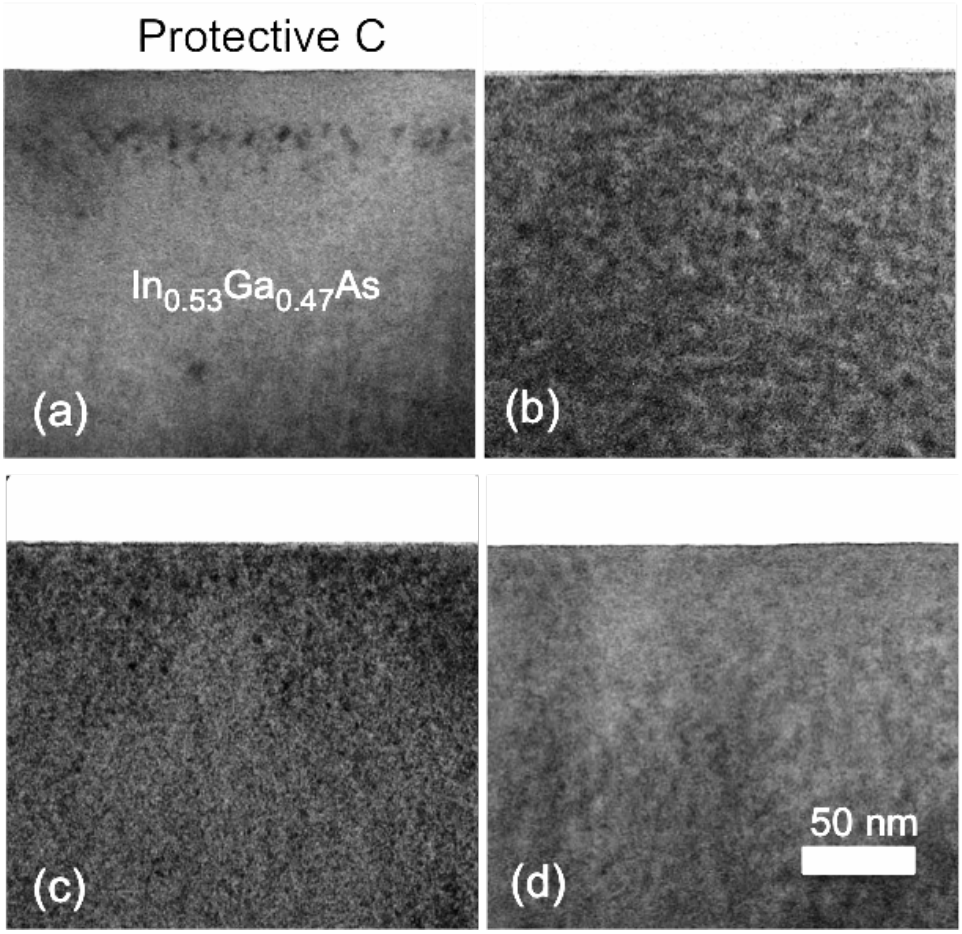

Figure 6-7. Post 750°C RTA XTEM of 10 keV, 5×10^{14} cm^{-2} Si^{+} at 80°C. Micrographs are after (a) 5 s RTA, (b) 10 s RTA, (c) 20 s RTA and (d) 40 s RTA.

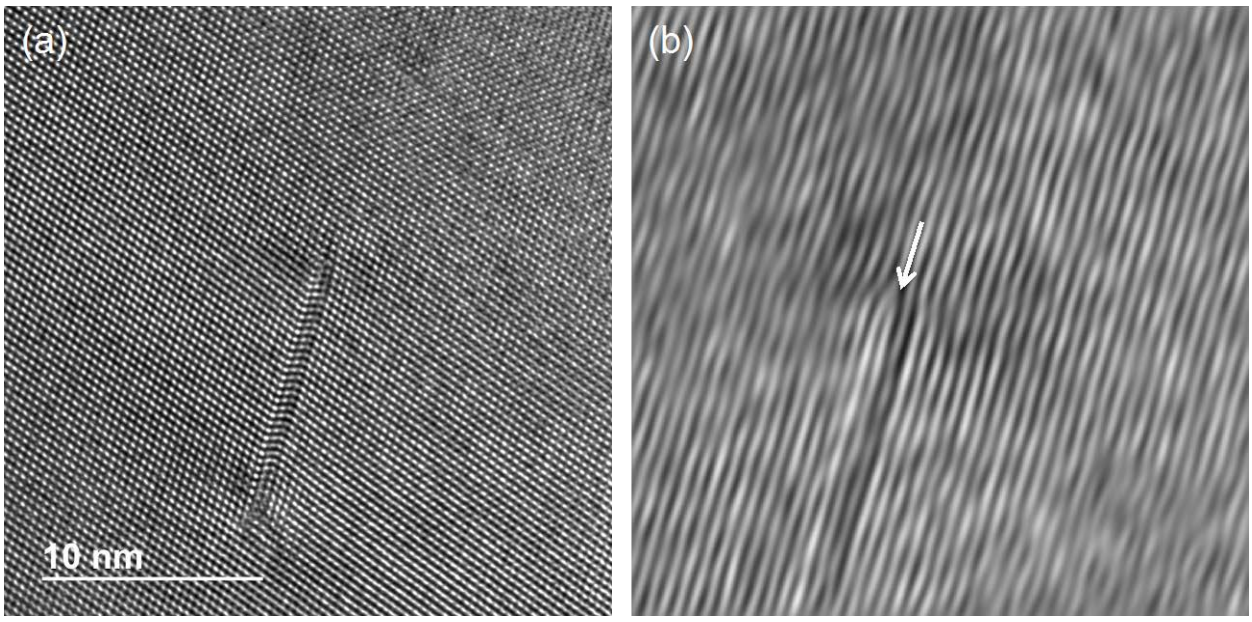

Figure 6-8. Micrographs of extrinsic defect loop from P implant into InGaAs. Micrographs are of (a) HR-TEM of loop defect formed by 20 keV, 6×10^{14} cm^{-2} P^+ at 20°C after annealing for 320 s at 650°C and (b) FFT of (a). It is clear from the FFT that the loops that are formed are extrinsic as indicated by the extra planes of atoms.

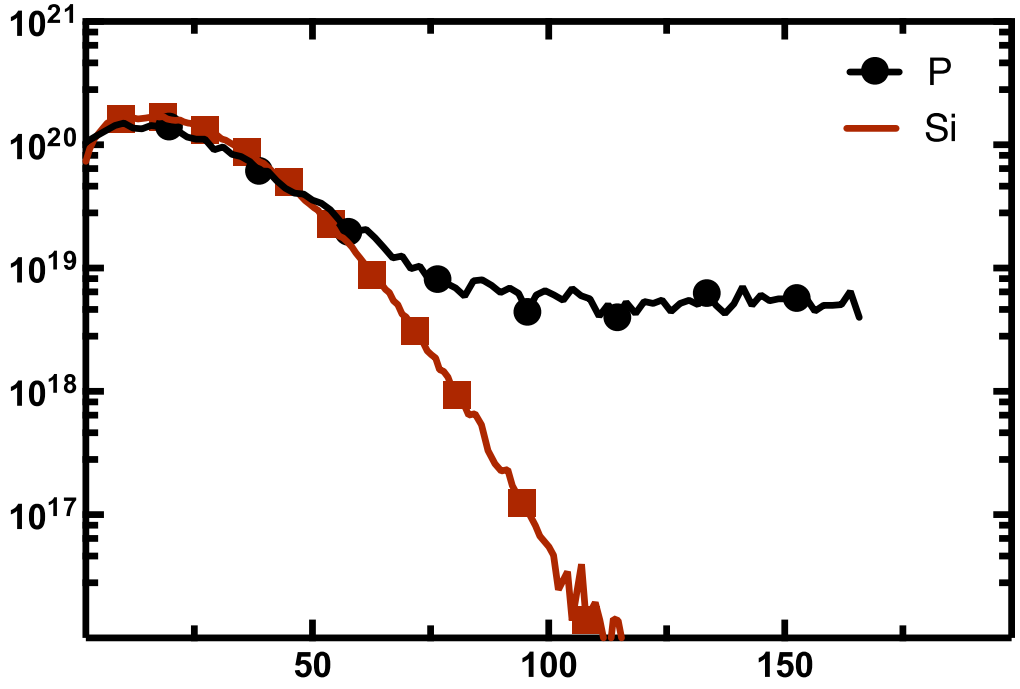

Figure 6-9. Si and P concentration as a function of depth a determined by SIMS. SIMS of as-implanted 80°C, 20 keV, 6×10^{14} cm^{-2} P^{+} and 80°C, 20 keV, 6×10^{14} cm^{-2} Si^{+}. MOCVD grown InGaAs on InP is shown to have a large background concentration of P equivalent to 1×10^{19} cm^{-3}.

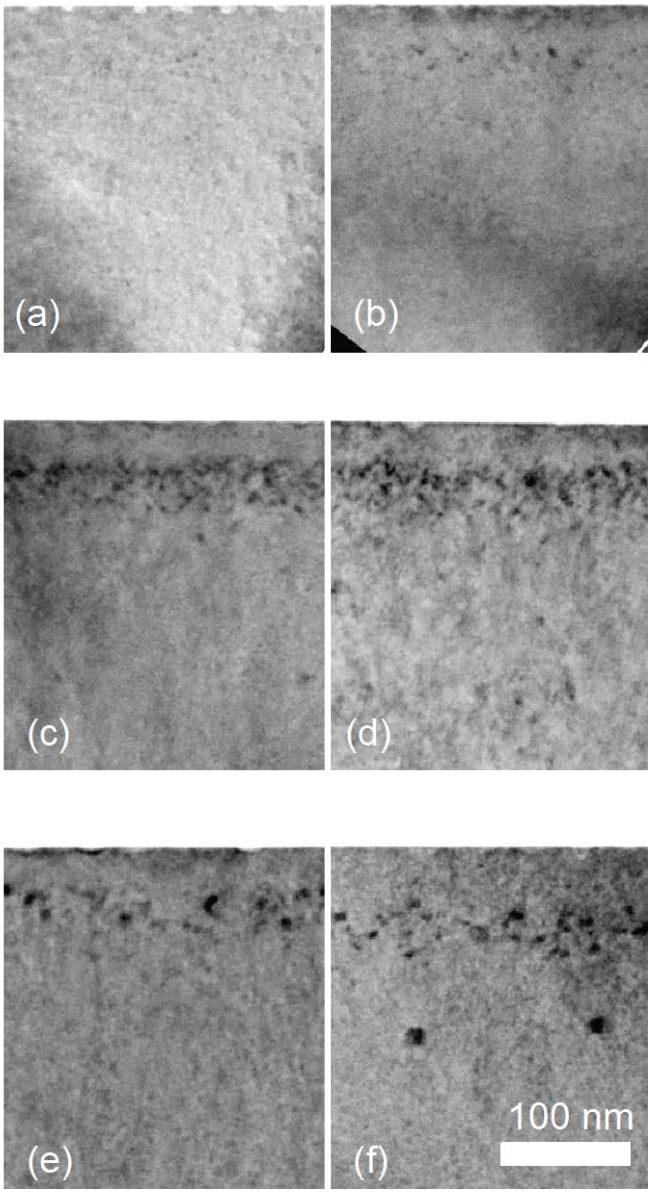

Figure 6-10. Subthreshold defect loops from Si and P implantation in InGaAs at varying annealing temperatures. Micrographs are post anneal XTEM of a 80°C, 20 keV, 6×10^{14} cm^{-2} (a) P^+ for 5 s at 550°C (b) Si^+ for 5 s at 550°C (c) P^+ for 5 s at 650°C (d) Si^+ for 5 s at 650°C (e) P^+ for 5 s at 750°C (f) Si^+ for 5 s at 750°C

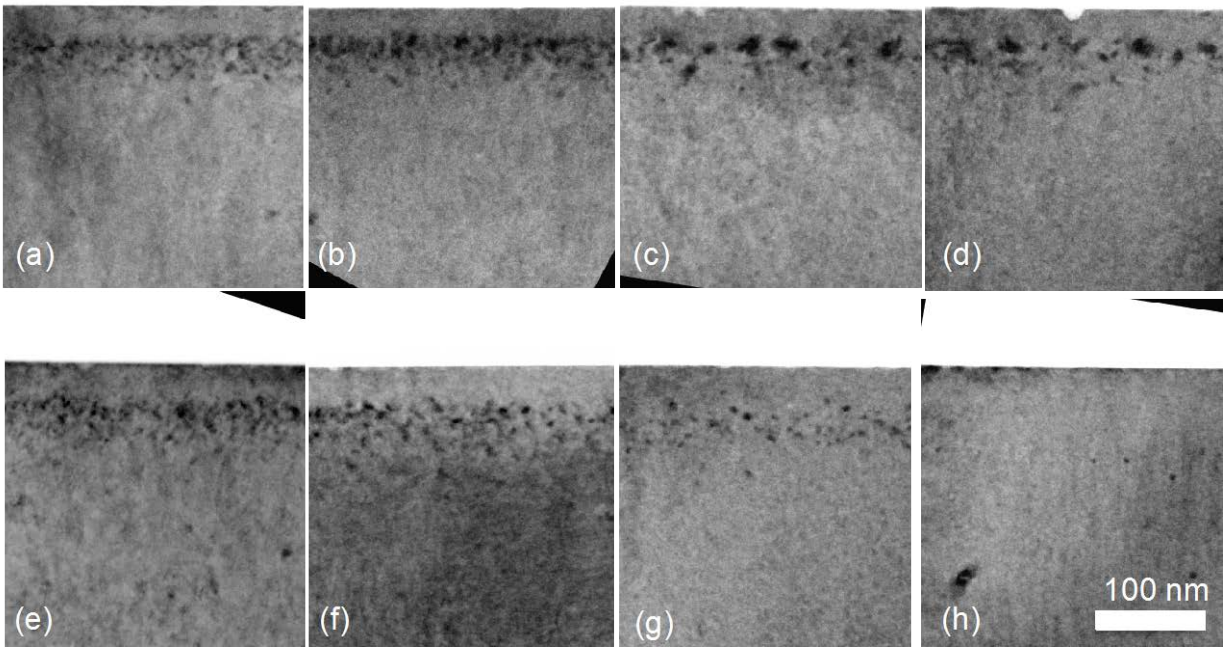

Figure 6-11. XTEM of subthreshold defect loops as a function of annealing time for Si and P implants into InGaAs. Post anneal micrographs are of a 80°C, 20 keV, 6×10^{14} cm^{-2} P^{+} after 650°C RTA for (a) 5 s (b) 40 s (c) 320 s (d) 900 s and 80°C, 20 keV, 6×10^{14} cm^{-2} Si^{+} after 650°C RTA (e) 5 s (f) 40s (g) 320 s (h) 900 s

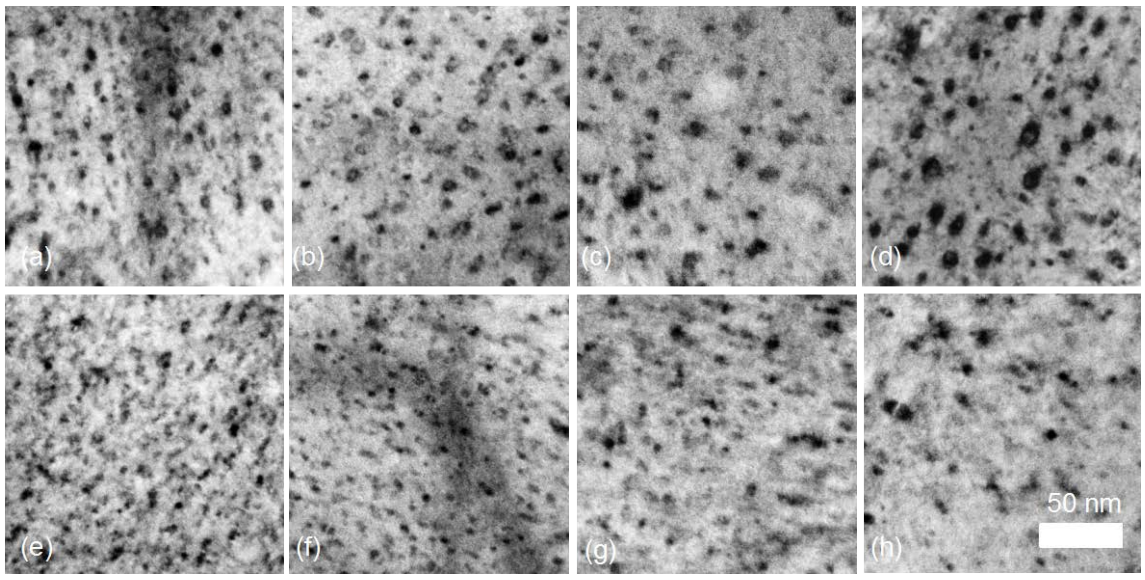

Figure 6-12. PTEM of subthreshold defect loops as a function of annealing time for Si and P implants into InGaAs. Post anneal micrographs are of a 80°C, 20 keV, 6×10^{14} cm^{-2} P^{+} after 650°C RTA for (a) 5 s (b) 40 s (c) 320 s (d) 600 s and 80°C, 20 keV, 6×10^{14} cm^{-2} Si^{+} after 650°C RTA (e) 5 s (f) 40 s (g) 320 s (h) 600 s

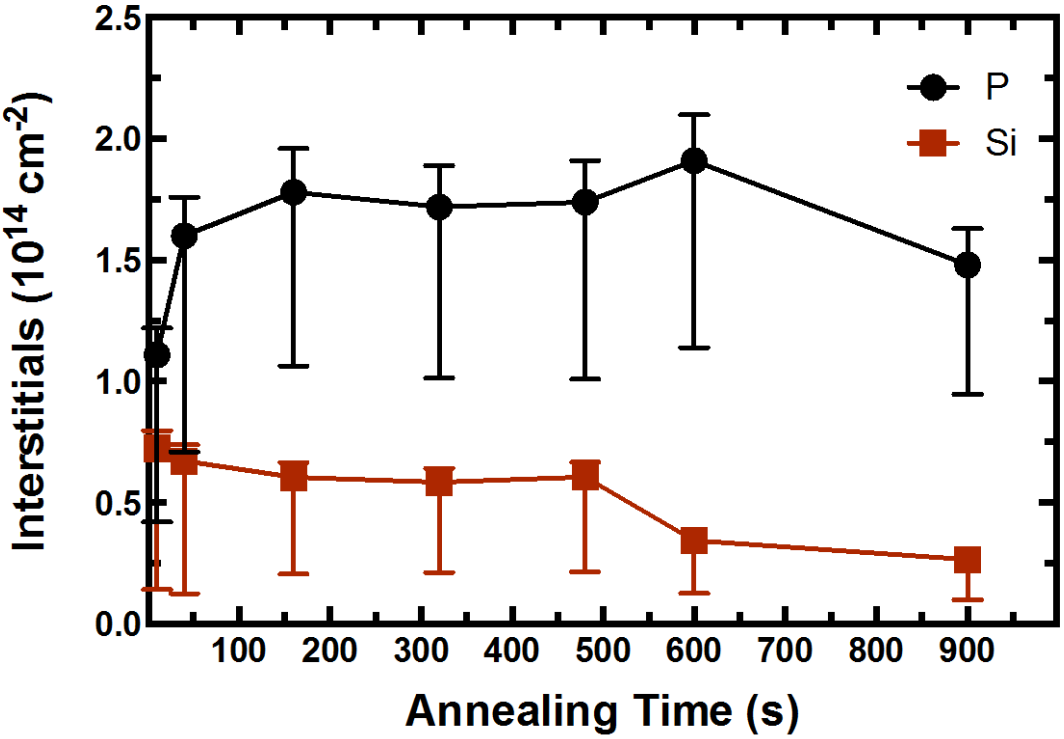

Figure 6-13. Plot of total number of interstitials contained in loops as a function of annealing time at 650°C. Measurements are for 80°C, 20 keV, 6×10^{14} cm^{-2} P^{+} and Si^{+} implants.

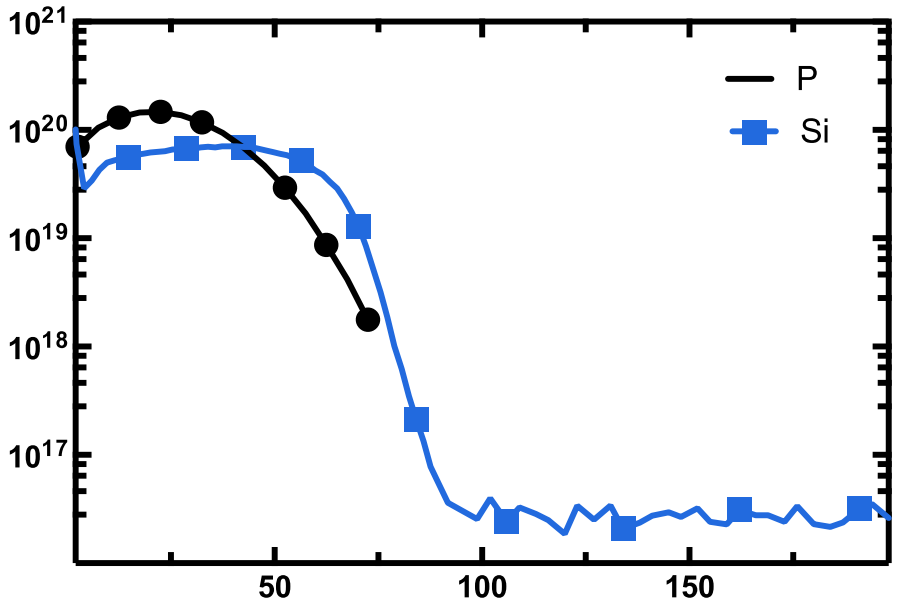

Figure 6-14. Implanted P and grown in Si concentration as a function of depth as determined by SIMS.

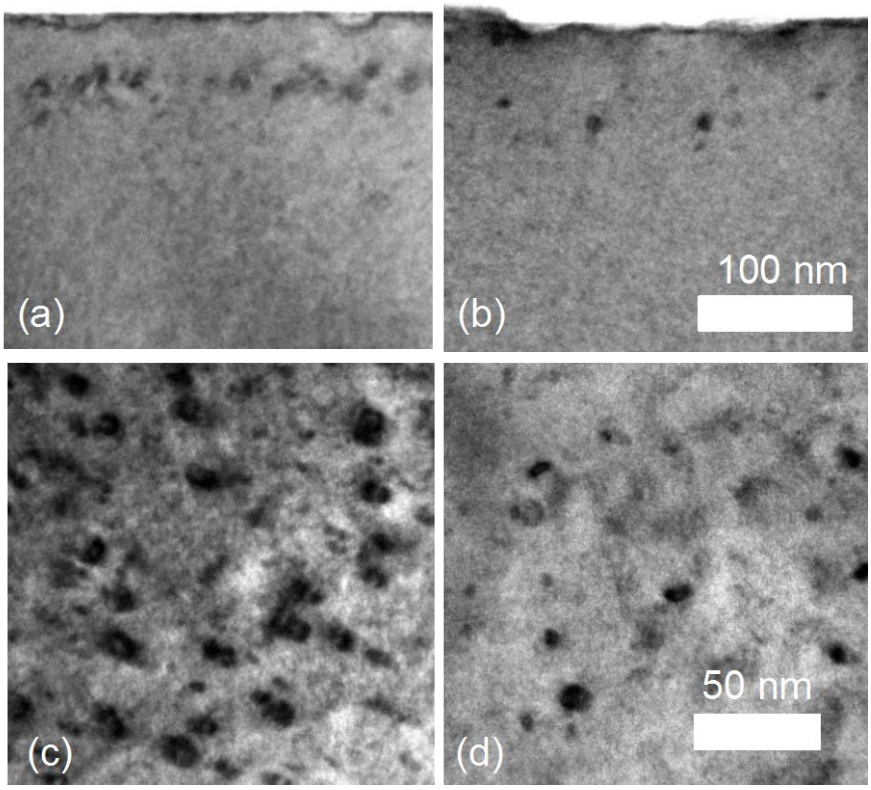

Figure 6-15. XTEM and PTEM of dislocation loops in heavily doped and nominally undoped InGaAs. Micrographs are of post anneal XTEM of a 80°C, 20 keV, 6×10^{14} cm^{-2} P^{+} implant after 300 s 650°C RTA of (a) nominally un-doped MOCVD InGaAs substrate (b) heavily Si doped MBE substrate and PTEM of (c) nominally un-doped MOCVD InGaAs substrate (d) Heavily Si doped MBE InGaAs

CHAPTER 7
CONCLUSIONS

7.1 The Role of Point Defects on Si Activation and Diffusion and N-Type Doping Limits in InGaAs

There has been much speculation on the part of previous experiments as to the nature of self-compensation of Si implanted into in InGaAs and related III-V materials such as GaAs. The four historically hypothesized reasons for upper activation limits of n-type dopants in ion implanted InGaAs are 1) chemical solubility limited activation for group IV or group VI dopants 2) amphoteric self-compensation in the case of group IV dopants or 3) implant damage compensation, and 4) defect limited activation. Initial experiments with ion implantation generally believed that the limited activation of Si in InGaAs was due to the amphoteric self-compensation of these dopants or due to limited chemical solubility. Arguments for chemical solubility limited activation have perhaps the least convincing evidence given the lack of increasing dopant solubility with increasing anneal temperature or the lack of evidence of large amounts of immobile Si clusters in post anneal SIMS of Si in InGaAs or GaAs or the results of RBS/PIXE experiments indicating that for the most part Si is substitutional even for heavily compensated doses. Comparison of Si activation in heavily-damaged, regrown layers and nominally defect free layers suggests that implant damage itself does not prevent dopant activation and the fact that intermediate temperature implants which are shown to be more damaging than high temperature implants have higher Si activation in InGaAs echoes the same conclusion.

There is good evidence that Si can behave as an amphoteric dopant especially in MBE experiments were the group III/V ratio can be modulated to cause Si to preferentially occupy one site over the other or the surface adsorption of Si dopants can

be caused to happen on completely Ga or As terminated surfaces. In ion implant experiments where the there is a pre-existing stoichiometric ratio of group III to group V sites there is limited evidence of anomalous activation except for a few reports which indicate that at very high annealing temperatures Si can undergo type changes from n to p type in GaAs. Previous MBE experiments also do not indicate whether the p-type doping of Si in GaAs is stable on post-growth anneals. There are no reports of type switching behavior of Si in the case of InGaAs but very high annealing temperatures in these materials tend to result in large amounts of surface degradation if processed over 850°C. Challenges in resolution with Raman or EXAFS in the ternary system to look for direct evidence of sublattice site occupation in these materials limits the ability to say with certainty how much Si is sitting on group III or group V sites. Raman experiments themselves have no good way to calibrate the compensation ratio of donor configurations to acceptor configurations and all that can be stated is that there is commensurate intensity shift in the intensity of Si_{III} to Si_{As}. At high doping concentrations, there is also no obvious effect of co-implants, which should be able to effectively modulate site selection of Si dopants as shown in III-V growth papers.

Perhaps the best evidence against the amphoteric interpretation of limited dopant activation is the preponderance of evidence for high concentrations of point defects at high Si doping concentrations. The heavily concentration dependent diffusion of Si suggests that at high Si concentrations there is an excess of point defects which allow for the enhanced Si motion. Si concentrations above 3×10^{19} cm^{-3} are shown to be highly mobile yet compensated. The $(Si_{Ga}\text{-}V_{Ga})^{2-}$ complex appears the be the dominant diffusion mechanism in GaAs from computational studies and would readily explain the

possibility of mobile, yet inactive Si. P-type carriers from Si_{As} could explain the compensation but this configuration is not expected to be mobile and DFT calculations also suggest that the V_{Ga}^{3-} defect to be more stable at higher shifts of the Fermi level towards the conduction band. This result is also echoed in the results of quantum well intermixing studies, which indicate that heavily n-doped Si superlattice structures have much more inter-diffusion of group III species than group V species. The enhancement in extended defect dissolution formed by ion implantation in heavily n-type materials also results for convincing evidence that in heavily n-type substrates there is an excess of cation vacancies that could complex with n-type dopants that can explain the observed compensation. Positron annihilation spectroscopy studies also regularly indicate that as-grown heavily n-type GaAs has a large increase in vacancy defects.

Based on the results of other experimenters and the results in this work it appears that the most likely explanation for the observed electrical compensation, concentration dependent diffusion and enhancement in extended defect dissolution in n-type materials is the presence of large numbers of cation vacancies which are able to form inactive complexes with n-type dopants in InGaAs. This understanding explains the majority of observations detailed in proceeding chapters such as the heavily concentration dependent diffusion, lack of co-implant effects, similar activation limits in group IV and group VI dopants, and the Fermi level effects on extended defect dissolution. Based on the understanding advanced in this work, a brief discussion of optimization for processing n-type InGaAs is warranted.

7.2 Optimization of Implantation Conditions

The evidence presented in this work suggests a few routes to improving the activation of ion-implanted material. In the case of modern finFET or future nanowire

devices it is clear that amorphization should be avoided in order to prevent poor regrowth of the amorphized material. Studies of elevated temperature implants show that the temperature required to avoid amorphization is only in the range of 50-100°C for high enough doses that saturation occurs. Intermediate temperature implants are also shown to activate quicker than implants performed at higher temperatures that encourage more dynamic annealing or at lower temperatures that result in amorphization.

Perhaps one of the most important controls in activation of implanted Si is the selection of implant dose. There is no benefit to implanted doses that result in peak implanted concentrations above 3×10^{19} cm^{-3}. Implanted Si above this concentration is not shown to be active and it instead shows heavily concentration dependent diffusion. Implants with peak concentration profiles below 1.5×10^{19} cm^{-3} will show much more limited diffusion and will not result in the maximum saturated activation of 1.5×10^{19} cm^{-3}. A narrow window of peak-implanted concentrations between 1.5×10^{19} cm^{-3} and 3×10^{19} cm^{-3} will result in saturated or nearly saturated activation but also minimize Si redistribution since the Si concentrations are below what is shown to result in heavily concentration dependent diffusion. It seems that some Si motion is necessary to result in maximized activation and this motions is strongly dependent on implanted concentration but the appropriate dose and annealing would be enough that some Si motion occurs to cause saturation but not so much that Si causes significant motion.

7.3 Optimization of Thermal Processing

Any thermal treatment seeking to optimize the activation of implanted dopants must first prevent any sort of surface degradation. Proper annealing ambient,

encapsulation and limited thermal budgets to prevent surface degradation might all be employed to prevent the preferential loss of group V materials from the surface which can change site stoichiometry and potentially influence activation or even prevent proper alloying or metallization of contacts. Optimization of thermal anneals for implants must also be such that damage can be recovered and that Si motion is limited, but results in saturated activation.

Thermal treatment of grown in Si must be careful to also prevent surface degradation but due to the meta-stability of grown in concentrations above 1.5×10^{19} cm^{-3} subsequent annealing processes should be limited to temperatures below the growth temperature or use annealing treatments that are far from equilibrium to prevent deactivation.

7.4 Optimization of Dopant Selection

Si^{+} and S^{+} has been used in implantation because as lighter species they are far less damaging than other implants such as Se, Sn, and Te but some experimenters have had good success using Sn and Te as grown in dopants for creating heavily doped InGaAs and InAs layers.[51], [52], [302] Deactivation results of Te dopants indicate that these dopants may also be compensated by complexing with group III cation vacancies but the large radius of these dopants may result in preferential diffusion of Te on the group V sublattice rather than the group III sublattice. In this case, the dopants may become heavily compensated due to complexing excess group III vacancies but they will still show limited diffusion and will likely not show the same heavily concentration dependent diffusion exhibited by n-type dopants that diffuse via group III vacancy mechanisms. Se implants have shown similar activation to Si implants in previous studies and it is possible that Se will diffuse via a group V vacancy

mechanism. In this case, the diffusion would be lessened and it might be an attractive choice for further explorations although it seems unlikely that Se or Te will result in higher activation than achieved with Si but the potential for reduction in complications from dopant diffusion could be worth pursuing Se or Te doping in InGaAs or InAs.

7.5 Materials Selection for Improving Contact Resistances

For the Si-InGaAs system is appears that the maximum stable carrier concentration is 1.5×10^{19} cm^{-3}. It has been known for some time that InP and group III-P materials have n-type carrier limits nearer to 1×10^{20} cm^{-3}. In the case of grown materials, it may be possible to grown InGaAs/InP heterostructure with heavily doped InP regions that are perfectly contacted to InGaAs. Another strategy already in heavy use for III-V devices is the alloying of GaAs or InGaAs down to InAs. InAs has slightly higher stable electron concentrations closer to $0.6\text{-}1\times10^{20}$ cm^{-3}. InAs also has the further benefit of having its Fermi level pinned in the conduction band, which further reduced contact resistances. The InGaAs/InAs system is also ideal given that it can alloy easily with Ni and results in an epitaxial Ni-InGaAs intermetallic phase[207], [303], [304]. This might make this system more favorable over InP or other materials since it will allow for the easy creation of self-aligned Ni contacts.

APPENDIX A
LESSONS LEARNED AND FAILED EXPERIMENTS

A.1 Prevention of Surface Degradation

Multitudes of previous attempts to prevent surface degradation in III-V's exist. Some of the first attempts were the use of proximity caps made of other III-V wafers or even Si that the samples were annealed on top of. During the early stages of these experiments multiple methods were tested to prevent surface degradation of the InGaAs. One of the first methods employed was the use of a proximity cap of either GaAs or InGaAs. It was immediately evident that these methods failed to prevent even macroscopic surface degradation at annealing temperatures of 850°C but samples annealed at 750°C looked specular to the unaided eye. Subsequent analysis in the SEM showed that even specular surfaces had pits and obvious surface degradation on the order of 0.5-3 μm and there was limited evidence to indicate that using a III-V wafer was that much better than even just Si as a proximity cap. For previous experiments that used very high energy implants, specular surfaces might be sufficient to prevent large amounts of implanted dose loss but it was clear that proximity capping would not be sufficient to prevent dose lose from implants with a projected range of 20 nm or less as was used in this study. It is the opinion of this author to be highly skeptical of electrical activation results and the results of profiling near the surface of implants in previous experiments that used proximity caps and do not show microscopic evidence of adequate surface protection from encapsulation.

Other experimenters also relied heavily on dielectric encapsulation formed by PECVD methods. PECVD is versatile in that SiO_2, Si_3N_x, and even SiO_xN_y can all be formed and used as encapsulant materials. Typically, the deposition rate of these is

also very high on the order of 10-50 nm per minute. It is desirable to make thin layers that can accommodate thermal stress well but also have the uniformity that prevent pinholes and other defect from forming. PECVD SiO_2 was shown to prevent obvious macroscopic surface degradation up to 850°C and TEM for 50-100 nm thick cap layers showed that at 750°C for InGaAs some surface degradation was present but it would have not been observable in SEM given that the defects were from pits of 25 nm or less. Even this amount of surface degradation would result in reductions in activation due to dose loss if a large enough area were covered. Other experiments previously used ALD as well to deposit much thinner layers that could better accommodate thermal stresses but also have good enough uniformity that pinholes and other defects were limited.

The first attempt to use ALD settled on a thermal exposure mode recipe that resulted in a 15 nm thick layer and direct comparison in TEM of these samples to the PECVD encapsulated samples annealed at 850°C indicated that the ALD encapsulated were much better at preventing surface degradation than the PECVD encapsulated samples. Based on these results, it was decided that the best way forward would be to settle on the use of a 15 nm ALD cap formed by thermal exposure and limit annealing to 750°C or less. No subsequent improvements were made to the cap over the course of the work in an effort to keep the capping process consistent such that subsequent experiments could be directly compared without complication of varying capping procedures or thicknesses. The capping materials and process used here is by no means optimized but it is sufficient to prevent surface degradation that could result in erroneous electrical measurements from experiment to experiment.

One unintentional discovery was that the thermal exposure mode resulted in improved surface protection over non-exposure mode recipes. At one point samples were sent to Georgia Tech to undergo ALD encapsulation on the same model of equipment but instead of the exposure mode a standard thermal recipe was used. In exposure mode, the precursors are allowed to sit 5 minutes between pulses to allow for more surface diffusion whereas in the standard mode the wait time between pulses is less than a minute. Both methods resulted in similar layer thicknesses but it was clear after thermal treatments and subsequent TEM investigation that not using exposure mode resulted in worse surface protection. Exposure mode was originally intended to cover high aspect ratio features but it was evident that it also must have made better encapsulation layers. The drawback of exposure mode is that to place 15 nm of Al_2O_3 requires a 13-hour run time whereas the normal thermal mode can be completed in less than an hour.

A.2 Laser Annealing of Si Implanted InGaAs

Laser annealing has come into more frequent use since the short anneal times of ms or less and high temperatures can be achieved. Higher annealing temperatures often results in increased dopant activation while limited annealing times minimize diffusion. An early goal of this work was to investigate whether laser annealing was effective for increasing the dopant activation of Si in InGaAs.

The first investigation of laser annealing in this work relied on a die-by-die laser anneal from a 532 nm laser operated by Applied Materials. The initial problem with this method was that it was nearly impossible to calibrate the surface temperature of the InGaAs based on the optical observation of a melting transition or optical pyrometer reading since the direct band gap InGaAs had the propensity to fluoresce and

overwhelm the optical detection. Ge capping layers were tried to attenuate the fluorescence but this did not work either and there was no way to measure the temperature of the InGaAs during the laser anneal. Instead the fluence was increased for a short 25 ns FWHM anneal until the advent of surface degradation. SIMS of the post anneal samples shown in Figure A-1 as well as micro 4pp measurements shown in Figure A-2 were then performed and the sheet resistance could be related to the increase in fluence.

Fluences above 293 mJ resulted in heavy surface degradation observed in STEM shown in Figure A-3. SIMS of post anneal samples indicated that anneals above 176 mJ could cause melting based on the box-like profiles of Si concentration and anneals below 117 mJ could not be measured by micro four-point probe since they were presumably unable to recover implant damage and activate. Based on the sheet resistance values, which were higher than conventional RTA anneal samples, the laser annealing experiment was abandoned for the time being since there was no known way to obtain carrier concentration data or accurate annealing temperature data although in hindsight the micro-Raman would have worked well in this case for active concentration measurements.

A subsequent investigation of laser annealing was performed in collaboration with students at Cornell who had developed a method to calibrate ms laser annealing to a given temperature and use Raman to measure active carrier concentration. A large number of implanted samples were sent to this group and using ms laser annealing the activation limits as measured by Raman were consistent with the maximum activation values for implanted species in this work indicating that Si activation by ms laser

annealing was likely subject to the same thermodynamic limit observed in more conventional anneals. . Laser annealing may result in less diffusion but it was clear from these experiments that activation was not improved. Systems that regularly benefit form laser annealing due to increased chemical solubility often result in increased activation but based on the work presented in previous chapters is seems unlikely that chemical solubility limits Si activation in InGaAs since there is temperature independent activation presented in this work.

A.3 Si Implants into InGaAs with MeV He^+ Implants for Vacancy Engineering

Early in the course of this work it was thought that the creation of more vacancies would help improve Si activation since it was unknown at the time what actually caused the limited Si activation whether it be amphoteric site occupation or the result of clustering or limited chemical solubility. MeV He ion implantation showed no net effect on increasing Si activation in InGaAs and in hindsight it is not so surprising to see why since the results of this work seem to give most support to large numbers of vacancies caused by Fermi level effects limiting the observed activation. MeV He implants might provide further evidence that clustering was not limiting activation since vacancy engineering often improves activation for dopants that are prone to clustering such as B in Si. These results also suggests that vacancy engineering will be unsuccessful in improving the maximum active n-type doping concentration in most III-V arsenides given that they are likely already limited in activation by vacancies and dopant-vacancy complexing and not clustering.

A.4 Nitrogen implants for Dilute Nitride Formation

50 keV, high dose nitrogen implants 1-2×10^{16} cm^{-2} into heavily Te doped InGaAs were performed to see if the addition of nitrogen could improve the activation of grown–

in dopants with a subsequent thermal anneal to recover damage from the nitrogen implant and move nitrogen onto lattice sites. Previous experiments have shown that nitrogen implants could be used to create dilute nitrides[305]. The active concentrations after implantation and annealing at 750°C for 30 s were much lower than the active concentrations in the as-grown state which suggested that the annealing was not able to form dilute nitrides and result in enhanced Te activation. Based on these initial electrical results it was decided to not pursue this project any further but the high nitrogen doses also likely formed bubbles further limiting the usefulness of such an implant. It seems likely that melting laser anneals would be necessary to cause N incorporations and the proper alloying of the material to form the dilute nitride.

A.5 Nitridation of InGaAs and InAs via Atomic Nitrogen Plasma

There is a large body of work on dilute nitride arsenides which have interesting properties and order of magnitude higher electron concentrations than III-V arsenides. One idea was that the surface of a pre-existing InGaAs could be nitrided to form a dilute nitride at the surface and increase the donor electron concentration at this surface[306]. The initial experiments attempted to form this nitride at 450°C with the nitrogen plasma in an ALD reactor. The presence of the native oxide however prevented the formation of any observable nitride so hydrogen plasma clean was added prior to the nitridation to attempt to clean the native oxide surface. Cleaning the native oxide surface with the hydrogen plasma had the effect of reducing the surface and leaving In and Ga metal balls on the surface and no nitride was observed in this case. It is unclear whether or not this would work if the recipe could be optimized such that the surface adequately cleaned without being reduced but the initial results suggested that solving this problem would be more trouble than it was worth.

A.6 Monolayer Doping of InGaAs with H_2S

Another early thought in the early stages of the work presented in this dissertation was that the surface of already Si implanted InGaAs could be made more active by monolayer doping with S. Previously activated Si implants into InGaAs were treated with H_2S for 1-5 minutes before being capped with an 80°C ALD Al_2O_3 layer. Once this process was complete, the samples were annealed at 750°C for 5 s. Subsequent van der Pauw Hall effect did not reveal any increased activation in the sheet number over that of Si implants alone. These experiments were performed well before the co-implant experiment detailed in this work. Given the results of the co-implant experiment in which it was found that S and Si implantation was not additive and that Si alone resulted in higher active concentrations that S alone once diffusion is accounted for the result of this experiment seems to be consistent with those of the co-implant experiment

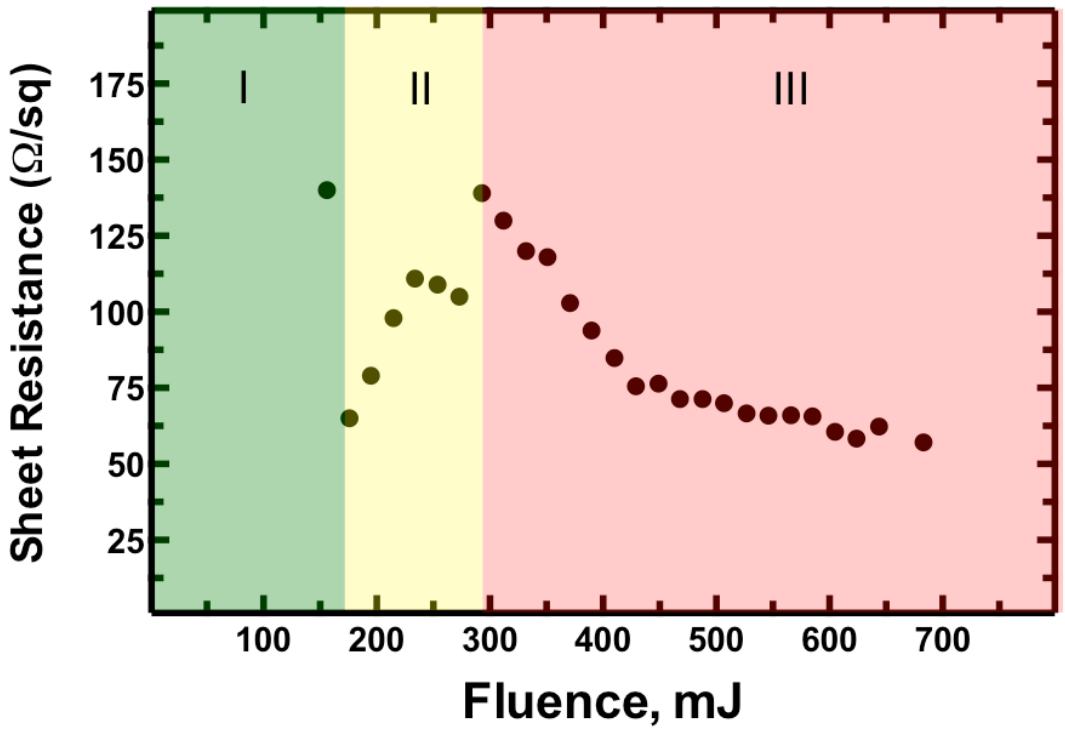

Figure A-1. Post laser anneal sheet resistance as a function of laser fluence. Laser anneal is from a 25 ns FWHM pulse on 80°C, 20 keV, 6×10^{14} cm^{-2} Si^{+} InGaAs. Region I indicates fluences that are Sub-melt, Regions II indicated melt and the onset of surface degradation and regions III indicated heavy surface degradation and lower sheet resistances from auto-doping of the InP substrate.

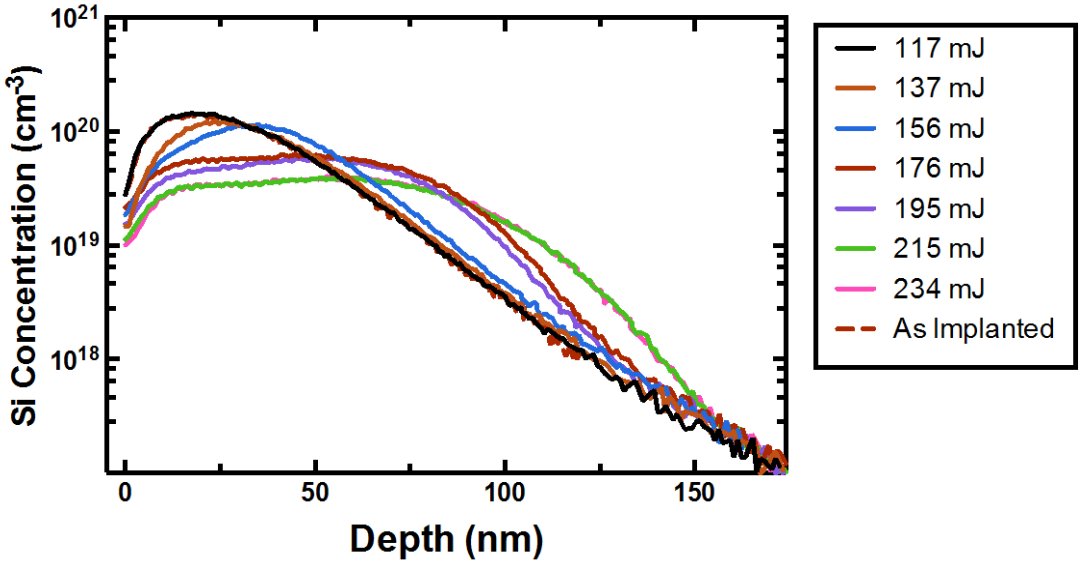

Figure A-2. SIMS of post laser anneal of 80°C, 20 keV, 6×10^{14} cm^{-2} Si^{+} implants into InGaAs. The box-shape profiles for fluences above 176 mJ indicate the onset of melting of the InGaAs.

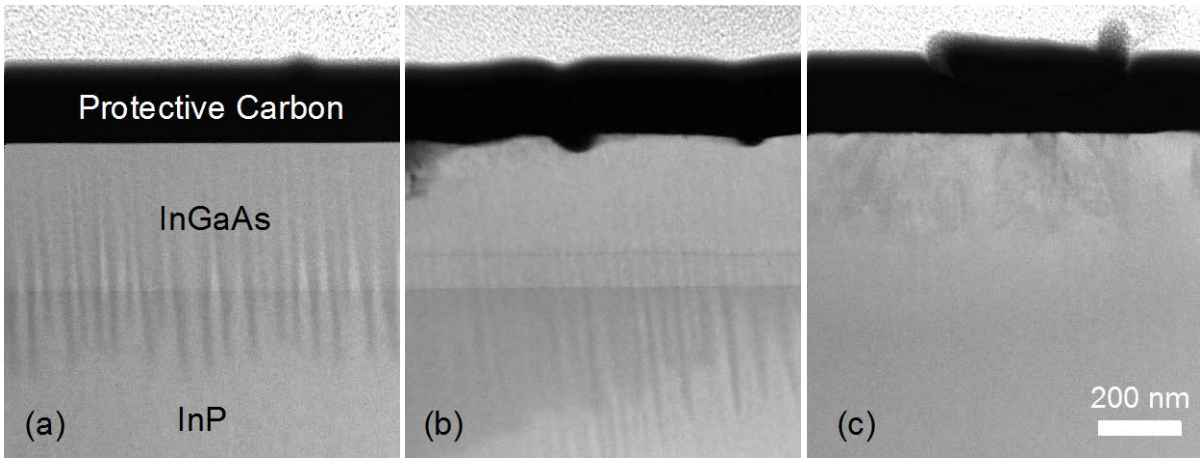

Figure A-3. Post laser anneal STEM of 80°C, 20 keV, 6×10^{14} cm^{-2} Si^{+} after a single laser pulse. Pulses were performed at fluences of (a) 176 mJ, (b) 293 mJ, and (c) 605 mJ.

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APPENDIX B
SUPPLEMENTARY INFORMATION ON EXPERIMENTS AND METHODS

B.1 Mathematica Program for Determining Active Carrier Concentration from Post Anneal SIMS and Hall Effect Measurements

```
(*The calculator assumes that the input file is a .CSV formatted for \
concentration in cm^-3and depth in in nm. It will output the total integrated \
dose (sanity check) as well as the total dose under the guessed solubility \
for "solubilityguess" which should match the measured hall value *)

solubilityguess = .3*10^19;
list = MovingAverage[Import["/Users/Aaron/Desktop/Test Folder/FILENAME.csv"],
   3];
length = Length[list] - 3;

xlist = ConstantArray["", length];
        Do[xlist[[i]] = list[[i, 1]]*1*10^-7, {i, 1, length}]
ylist = ConstantArray[0, length];
        Do[ylist[[i]] = list[[i, 2]], {i, 1, length}]

subtractedcurve = ylist - solubilityguess;
topcurve = ConstantArray["", length];
        Do[topcurve[[i]] = If[subtractedcurve[[i]] < 0, 0, subtractedcurve[[i]]], {i,
   1, length}]


wholecurve = Interpolation[Partition[Riffle[xlist, ylist], 2]];
partcurve = Interpolation[Partition[Riffle[xlist, topcurve], 2]];

CalculatedDose =
 NIntegrate[wholecurve[x], {x, xlist[[1]], xlist[[length]]}] -
  NIntegrate[partcurve[x], {x, xlist[[1]], xlist[[length]]}]
NIntegrate[wholecurve[x], {x, xlist[[1]], xlist[[length]]}]
smoothlist = MovingAverage[list, 3];
ListLogPlot[{list, smoothlist}]
```

B.2 Exposure Mode ALD Recipe

Step	Instruction	#	Value	Units
1	flow	0	20	sccm
2	flow	1	40	sccm
3	heater	16	150	C
4	heater	17	150	C
5	stabilize	16		
6	stabilize	17		
7	heater	12	245	C

8	heater	13	245	C
9	heater	14	245	C
10	heater	15	250	C
11	stabilize	12		
12	stabilize	13		
13	stabilize	14		
14	stabilize	15		
15	wait		600	sec
16	flow	0	20	sccm
17	flow	1	60	sccm
18	wait		5	sec
19	stopvalve		0	closed
20	wait		1	sec
21	pulse	Al	0.3	sec
22	wait		60	sec
23	stopvalve		1	open
24	flow	0	40	sccm
25	flow	1	140	sccm
26	wait		90	sec
27	flow	0	20	sccm
28	flow	1	60	sccm
29	wait		5	sec
30	stopvalve		0	closed
31	wait		1	sec
32	pulse	0	0.3	sec
33	wait		60	sec
34	stopvalve		1	open
35	flow	0	40	sccm
36	flow	1	140	sccm
37	wait		90	sec
38	flow	0	20	sccm
39	flow	1	60	sccm
40	wait		5	sec
41	goto	18	137	cycles
42	flow	0	20	sccm
43	flow	1	40	sccm
44	wait		30	sec
45	heater	12	195	C
46	heater	13	195	C
47	heater	14	195	C
48	heater	15	200	C
49	wait		5	sec
50	flow	0	0	sccm
51	flow	1	0	sccm
52	wait		10	sec

B.3 Supplementary Information on Sample Substrates

Two distinct $In_{0.53}Ga_{0.47}As$ substrates were used in this work. The majority of the experiments in this work used unintentionally doped, MOCVD grown $In_{0.53}Ga_{0.47}As$ on InP grown by IQE. The layer thickness of the InGaAs was limited chosen to be 300nm to allow deep enough thickness to study diffusion but also to limit the background sheet number from unintentional dopants for post-implant electrical activation results. The semi-insulating InP substrate further limited electrical measurements to the epitaxial InGaAs layer only. Hall effect of the as-received MOCVD InGaAs samples indicated that they were lightly n-type with a background doping density of 7.6×10^{16} cm^{-3}. Samples used in experiments studying the electrical deactivation of grown-in Si in InGaAs were grown by Cory Bomberger at the University of Delaware. The heavily doped InGaAs film was grown by solid source MBE at 490°C on a semi-insulating InP substrate. The InGaAs layer is 380 nm thick with the top 60 nm being heavily doped with Si resulting in a carrier concentration of 2.9×10^{19} cm^{-3}. The chemical concentration of Si measured via SIMS was approximately 7×10^{19} cm^{-3}, which is higher than the active carrier concentration in the case of the MBE substrate. Finally, the InAs samples used in this were commercially available 3” wafers grown by Wafertech using the liquid encapsulated Czochralski method (LEC). The wafers were Zn-doped which resulted in a background p-type carrier density of 3×10^{17} cm^{-3}.

Table B-1. Variable Temperature Implants into InGaAs

Sample	Substrate	Implant Species	Implant Energy (keV)	Implant Dose (cm^{-2})	Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
1	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	20	750	5
2	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	80	750	5
3	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	140	750	5
4	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	200	750	5
5	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	300	750	5
6	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	20	750	5
7	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	50	400:50:750	5
8	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	80	400:50:750	5
9	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	110	400:50:750	5
10	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	140	400:50:750	5
11	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	200	400:50:750	5
12	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	300	400:50:750	5

Table B-2. Variable Dose Implants into InGaAs

Sample	Substrate	Implant Species	Implant Energy (keV)	Implant Dose (cm^{-2})	Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
1	MOCVD InGaAs on SI InP	Si	12	3×10^{13}	80	750	5
2	MOCVD InGaAs on SI InP	Si	12	6×10^{13}	80	750	5
3	MOCVD InGaAs on SI InP	Si	12	1×10^{14}	80	750	5
4	MOCVD InGaAs on SI InP	Si	12	3×10^{14}	80	750	5
5	MOCVD InGaAs on SI InP	Si	12	6×10^{14}	80	750	5
6	MOCVD InGaAs on SI InP	Si	12	1×10^{15}	80	750	5
7	MOCVD InGaAs on SI InP	Si	20	3×10^{13}	80	750	5
8	MOCVD InGaAs on SI InP	Si	20	6×10^{13}	80	750	5
9	MOCVD InGaAs on SI InP	Si	20	1×10^{14}	80	750	5
10	MOCVD InGaAs on SI InP	Si	20	3×10^{14}	80	750	5
11	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	80	750	5
12	MOCVD InGaAs on SI InP	Si	20	1×10^{15}	80	750	5

Table B-3. Variable Energy Si Implants into InGaAs

Sample	Substrate	Implant Species	Implant Energy (keV)	Implant Dose (cm^{-2})	Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
1	MOCVD InGaAs on SI InP	Si	2	6×10^{14}	80	750	5
2	MOCVD InGaAs on SI InP	Si	4	6×10^{14}	80	750	5
3	MOCVD InGaAs on SI InP	Si	8	6×10^{14}	80	750	5
4	MOCVD InGaAs on SI InP	Si	12	6×10^{14}	80	750	5
5	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	80	750	5
6	MOCVD InGaAs on SI InP	Si	30	6×10^{14}	80	750	5
7	MOCVD InGaAs on SI InP	Si	2	6×10^{14}	20	750	5
8	MOCVD InGaAs on SI InP	Si	4	6×10^{14}	20	750	5
9	MOCVD InGaAs on SI InP	Si	8	6×10^{14}	20	750	5
10	MOCVD InGaAs on SI InP	Si	12	6×10^{14}	20	750	5
11	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	20	750	5
12	MOCVD InGaAs on SI InP	Si	30	6×10^{14}	20	750	5

Table B-4. Thermal Stability of Implanted Si Dopants

Sample	Substrate	Implant Species	Implant Energy (keV)	Implant Dose (cm^{-2})	Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
1	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	750	5
2	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	750	10
3	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	750	20
4	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	750	40
5	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	750	300
6	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	750	600
7	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	750	1200
8	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	700	900
9	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	700	1800
10	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	700	3600
11	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	650	3600
12	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	650	7200
13	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	650	14400
14	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	600	7200

Table B-4. Continued

Sample	Substrate	Implant Species	Implant Energy (keV)	Implant Dose (cm^{-2})	Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
15	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	600	14400
16	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	600	28800
17	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	550	14400
18	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	550	28800
19	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	550	57600

Table B-5. Co-Implants into InGaAs

Sample	Substrate	Co - Implant Species	Co-Implant Energy (keV)	Co-Implant Dose (cm^{-2})	Co-Implant Temperature (°C)	Dopant Species	Dopant Energy (°C)	Dopant Dose (cm^{-2})	Dopant Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
1	MOCVD InGaAs on SI InP	Al	20	3×10^{13}	100	Si	20	6×10^{14}	100	750	5
2	MOCVD InGaAs on SI InP	Al	20	6×10^{13}	100	Si	20	6×10^{14}	100	750	5
3	MOCVD InGaAs on SI InP	Al	20	1×10^{14}	100	Si	20	6×10^{14}	100	750	5
4	MOCVD InGaAs on SI InP	Al	20	3×10^{14}	100	Si	20	6×10^{14}	100	750	5
5	MOCVD InGaAs on SI InP	Al	20	6×10^{14}	100	Si	20	6×10^{14}	100	750	5
6	MOCVD InGaAs on SI InP	P	20	3×10^{13}	100	Si	20	6×10^{14}	100	750	5
7	MOCVD InGaAs on SI InP	P	20	6×10^{13}	100	Si	20	6×10^{14}	100	750	5
8	MOCVD InGaAs on SI InP	P	20	1×10^{14}	100	Si	20	6×10^{14}	100	750	5
9	MOCVD InGaAs on SI InP	P	20	3×10^{14}	100	Si	20	6×10^{14}	100	750	5

Table B-5. Continued

Sample	Substrate	Co - Implant Species	Co-Implant Energy (keV)	Co-Implant Dose (cm^{-2})	Co-Implant Temperature (°C)	Dopant Species	Dopant Energy (°C)	Dopant Dose (cm^{-2})	Dopant Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
10	MOCVD InGaAs on SI InP	P	20	6×10^{14}	100	Si	20	6×10^{14}	100	750	5
11	MOCVD InGaAs on SI InP	Ar	27	3×10^{13}	100	Si	20	6×10^{14}	100	750	5
12	MOCVD InGaAs on SI InP	Ar	27	$6.\times10^{13}$	100	Si	20	6×10^{14}	100	750	5
13	MOCVD InGaAs on SI InP	Ar	27	1×10^{14}	100	Si	20	6×10^{14}	100	750	5
14	MOCVD InGaAs on SI InP	Ar	27	3×10^{14}	100	Si	20	6×10^{14}	100	750	5
15	MOCVD InGaAs on SI InP	Ar	27	6×10^{14}	100	Si	20	6×10^{14}	100	750	5
16	MOCVD InGaAs on SI InP	S	20	3×10^{14}	100	Si	20	6×10^{14}	100	750	5
17	MOCVD InGaAs on SI InP	S	20	6×10^{14}	100	Si	20	6×10^{14}	100	750	5
18	MOCVD InGaAs on SI InP	S	20	1×10^{15}	100	Si	20	6×10^{14}	100	750	5
19	MOCVD InGaAs on SI InP	Control				Si	20	6×10^{14}	100	750	5

Table B-5. Continued

Sample	Substrate	Co - Implant Species	Co-Implant Energy (keV)	Co-Implant Dose (cm^{-2})	Co-Implant Temperature (°C)	Dopant Species	Dopant Energy (°C)	Dopant Dose (cm^{-2})	Dopant Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
20	MOCVD InGaAs on SI InP	Al	20	6×10^{13}	100	Si	20	6×10^{14}	100	750	600
21	MOCVD InGaAs on SI InP	Al	20	3×10^{14}	100	Si	20	6×10^{14}	100	750	600
22	MOCVD InGaAs on SI InP	Al	20	6×10^{14}	100	Si	20	6×10^{14}	100	750	600
23	MOCVD InGaAs on SI InP	P	20	6×10^{13}	100	Si	20	6×10^{14}	100	750	600
24	MOCVD InGaAs on SI InP	P	20	3×10^{14}	100	Si	20	6×10^{14}	100	750	600
25	MOCVD InGaAs on SI InP	P	20	6×10^{14}	100	Si	20	6×10^{14}	100	750	600
26	MOCVD InGaAs on SI InP	Ar	27	6×10^{13}	100	Si	20	6×10^{14}	100	750	600
27	MOCVD InGaAs on SI InP	Ar	27	3×10^{14}	100	Si	20	6×10^{14}	100	750	600
28	MOCVD InGaAs on SI InP	Ar	27	6×10^{14}	100	Si	20	6×10^{14}	100	750	600

Table B-5. Continued

Sample	Substrate	Co - Implant Species	Co-Implant Energy (keV)	Co-Implant Dose (cm^{-2})	Co-Implant Temperature (°C)	Dopant Species	Dopant Energy (°C)	Dopant Dose (cm^{-2})	Dopant Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
29	MOCVD InGaAs on SI InP	S	20	3×10^{14}	100	Si	20	6×10^{14}	100	750	600
30	MOCVD InGaAs on SI InP	S	20	6×10^{14}	100	Si	20	6×10^{14}	100	750	600
31	MOCVD InGaAs on SI InP	S	20	1×10^{15}	100	Si	20	6×10^{14}	100	750	600
32	MOCVD InGaAs on SI InP	Control				Si	20	6×10^{14}	100	750	600
33	MOCVD InGaAs on SI InP	S	20	6×10^{14}	100	Control				750	600
34	MOCVD InGaAs on SI InP	Al	20	6×10^{13}	100	S	20	6×10^{14}	100	750	600
35	MOCVD InGaAs on SI InP	Al	20	3×10^{14}	100	S	20	6×10^{14}	100	750	600
36	MOCVD InGaAs on SI InP	Al	20	6×10^{14}	100	S	20	6×10^{14}	100	750	600
37	MOCVD InGaAs on SI InP	P	20	6×10^{13}	100	S	20	6×10^{14}	100	750	600

Table B-5. Continued

Sample	Substrate	Co - Implant Species	Co-Implant Energy (keV)	Co-Implant Dose (cm^{-2})	Co-Implant Temperature (°C)	Dopant Species	Dopant Energy (°C)	Dopant Dose (cm^{-2})	Dopant Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
38	MOCVD InGaAs on SI InP	P	20	3×10^{14}	100	S	20	6×10^{14}	100	750	600
39	MOCVD InGaAs on SI InP	P	20	6×10^{14}	100	S	20	6×10^{14}	100	750	600

Table B-6. Si Implants into InAs

Sample	Substrate	Implant Species	Implant Energy (keV)	Implant Dose (cm^{-2})	Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
1	Zn-doped LEC InAs	Si	20	1×10^{13}	100	700	30
2	Zn-doped LEC InAs	Si	20	5×10^{13}	100	700	30
3	Zn-doped LEC InAs	Si	20	1×10^{14}	100	700	30
4	Zn-doped LEC InAs	Si	20	5×10^{14}	100	700	30
5	Zn-doped LEC InAs	Si	20	1×10^{15}	100	700	30
6	Zn-doped LEC InAs	Si	20	1×10^{15}	100	600	30
7	Zn-doped LEC InAs	Si	20	1×10^{15}	100	500	30
8	Zn-doped LEC InAs	Si	20	1×10^{15}	100	400	30
9	Zn-doped LEC InAs	Si	20	1×10^{15}	100	700	1
10	Zn-doped LEC InAs	Si	20	1×10^{15}	100	700	5
11	Zn-doped LEC InAs	Si	20	1×10^{15}	100	700	90
12	Zn-doped LEC InAs	Control					

Table B-7. Activation and Deactivation Study of MBE and Implanted Si

Sample	Substrate	Implant Species	Implant Energy (keV)	Implant Dose (cm^{-2})	Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
1	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	550	600
2	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	600	600
3	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	650	600
4	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	700	600
5	MOCVD InGaAs on SI InP	Si	10	5×10^{14}	80	750	600
6	380 nm MBE n-InGaAs on SI InP					550	600
7	380 nm MBE n-InGaAs on SI InP					600	600
8	380 nm MBE n-InGaAs on SI InP					650	600
9	380 nm MBE n-InGaAs on SI InP					700	600
10	380 nm MBE n-InGaAs on SI InP					750	600

Table B-8. Pre-amorphized vs Crystalline

Sample	Co Implant Species	Co-Implant Energy (keV)	Co-Implant Dose (cm^{-2})	Co-Implant Temperature (°C)	Dopant Species	Dopant Energy (keV)	Dopant Dose (cm^{-2})	Dopant Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
1	As	220	3×10^{14}	20	Si	20	6×10^{14}	20	450	5
2	As	220	3×10^{14}	20	Si	20	6×10^{14}	20	500	5
3	As	220	3×10^{14}	20	Si	20	6×10^{14}	20	550	5
4	As	220	3×10^{14}	20	Si	20	6×10^{14}	20	600	5
5	As	220	3×10^{14}	20	Si	20	6×10^{14}	20	650	5
6	As	220	3×10^{14}	20	Si	20	6×10^{14}	20	700	5
7	As	220	3×10^{14}	20	Si	20	6×10^{14}	20	750	5
8					Si	20	6×10^{14}	250	450	5
9					Si	20	6×10^{14}	250	500	5
10					Si	20	6×10^{14}	250	550	5
11					Si	20	6×10^{14}	250	600	5
12					Si	20	6×10^{14}	250	650	5
13					Si	20	6×10^{14}	250	700	5
14					Si	20	6×10^{14}	250	750	5

All substrates are 300nm of MOCVD InGaAs on SI InP

Table B-9. Fermi Level Effects

Sample	Substrate	Implant Species	Implant Energy (keV)	Implant Dose (cm^{-2})	Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
1	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	80	550	5
2	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	80	650	5
3	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	80	750	5
4	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	80	650	10
5	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	80	650	40
6	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	80	650	160
7	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	80	650	320
8	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	80	650	480
9	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	80	650	600
10	MOCVD InGaAs on SI InP	Si	20	6×10^{14}	80	650	900
11	MOCVD InGaAs on SI InP	P	20	6×10^{14}	80	550	5
12	MOCVD InGaAs on SI InP	P	20	6×10^{14}	80	650	5
13	MOCVD InGaAs on SI InP	P	20	6×10^{14}	80	750	5
14	MOCVD InGaAs on SI InP	P	20	6×10^{14}	80	650	10

Table B-9. Continued

Sample	Substrate	Implant Species	Implant Energy (keV)	Implant Dose (cm^{-2})	Implant Temperature (°C)	Anneal Temperature (°C)	Anneal Time (s)
15	MOCVD InGaAs on SI InP	P	20	6×10^{14}	80	650	40
16	MOCVD InGaAs on SI InP	P	20	6×10^{14}	80	650	160
17	MOCVD InGaAs on SI InP	P	20	6×10^{14}	80	650	320
18	MOCVD InGaAs on SI InP	P	20	6×10^{14}	80	650	480
19	MOCVD InGaAs on SI InP	P	20	6×10^{14}	80	650	600
20	MOCVD InGaAs on SI InP	P	20	6×10^{14}	80	650	900
21	MOCVD InGaAs on SI InP	P	20	6×10^{14}	80	650	400
22	380 nm MBE n-InGaAs on SI InP	P	20	6×10^{14}	80	650	400

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BIOGRAPHICAL SKETCH

Aaron Lind was born to his two loving parents, Gregg and Suzanne. Throughout his childhood both Gregg and Suzanne indulged his curiosities whether they be athletic, artistic, or academic but they also made sure that he learned and understood the value of hard work and self-discipline. Aaron received his B.S. in materials engineering from Iowa State University in 2011 and his M.S in Materials Science and Engineering from The University of Florida in 2012 prior to obtaining his Ph.D in Materials Science and Engineering at the University of Florida in 2015. Aaron is something, but he is not everything. Perhaps he is something more like a falling leaf. Or, maybe, a snowflake. Born of dust and water, destined to return to dust and water, and, hopefully, beautiful as he passes.