DOPANT-DEFECT INTERACTIONS IN EPITAXIALLY GROWN HIGHLY DOPED SI:P

By

## ZACHARY NATHAN WEINRICH

## A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

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To the noble pursuit of attempting to better understand the world in which we live

#### ACKNOWLEDGMENTS

Science is not done in a vacuum. While my name may be on the cover, this is not a truly accurate representation of the cumulative effort put into the creation of this document. Without the support and inspiration of mentors, colleagues, friends and family I would not be who I am today, and this work would not have been possible. For these people I am thankful.

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## LIST OF ABBREVIATIONS

APT	Atom probe tomography
BJT	Bipolar junction transistor
BOE	Buffered oxide etch
CDE	Cyclic deposition etch process
CMOS	Complementary metal-oxide-semiconductor technology. Use of nMOS and pMOS components together in the same circuit
CVD	Chemical vapor deposition
CVE	Chemical vapor etch
DCS	dichlorosilane
DFT	Density functional theory
DIBL	Drain induced barrier lowering
DOS	Density of states
DP	Diffraction pattern
DSA	Dynamic surface anneal
EELS	Electron energy loss spectroscopy
ELNES	Analysis of the near edge structure within electron energy loss spectroscopy
ESR	Electron spin resonance
EXAFS	Extended x-ray absorption spectroscopy with a focus on the fine structure elements of the spectra
EXELFS	Extended electron energy loss spectroscopy with a focus on the fine structure elements of the spectra
GAAFET	Gate-all-around field effect transistor
FET	Field effect transistor
FIB	Focused ion beam lithography tool

finFET	Multi-gate field effect transistor constructed out of a 3-dimensional fin structure
FLOOPS	Florida object oriented process simulator
GGA	Generalized gradient approximation used within DFT simulations
HAADF-STEM	High angle annular dark field scanning transmission electron microscopy
HDSiP	Highly doped Si:P
HS:SiP	Highly strained Si:P. Another term occasionally used in the literature in place of HDSiP
HEMT	High electron mobility transistor
HF	Hydrofluoric acid
HR-TEM	High resolution transmission electron microscopy
HR-XRD	High resolution transmission electron microscopy
ITRS	International technology roadmap for semiconductors
JFET	Junction field effect transistor
LDA	Local density approximation used within DFT simulations
LDD	Lightly doped drain region of a MOSFET
LDSiP	"Low-doped Si:P" sub $1 \times 10^{21}$ cm <sup>-3</sup> P epitaxially grown layers which exhibit slightly different properties compared to HDSiP but grown using the same selective epitaxy method.
LEAP	Local electron atom probe tomography
MBE	Molecular beam epitaxy
MOSFET	Metal oxide semiconductor field effect transistor
nMOS	n-type metal-oxide-semiconductor technology. Refers to n-channel transistors
NMR	Nuclear magnetic resonance spectroscopy
PAS	Positron annihilation spectroscopy
PIC	Phosphorus interstitial cluster

PID	Proportional integral derivative controller
pMOS	p-type metal-oxide-semiconductor technology. Refers to p-channel transistors
PTEM	Plan view transmission electron microscopy
RP-CVD	Reduced pressure chemical vapor deposition
RSD	Raised source-drain transistor design
RTA	Rapid thermal annealing
RTO	Rapid thermal oxidation
S/D	Source and drain regions of a transistor
SCE	Short channel effects
SEG	Selective epitaxial growth
SEM	Scanning electron microscopy
SIMS	Secondary ion mass spectrometry
SOI	Silicon on insulator
SS	Subthreshold swing
SSNMR	Solid state nuclear magnetic resonance spectroscopy
SRB	Strain relaxed buffer
STEM	Scanning transmission electron microscopy
UHV	Ultra-high vacuum
UHV-CVD	Ultra-high vacuum chemical vapor deposition
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
XTEM	Cross-sectional transmission electron microscopy

## Abstract of Dissertation Presented to the Graduate School of the University of Florida in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy

## DOPANT-DEFECT INTERACTIONS IN EPITAXIALLY GROWN HIGHLY DOPED SI:P

By

Zachary Nathan Weinrich

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Highly-doped Si:P (HDSiP) epitaxially grown thin films with phosphorus concentrations above 10<sup>21</sup> cm<sup>-3</sup> are being investigated for transistor applications. With the ability to realize record-setting low contact resistance junctions, HDSiP fulfills the ITRS target for the 7 nm transistor node. Ultra-low contact resistance combined with finFET compatibility and the generation of tensile strain in the channel region makes HDSiP ideal as an nMOS source and drain material. Efficient dopant activation of HDSiP has been reported with a millisecond laser dynamic surface anneal (DSA). As a result of the DSA, activation levels well beyond the previously established electrical solubility limit for phosphorus in silicon can be obtained with negligible diffusion and minimal loss of strain. However, the mechanism behind this activation and the stability of the resulting metastable state is not well understood. This work seeks to understand the fundamental processes behind activation, clustering, strain, and stability of HDSiP after exposure to various thermal treatments. Deactivation kinetics, point defect release, strain evolution and defect formation were among phenomena studied to obtain fundamental knowledge of HDSiP prior to incorporation into transistor process flow.

## CHAPTER 1 INTRODUCTION

#### **1.1 Motivation**

Looking back through history, society has characterized distinct periods of time throughout human evolution based on the enabling material of that respective period. The stone age came about as the time period when human beings first started purposefully modifying their surroundings in order to better complete daily tasks. The bronze age arrived as copper was able to be reduced from malachite and thus enabled a whole new set of tools which vastly enhanced the effectiveness of tasks in many areas of daily life from farming and hunting to conducting war. Most recently, we are said to exist in a time today called the information age, which can be easily attributed to the materials advances made with silicon semiconductors that have become so prolific and necessary to every day modern life. Just as continual development with iron lead to more enabling properties of the material, the same should be done for silicon in order for humanity to progress. This progress is not only for the purposes of benefitting society and satiating people's needs for new gadgets but also to hopefully lessen the negative impacts our species has inflicted on the environment of the planet where we all reside. More power conscientious electronic devices as well as smart electronics which can monitor and reduce power usage will be of paramount importance to reducing energy consumption over the next 50 years. Previously, the biggest driver of the microelectronics industry had always been for increased processing speed and performance. Now that mobile computing and cellular technology dominate the microelectronics marketplace, consumer demands for increased device battery life are co-aligning with the more noble goal of decreasing power consumption for reduced environmental impact.

Metal oxide semiconductor field effect transistors (MOSFETs) have been central to the microelectronics industry due to their computational abilities. Over the past 70 years, MOSFET research has been focused on making the devices smaller such that more may fit on a single chip for economic reasons as well as for performance gains. In the modern era, the focus has shifted to also include reduced power consumption as a market driving force.[1] As MOSFETs continue to shrink in node size, diminishing returns are seen in power consumption. This is in part due to how as the channel becomes smaller, its resistance becomes a minor contributor to power consumption in comparison to the various other resistances within the device in its "on" state. Of these other resistances, contact resistance between the transistor and the metal interconnects dominates. To minimize the impact of contact resistance, high transistor source and drain doping levels are required. A novel material made through a selective epitaxial growth process has been developed to suite this demand for nMOS transistors.

Highly phosphorus doped silicon (HDSiP) is a semiconductor alloy doped well above the solid solubility limit (>1x10<sup>21</sup> cm<sup>-3</sup>) for phosphorus in silicon.[2]–[5] Due to the extremely high doping level, HDSiP has been demonstrated to form record setting low contact resistance junctions and show promise for use in future MOSFET technology nodes.[6], [7] However, as HDSiP is a relatively novel material, the structure-property relationships as well as the integrability into modern transistor process flow are not well known. The purpose of this work is to characterize HDSiP from a fundamental materials science standpoint and understand how it will fit into a transistor process. By doing this, future transistors technology nodes will be enabled, and enhanced electronic device performance can be realized.

### **1.2 Transistor Technology**

The advent of the transistor was arguably the most impactful development to science and technology of the 20<sup>th</sup> century. Since its introduction in 1947, the transistor has formed the

backbone of modern computational logic processing. As a circuit element, the transistor can act both as a switch in digital logic computations or as a signal amplifier when used in an analog circuit. There are many types of transistors such as the original point contact transistor, the bipolar junction transistor (BJT), the junction field effect transistor (JFET), the high electron mobility transistor (HEMT), and the metal oxide semiconductor field effect transistor (MOSFET).[8], [9] Each type of transistor has its associated advantages and disadvantages, however, MOSFETs and so-called complementary metal oxide semiconductor (CMOS) technology have formed the backbone of digital logic operations due to their high switching speeds and efficiency. As digital logic and CMOS technology typically drives the semiconductor market with the most advanced cutting-edge technology, improving on aspects of CMOS transistors will be the focus of the work described herein.

The International Technology Roadmap for Semiconductors (ITRS) has determined that the industry driving force for MOSFET performance improvements has switched from maximum speed of operation to low power consumption.[1] As mobile devices constitute a large percentage of the market in current times, the need for integrated circuit elements which can extend battery life has likewise increased. Historically, performance improvements of MOSFETs have occurred through the down-scaling of their physical dimensions.[10], [11] As the physical dimensions of a modern MOSFET are approaching the atomic scale, additional methods are required to continue this trend.

The following sections will give a background on MOSFET technology and then focus on three specific approaches to allow for continued transistor scaling while increasing performance and decreasing power consumption. The first approach to enable this scaling involves the switching to increasingly complex 3-dimensional transistor structures. These

structures allow for a higher degree of control over the switching behavior of the transistor. Secondly, as devices become smaller, the resistance of each specific component increases. To combat these resistance increases, lower resistance materials need to be integrated into the manufacturing process for MOSFETs. The final approach to improving MOSFET properties makes use of strain engineering. It has been determined that introducing tensile or compressive strain in certain areas of the transistor can have dramatic effects on performance. As modern transistors are complex entities, a multi-faceted approach to improving their design is necessary.

#### **1.2.1 Basic Transistor Operation**

Depicted in Figure 1-1 as an electrical circuit diagram element, the MOSFET is a threeterminal device. The terminals are labeled "source" for electron source, "drain" for electron drain



Figure 1-1. Circuit Diagram depiction of a transistor with the three terminals labeled. and the "gate" for the terminal that controls flow of electrons between the source and drain. Originally, the drain terminal was to be called a "sink" but to avoid confusion with the shorthand lettering used in diagrams, "drain" was adopted. This device is typically wired into a circuit in what is known as a common source mode where the input voltage,  $V_{GS}$ , and the output voltage  $V_{DS}$ , are both measured relative to the source which is common between the two. (Figure 1-2) The current that flows from the drain to the source  $I_{DS}$  then becomes the important characteristic of the device and determines whether the MOSFET is on or off. From this common source configuration, two different types of electrical behavior can be obtained. These behaviors are called the output characteristics and the transfer characteristics.



Figure 1-2. MOSFET connected in common source mode

For a constant applied  $V_{GS}$ , the MOSFET either operates as a resistor or as a non-ideal current source depending on the source-drain voltage  $V_{DS}$ . The switchover of device characteristics occurs at a particular voltage  $V_{Dsat}$  which is determined by the device construction. Below  $V_{Dsat}$  the MOSFET operates like a resistor and above  $V_{Dsat}$  the current saturates and the device operates like a non-ideal current source. Increasing the constant applied  $V_{GS}$  from 0 V to  $V_{DD}$ , the circuit power supply voltage, has the effect of increasing I<sub>DS</sub> within



Figure 1-3. Typical output characteristics of a MOSFET connected in common source mode. Increasing the applied gate voltage (V<sub>GS</sub>) increases drain-source current (I<sub>DS</sub>).

both regimes. When  $V_{GS}$  and  $V_{DS}$  are at their maximum values ( $V_{GS} = V_{DS} = V_{DD}$ ), the on-state current  $I_{On}$  can be determined. Two important MOSFET metrics can be obtained by the slopes of the linear and the saturation regimes of the output plot provided that the  $V_{GS}$  is above the

threshold voltage  $V_T$  to turn the device on. The drain-source resistance  $R_{DS}$  is defined as the slope of the output plot within the linear regime and can be described by equation 1-1. The

$$R_{DS}(V_{DS} < V_{Dsat}) = \left(\frac{dI_{DS}}{dV_{DS}}\Big|_{V_{GS} > V_T}\right)^{-1}$$
(1-1)

output resistance  $r_0$  is defined by the slope of the output plot when the device is operating in saturation mode and is given by equation 1-2.

$$r_0(V_{DS} > V_{Dsat}) = \left(\frac{dI_{DS}}{dV_{DS}}\Big|_{V_{GS} > V_T}\right)^{-1}$$
(1-2)

The other important characteristic of a MOSFET is the transfer characteristics. Transfer characteristics are where  $V_{DS}$  is kept constant and  $I_{DS}$  is monitored with respect to changing  $V_{GS}$ . With sufficiently low  $V_{GS}$ , the device is considered to be in the off state and only a small amount of current can pass from the source to the drain. This current,  $I_{off}$  is deemed



Figure 1-4. Linear scale (left) and log scale (right) y-axis transfer characteristics of a typical MOSFET with a constant drain-source voltage applied (V<sub>DS</sub>)

the leakage current and seems to be a negligible value on a linear scale transfer plot (Figure 1-4 left). However, with billions of devices on a single chip that all possess this leakage current, this

value is no longer negligible. Above a characteristic  $V_{GS}$ , a dramatic increase in  $I_{DS}$  can be observed. This voltage is called the threshold voltage,  $V_T$ , and for  $V_{GS} > V_T$ , the device is considered on. In Figure 1-4 on the right,  $I_{DS}$  is plotted on a logarithmic scale so the sub threshold behavior of the device can be visualized. From this, the major figures of merit with regards to device performance are related to the slope of the transfer curve. The device transconductance  $g_m$  is the derivative of this plot and is one such metric. Below the threshold voltage, the

$$g_m = \frac{dI_{DS}}{dV_{GS}}\Big|_{V_{DS}}$$
(1-3)

transconductance is related to another commonly reported value called the subthreshold swing (SS). The subthreshold swing is determined by the voltage increase (in mV) needed to increase  $I_{DS}$  by a factor of 10. A low value of SS is indicative that the gate has a high degree of control over turning the device on or off.

A more detailed view of a MOSFET from a materials perspective can be seen in Figure 1-5 where two different types of MOSFET are shown. An n-channel MOSFET (nMOSFET) is composed of a highly n-doped source and drain region on a p-type substrate while a p-channel MOSFET (pMOSFET) has the same structure but the n and p regions have been switched. Just within the surface of the silicon below the gate stack, the energy band diagram can be drawn for the nMOSFET as follows in Figure 1-6. nMOSFET technology will be the focus of this work and thus from this point forward will be referred to without complementing pMOSFET discussion. The band diagram in Figure 1-6 exists when there is no applied voltage at either the gate or drain electrodes, and thus the source and drain have equal potential. It can be seen that there is a large energy barrier in the conduction band ( $E_{CB}$ ) for electrons at the Fermi level ( $E_F$ ) to move between the source and drain. With no voltage applied, built in potentials prevent

charges from flowing. Once a positive voltage is placed on the drain contact, the right side of the energy band diagram



Figure 1-5. Cross sectional image of an nMOSFET (top) and a pMOSFET (bottom) outlining terminals as well as important doped regions. Dimensions have been exaggerated for ease of comprehension.



Figure 1-6. Band diagram of an nMOSFET device showing large energy barrier for electrons to travel across channel region with no applied voltages.

shifts downwards as seen in Figure 1-7. This applied voltage serves to shorten the energy barrier for electrons moving from the source to the drain. Once sufficiently high voltage is applied, the potential barrier height also begins to decrease. This effect is magnified for short channel length MOSFETs and is given the name drain-induced barrier lowering (DIBL). Even with drain voltages which are insufficient to cause significant DIBL, a small I<sub>DS</sub> can be measured when V<sub>GS</sub> is equal to zero. This is due to the distribution of energies which electrons in the source possess. A very small fraction of these electrons will have sufficient thermal energy to pass the barrier giving rise to leakage current between the source and drain.



Figure 1-7. Band diagram showing only the conduction band for an nMOSFET device with larger V<sub>DS</sub> applied. Barrier for current flow reduces with higher V<sub>DS</sub> (DIBL).

When a voltage is applied to the gate, the conduction band energy of the channel region becomes depressed as seen in Figure 1-8. Once  $V_{GS} > V_T$ , the device is operating in saturation and the energy barrier is approximately equal to the thermal energy of electrons in the source,  $k_bT$ . This allows for the free flow of electrons from source to drain. Now that the fundamentals behind nMOSFET operation have been covered, the following sections will discuss methods to improve their function.



Figure 1-8. Band diagram showing only the conduction band for an nMOSFET device with an applied voltage at the drain showing the effects of larger applied VGS. Device turnon occurs when the channel barrier height is sufficiently reduced.

## **1.2.2 Transistor Scaling**

Transistor scaling has been the driving force for technological advances within the semiconductor field since its induction. In the early days of the industry, a simple scaling factor could be used to shrink each of the dimensions of a transistor by the same amount.[10]–[12] This method worked extremely well and dramatic increases to the number of transistors that could be fabricated onto a single chip were observed. The driving forces for scaling were numerous: smaller transistors could be operated at a higher frequency due to currents not having to travel as long of a distance, transistors could be more densely packed onto a chip and finally, the cost of each transistor produced diminished dramatically. As scaling trends continued, physical limitations of the technology were encountered diminishing the benefits to continued scaling. These effects are called short channel effects (SCEs) as they only manifest in sufficiently short channel length transistors.[11], [13]–[15] Modern transistor designs incorporate additional adjustments to address these SCEs and continue to realize performance gains. Generally, it is accepted by the semiconductor industry that despite these physical limitations of modern

transistor designs, performance will continue to improve and cost will continue to decrease up to the 2 nm node predicted by the ITRS for 2030.[1]

## **1.2.3 Device Architecture**

To combat short channel effects seen with shrinking MOSFET dimensions, perhaps one of the most profound changes to transistor design has been the switch to 3-dimensional device architecture. By switching to more complex double-gate, tri-gate (finFET) and gate-all-around (GAAFET) structures, increased performance can be realized. By switching to these more complex structures, greater electrostatic control over



Figure 1-9. Cross-sectional depiction of complex geometry MOSFETs. Grey areas are silicon, blue areas represent dielectric and red areas are conductive gate material. Devices are shown with the channel direction perpendicular to the page.

the channel region can be obtained, parasitic capacitances can be reduced and electric field lines that penetrate from the source to the drain far from the gate can be mitigated.[16]–[19] These features lead to improved electrical characteristics of decreased DIBL and SS. These beneficial properties lead to the adoption of finFET structures for the 22 nm transistor node.[20] For the manufacturing of finFET transistors and higher complexity architectures, certain processing methods cannot be used. For example, melt thermal processing will need to be avoided to maintain integrity of the structure. For this reason, non-melt thermal processing will be discussed exclusively in this work.

## **1.2.4 Sources of Parasitic Power Consumption**

As was mentioned in the beginning of section 1.2 of this report, lowering power consumption has become the primary target for transistor improvement dictated by the ITRS.[1]

Principally, this is to be done by reducing power supply voltage and designing transistors with lower sub threshold swing. In order to understand how materials advances can facilitate lower power consumption of logic integrated circuits, knowledge of power dissipation mechanisms within a transistor are required. As this work involves the source and drain regions of nMOSFETs, elements related to how these regions can be improved with novel materials will be the focus of this section.

Power dissipation for transistors can be broken down into two components: dynamic power consumption and static power consumption. Dynamic power consumption for a CMOS inverter circuit can be related to the power supply voltage,  $V_{DD}$ , the frequency of operation, *f* and the effective capacitances of the input circuit, C<sub>in</sub>, and output circuit, C<sub>out</sub>). As of 2009, this type of power consumption described in equation 1-4 typically accounts for ~90% of the power

$$P_{ac} = (C_{in} + C_{out})V_{DD}^2 f \tag{1-4}$$

consumption of a MOSFET circuit.[12] It can be seen that lowering the power supply voltage as the ITRS dictates for future devices will have a substantial impact on CMOS active power consumption.[1] In order to do this, however, without having a negative impact on individual transistor drive current, lower resistance materials will be required.

Static power is the other main type of power consumption for a transistor. Static power consumption is becoming a much larger concern for device designers now that there are billions of transistors on a chip. Related to leakage currents, static power consumption  $P_{\text{standby}}$  can be broken down into a few main parts: leakage from the source to the drain ( $I_{\text{Off}}$ ), gate oxide leakage ( $I_{\text{G}}$ ) and reverse bias p-n junction leakage to the bulk ( $I_{\text{DB}}$ ).[21]–[24]  $I_{\text{DB}}$  can be essentially

$$P_{standby} = V_{DD}(I_{Off} + I_{DB} + I_G)$$
(1-5)

neglected for finFET devices and other structures with fully depleted channel regions as the value for this leakage current is several orders of magnitude lower than that of  $I_{Off}$  and  $I_G$ . Gate oxide leakage is mainly controlled through the thickness of the gate oxide and the dielectric constant of that material.[22] For source-drain leakage, standby power can be related to the resistance of the materials used through Ohm's law. In this situation,  $R_{series}$  is defined as the resistance between the source and drain with  $V_{GS} = 0$ . It can be seen from equation 1-7 that a

$$I_{off} = \frac{V_{DD}}{R_{series}} \tag{1-6}$$

$$P_{standby} = \frac{V_{DD}^2}{R_{series}|_{V_{GS}=0}}$$
(1-7)

high  $R_{series}$  would benefit static power consumption.  $R_{series}$  is composed of multiple components that factor into the series resistance of the device and can be broken down into two main parts.

$$R_{series} = R_{external} + R_{channel}(V_{GS})$$
(1-8)

Ultimately, what is desirable is to have a high  $R_{channel}$  when  $V_G < V_T$  creating a high  $R_{series}$ and then a low external resistance ( $R_{external}$ ) for when  $V_G > V_T$  such that high drive current can be obtained.  $R_{external}$  is composed of several different factors that lead up to the channel region from the metal contacts. In the on-state, MOSFET channel resistance tends to be a small component of  $R_{series}$  due to short channel lengths and the high degree of electrostatic control that the gate possesses for finFET transistors, thus the main avenue for decreasing total device series resistance will come from advances in source/drain materials.

With some exceptions, a typical MOSFET is made to be symmetrical with respect to the source and drain. Therefore, in a typical device  $R_{external}$  can be described as twice the resistance

$$\frac{R_{external}}{2} = R_{Source} = R_{Drain} \tag{1-9}$$

associated with the source,  $R_{Source}$ , or twice the resistance associated with the drain,  $R_{Drain}$ (equation 1-9).[12] These terms become even more important when transistor dimensions decrease as series resistance components of the source and drain increase more than proportionally.[25] Given that the a primary directive of the ITRS is to lower power supply voltages, in order to maintain high drive currents,  $R_{external}$  must be minimized.[1] To do this, the focus of design engineers and materials scientists needs to be on minimizing the resistance of each element that composes  $R_{external}$  as shown in equation 1-10. The four major sources of resistance are accumulation resistance ( $R_{ac}$ ), spreading resistance ( $R_{sp}$ ), resistance of the source/drain bulk ( $R_{sd}$ ) and contact resistance with the adjacent silicide ( $R_{co}$ ).[25] These

$$R_{ext} = R_{ac} + R_{sp} + R_{sh} + R_{co}$$
(1-10)

resistances have been depicted in Figure 1-10. As the metal interconnects possess a resistance





several orders of magnitude lower than these values, metal/silicide contact resistance and bulk

resistance of the metal and silicide are typically neglected. All four of these sources of series

resistance will be discussed in the following sections as well as approaches to diminish their effects.

### **1.2.4.1** Accumulation resistance

An ideal source/drain extension region would have a perfectly sharp dopant concentration profile cutoff between the n+ heavily doped extension and the p-doped channel region. As this type of profile is not possible in practice, a non-ideal dopant profile gradient is produced where some n-type doping extends under the gate of the device. This overlapping region is under the control of the gate voltage as the resistivity of this region is less than that of the bulk of the source/drain extension region and charge carriers will accumulate here with the presence of a gate voltage (Figure 1-11). As a result, conduction takes place only at the surface in this overlap region until the extension bulk resistivity becomes lower than that of the accumulation layer.[12], [25] Accumulation layer resistivity can be estimated by the following equation 1-11 where  $\mu_{ac}$  is

$$\begin{array}{c} Fur = \mu_{ac}C_{ox}V_{GS} \\ \hline \\ Gate \\ Oxide \\ n+Si \\ n Si \\ n Si \\ p Si \\ \end{array}$$

$$\rho_{ac} = \frac{1}{\mu_{ac} C_{Ox} V_{GS}} \tag{1-11}$$

Figure 1-11. Accumulation region within the metallurgical junction of the source or drain area is shown as the dark green region just under the gate oxide in the overlap region. At lateral distances until dopant concentration gradient is sufficiently high, the majority of conduction through this region will take place in the very surface layer.

defined as the average carrier mobility within the accumulation layer.[12] The accumulation layer resistivity can be minimized by creating a sharper dopant profile cutoff for the extension regions.

## **1.2.4.2 Spreading resistance**

Spreading resistance in a MOSFET device can be attributed to the small dimensions of the area of the source and drain extension regions that gets contacted by the channel and accumulation region when the transistor is in the on state. As current flows through a material of uniform resistivity from a region of small cross-sectional area to a region of large cross-sectional area additional resistance is experienced by the circuit. This resistance can be modeled by the following equation 1-12 where xj and xc can be determined from Figure 1-12. Spreading resistance can be decreased by creating deeper source-drain extension regions

$$R_{sp} = \frac{2\rho}{\pi W} \ln\left(\frac{3x_j}{4x_c}\right) \tag{1-12}$$

Or by increasing the depth of the inversion region of the MOSFET in the on-state.[12], [25] As neither of these solutions to decrease the effects of spreading resistance ultimately benefit device properties due to various trade-offs, spreading resistance is tolerated during device design.



Figure 1-12. Depiction of spreading resistance to accompany equation 1-12.

#### **1.2.4.3 Source drain bulk resistance**

The sheet resistance of the bulk source and drain regions contributes a significant fraction of the total device resistance. For MOSFETs with longer channel regions, it used to be assumed that current through the source and drain was shunted at the silicide contact and thus the only contributions to sheet resistance were by the region of the source and drain (length S, thickness

$$R_{sh} = \rho_{sd} \frac{S}{W} \tag{1-13}$$

x<sub>j</sub>) under the spacer leading up to the silicide region.[12] For short channel devices, and particularly in finFET structures, this is not the case, and the lateral dimensions including the junction depth of these regions becomes significant. Diminishing the contribution of source/drain resistance to total device series resistance was one of several motivating factors for implementing a raised source/drain (RSD) structure with finFET technology.[19], [26], [27] Pictured in Figure 1-13, RSD design allows for greater cross-sectional area of the source and drain regions allowing for less of a voltage drop in the source/drain regions despite a slightly increased length of the connection.

$$R_{sd} = \rho_{sd} \frac{S}{A} \tag{1-14}$$

In order to minimize the contributions of this resistance term, it is important to optimize RSD geometry and minimize the resistivity of the source and drain materials used in the process to create the RSD. RSDs are created through a selective epitaxial growth (SEG) step in the process flow, and doping is achieved either in-situ during growth or by a post growth ion implant. Therefore, resistivity of the RSD can be decreased by modifying ion implant and subsequent anneal conditions or by growing in more active dopants and subjecting these regions to a further activating anneal after growth before silicidation.



Figure 1-13. Diagram showing the current pathways in a transistor source or drain when RSD structures are implemented. The increased cross-sectional area is able to offset the increased path length through the uniform resistivity material.

## **1.2.4.4 Contact resistance**

Broadly, contact resistance is defined as the resistance associated with current travelling through two dissimilar materials.[28] In the case of contact resistance in a MOSFET, the contact of interest is between the source/drain regions and their respective silicides that interface with the metal interconnect. The resistance associated with these metal semiconductor contacts dominates the total device series resistance for modern devices due to the very small contact areas achievable for these processes.[29] Therefore improvements that can be made to this area will directly translate into higher performance devices.

When a metal (or silicide) and a semiconductor are physically put in contact with one another, the electrical characteristics (Figure 1-14) can either have Ohmic (linear) or Schottky (rectifying) behavior. The behavior of this contact can be predicted from physical properties of the materials using the Schottky-Mott rule. This rule can predict the contact Schottky barrier height  $\Phi_{Bn}$  for an n-type semiconductor. For clean a clean interface without gap states, ohmic behavior results from  $\Phi_{Bn}$  values which are approximately equal to room temperature thermal energy  $k_bT$  or less.


Figure 1-14. Metal-semiconductor contact current voltage behavior. Ohmic contact shown on left and Schottky diode rectifying behavior shown on right.

$$\Phi_{Bn} = \Phi_m - X_{sc} \tag{1-15}$$

In an n-type semiconductor-metal ohmic contact, it is the electrons which possess energy higher than  $k_bT$  that allow for conduction over the potential barrier via thermionic emission (Figure 1-15, left). Contact resistance for this type of junction is determined by equation 1-16 where A\* is Richardson's constant. Alternatively, When the n-type doping concentration is degenerate, the

$$R_c = \frac{k_b}{qA^*T} \exp\left(\frac{q\Phi_{Bn}}{k_bT}\right) \tag{1-16}$$

depletion region width of the semiconductor becomes thin such that carriers can tunnel through the barrier (Figure 1-15, right).[12], [30] When this occurs, ohmic contact behavior can result despite not fulfilling the Schottky-Mott relation stated above. The resistance of said contact still is dependent on the Schottky barrier height, so the selection of materials is of upmost importance. In this case, contact resistance can be related to the active donor concentration within the n-type semiconductor by

$$R_c \approx exp\left[\left(\frac{2\sqrt{\epsilon_s m^*}}{\hbar}\right)\left(\frac{\Phi_{Bn}}{\sqrt{N_D}}\right)\right]$$
 (1-17)

equation 1-17. Typically, the metal contacting the source/drain regions of a MOSFET is a silicide due to favorable work functions and the ability to form a clean interface. Therefore, in order to minimize contact resistance of a MOSFET, it is of upmost importance to maximize the active dopant concentration in the semiconductor.



Figure 1-15. Band structures for two types of ohmic contacts. For the left structure, conduction is achieved through a small barrier height relative to  $k_bT$ . Electrons which have sufficient energy (depicted in blue) can easily pass the barrier. For the right structure, a much higher barrier height prevents the flow of thermal electrons however due to the high doping level of the n-type semiconductor, the depletion region is sufficiently thin to allow for tunneling current.

# **1.2.5 MOSFET Strain Engineering**

When dealing with device dimensions on the order of several nanometers, the addition of strain into certain regions of the device becomes unavoidable. This effect can be used to the advantage of the device designer by controlling the direction of the strain in certain areas of the transistor. The usage of strain engineering has allowed for significant performance gains starting with the 90 nm MOSFET node and has been a major influencing factor for the continued usage of finFET devices over nanowire FETs.[31][32] As early as 1900, a relation between electron mobility of a semiconductor and the effective mass of conducting electrons had been observed

$$\mu = \frac{q\tau}{m^*} \tag{1-18}$$

by Paul Drude (equation 1-18). [33] While this relation is overly simplistic for applications within MOSFET technology, it illustrates that beneficial properties can result by changing the effective mass of carriers in a controlled way. In reality, it is desirable to use strain to decrease the carrier effective mass in the channel direction, while increasing the carrier effective mass in directions orthogonal to the channel. Lower effective mass in the channel direction improves carrier transport properties. Higher effective mass orthogonal to the channel and increases the density of states in the channel region close to the surface.

Theory has suggested that for short channel MOSFETs, carrier velocity will be saturated and therefore independent of mobility below the 30 nm node.[17], [34] While velocity saturation does occur in modern devices, full ballistic transport of carriers still does not occur. The ballistic efficiency  $B_{sat}$  for a device can be defined through two relations as follows below.[35]  $r_c$  is

$$B_{sat} = \frac{1 - r_c}{1 + r_c} = \frac{I_{dsat}}{I_{dsat, ballistic}}$$
(1-19)

defined as the backscatter rate of the device.  $I_{dsat, ballistic}$  is the theoretical maximum achievable drive current for a given gate voltage. For high performance devices in 2001,  $B_{sat}$  values of 0.45 were able to be obtained. Even for ballistic carriers, ballistic current  $I_{dsat, ballistic}$  is determined by the injection velocity.[34] Injection velocity can be approximated by equation 1-21

$$I_{dsat} = Q_s v_{inj} \tag{1-20}$$

$$v_{inj} = \frac{4}{3\pi} \sqrt{\frac{4N_s \pi \hbar^2}{m_x m_D}}$$
(1-21)

where N<sub>s</sub> is the inversion layer density,  $m_x$  is the effective mass along the channel direction and  $m_D$  is the 2-D density of states mass.[35] Thus it can be seen that performance increases will be realized through increasing the effective mobility of the channel region in modern devices. It should be noted that the effects of strain on mobility are anisotropic and the effects observed are dependent on the channel orientation on the wafer. Changes in mobility can be related to the stress in the direction of carrier flow  $\sigma_{\parallel}$  and the out of plane stress  $\sigma_{\perp}$  through their respective piezoelectric coefficients  $\pi_{\parallel}$  and  $\pi_{\perp}$  as seen in equation 1-22.[31]

$$\frac{\Delta\mu}{\mu} \approx \pi_{||}\sigma_{||} + \pi_{\perp}\sigma_{\perp} \tag{1-22}$$

The intentional implementation of strain within a MOSFET has been demonstrated to impact device performance as early as the 1980s where the effects of biaxial tensile strain were studied.[36], [37] Since then, focus has shifted to applying uniaxial strain to the channel region of transistors for mobility enhancements.[31], [32] Through these enhancements pMOS and nMOS drain current increases of >50% and 32%, respectively, have been observed.[38] Several different methods have been used for implementing this uniaxial strain for both planar and finFET devices. The primary method for pMOS has been to etch and regrow the source/drain regions replacing substrate silicon with SiGe through selective epitaxial growth (SEG).[39], [40] SiGe has a greater lattice constant than silicon and therefore places the channel of the transistor under compressive stress improving hole mobility. This method has the additional benefit of being able to easily grow RSD structures discussed in section 1.2.4.3 for source/drain resistance improvements. More pronounced RSD structures have the effect of further increasing the strain associated with these regrown regions.[39] These SiGe source/drain regions are then either doped via ion implant or via epitaxial growth of SiGe:B.

Uniaxial compressive strain has been shown to improve the hole mobility for pMOS transistors, however electron mobility requires uniaxial tensile strain within the transistor channel. Originally with planar devices a tensile nitride etch-stop film was applied to the transistor over the gate and spacer regions. [41], [42] Thicker nitride films have the effect of increasing strain on the channel.[41] This technology was used to augment nMOS performance to complement the performance gains seen with SiGe selective epitaxial growth for pMOS. Unlike the pMOS situation however, additional vertical components of stress are introduced in this method due to the downward compression on the gate stack. More recently, selective epitaxial growth techniques have been developed to implement tensile strain into nMOS channels.[43], [44] In a similar method to using SiGe with a larger lattice constant than silicon to apply a compressive stress in pMOS, cubic Si:C alloys can be used to apply a tensile stress to nMOS channels. This Si:C which is grown using a similar SEG process typically employs ~1% carbon and can either be doped in-situ or with a post growth implant and anneal.[43]–[45] Typically phosphorus is used as a dopant for these source/drain regions as the diffusivity of arsenic is enhanced in the presence of carbon, while phosphorus diffusivity is retarded. Recently it has been demonstrated that similar levels of strain can be achieved for SEG processes using a high concentration of phosphorus instead of carbon. Epitaxially grown highly doped Si:P (HDSiP) is an alternate material of interest for forming RSD regions in finFETs.[2]-[5] HDSiP has the ability to give rise to a similar degree of uniaxial tensile strain as Si:CP or Si:C alloys only with preferable electrical properties.

### **1.3 Epitaxially Grown Highly P Doped Silicon**

Tensile strain inducing materials that be implemented into transistor process flow via SEG are of importance for CMOS technology. The need for materials advances in this region stem from the benefits of uniaxial tensile strain on channel mobility, RSD structures on finFET

source/drain resistance and minimization of contact resistance through active dopant incorporation.

Originally, the SEG process used to grow Si:C required ultrahigh vacuum chemical vapor deposition (UHV-CVD).[43], [44] Improved techniques which take advantage of more advanced precursors have been developed more recently to allow for growth using low temperature, reduced pressure CVD (RP-CVD). This new process is much more favorable for process integration than UHV growth. RP-CVD selective epitaxy processes were used to grow Si:C can either be doped via ion implantation or introduction of phosphine gas  $(PH_3)$  into the growth reactor which would in-situ dope the regions. [46]–[48] Through experimentation with precursor pressures and in-situ doping of these RSD regions, it was determined that a similar degree of tensile strain can be obtained in films which do not incorporate carbon at all by substituting for a high concentration of phosphorus. The resulting material is called highly doped Si:P (HDSiP) and is defined as a film grown via selective epitaxy with greater than  $\sim 1 \times 10^{21}$  cm<sup>-3</sup> phosphorus content. Strain measurements of HDSiP thin films were determined to possess higher than expected values of tensile strain than previous works on phosphorus doping.[49], [50] Despite the concentrations of incorporated phosphorus being well above the solid solubility limit of phosphorus in silicon, no defects can be observed through analysis of the layers in transmission electron microscopy (TEM). The lack of observable defects combined with the high concentration of inactive phosphorus which can be measured through electrical means suggests that a high concentration of sub-microscopic phosphorus defect clusters are being grown into the layers. Density functional theory (DFT) analysis has predicted the presence of a stable  $Si_3P_4$ dispersed phase (also denoted as P<sub>4</sub>V clusters) responsible for the high level of tensile strain and inactive phosphorus in the film (Figure 1-16).[51]–[54] Fundamental analysis of HDSiP grown

through a selective epitaxy process and the clusters present in the material will be the focus of this work.



Figure 1-16. Pseudocubic Si<sub>3</sub>P<sub>4</sub> crystal structure. When one unit cell of Si<sub>3</sub>P<sub>4</sub> is dissolved in silicon, this known as a P<sub>4</sub>V complex.[54]

# **1.3.1 Processes for Growing HDSiP**

Selective epitaxial growth (SEG) processes are employed to deposit epitaxial layers of HDSiP onto bulk substrates or fin structures.[55] This allows the epitaxially grown material to only grow on existing crystalline regions, but not amorphous or polycrystalline regions. The key for integrating this material deposition process into the transistor fabrication process is its selectivity. SEG takes place after the gate stack and nitride spacers have already been fabricated. Typically nMOS SEG occurs after pMOS SEG of SiGe:B as well and thus thermal budget must be a concern for growth temperatures as well as post growth annealing if necessary.[56] Selectivity is necessary for this step as it is undesirable to grow any n-type material onto the gate stack, spacer regions, or even on the masked pMOS transistor regions of the wafer. Selectivity ratios of >20 are desired.[57]

Two epitaxial growth methods are used to grow HDSiP onto silicon substrates. These are referred to as the co-flow process and the cyclic deposition etch (CDE) process. In order to have a selective growth process, either a selective growth is necessary or a selective in-situ chemical vapor etch (CVE) step is introduced into the process. Both the co-flow and CDE processes incorporate non-selective growth with selective etchants. Etchants are chosen such that their etch rate for amorphous or poly-silicon is much higher than for crystalline silicon. Material that is grown onto the gate stack, or masked regions will not grow epitaxially like material that is grown onto the source/drain regions and therefore will get etched away completely. These two approaches differ by when the etchant is introduced into the cycle. In the co-flow process, etchant gas and precursor gas are introduced into the CVD chamber simultaneously.[58]–[60] In this case, growth and etching take place as concurrent processes. For the CDE process, precursor gasses are separated from etch gasses with a purge step.[55], [59], [61]–[63] This process is done in 2 cycles as shown in Figure 1-17. Upon the completion of a growth step, the chamber is purged



Figure 1-17. The four steps in a cyclic-deposition-etch (CDE) epitaxial growth process. and then etch gas is introduced for the desired time. This is then purged and precursor gas is reintroduced. Growth step time is limited as the etch selectivity is dependent on polysilicon layer

thickness. While the CDE method has been reported to produce lower resistivity HDSiP films than the co-flow method, it also involves a longer process time due to the requirement that the chamber be purged multiple times during growth.[2]

High level of dopant incorporation are achieved by implementing low substrate temperatures, high pressures within the growth chamber and more reactive precursors. The lower the growth temperature and the higher the growth rate, the higher the possible phosphorus incorporation into the film. Growth temperatures typically range from ~500 °C to 700 °C. Pressures within the growth chamber range from 20 Torr to atmospheric pressure (760 Torr) and hydrogen is used as a precursor flow gas.[62] As process conditions modified to incorporate too high phosphorus concentration, epitaxial breakdown results. Layers start to incorporate high concentrations of interstitials which then agglomerate into pyramids on the surface of the growing film.[62], [64] Less ordered surface roughness also can be an issue at high incorporated concentrations of phosphorus.

The phosphorus precursor used for both processes is phosphine gas (PH<sub>3</sub>). For the coflow process, dichlorosilane (DCS) is used as the silicon precursor and also as the etchant. Some works have incorporated hydrochloric acid (HCl) gas simultaneously with DCS in the co-flow process for enhanced etching characteristics.[58] The CDE process typically uses Silcore (ASM proprietary Si<sub>3</sub>H<sub>8</sub>) as the silicon precursor as it is able to achieve faster growth rates at low temperature than disilane (Si<sub>2</sub>H<sub>6</sub>) or silane (SiH<sub>4</sub>).[57] Etching during the etch cycles is completed with HCl or Cl<sub>2</sub> and can be catalyzed by a low partial pressure of GeH<sub>4</sub>.[59]

### **1.3.2 Characterization of HDSiP**

HDSiP is a unique material that has the potential for improving nMOSFET performance, and as such warrants further investigation from a fundamental standpoint. HDSiP is defined as an epitaxially grown film on silicon with a phosphorus concentration above the solid solubility

limit (>1x10<sup>21</sup> cm<sup>-3</sup> P). Film thicknesses range from 30 - 100 nm and concentrations up to 6x10<sup>21</sup> cm<sup>-3</sup> P have been exhibited. Typically, the creation of a phosphorus doped layer at these concentrations above solid solubility is associated with the formation of orthorhombic or monoclinic precipitate phases. [65], [66] With HDSiP systems grown via the co-flow or CDE selective epitaxial growth processes, this is not the case. From TEM micrographs, no observable defect formation is present.[2], [3], [5] It should be noted that for higher concentration HDSiP films, dark contrast within the layer compared to the substrate is observed.[3], [5] Despite this lack of observable defects, the majority of phosphorus dopant species are grown into the film in an inactive state. This observation suggests the presence of a sub-microscopic clustering phenomena taking place.

#### 1.3.2.1 Activation of HDSiP

HDSiP has demonstrated the capability to incorporate higher than solubility levels of phosphorus in a defect free film. It was through that through annealing of the film, perhaps the electrical activation limit of phosphorus in silicon could be surpassed as well. This experiment was undertaken by two groups separately and significant activation was achieved.[4], [5], [67] Typically, as-grown active carrier concentrations between  $1.5-2.5 \times 10^{20}$  cm<sup>-3</sup> P have been observed with Hall-effect measurements independent of the concentration of chemically incorporated phosphorus. Spike annealing of a  $2.3 \times 10^{21}$  cm<sup>-3</sup> P sample at 1000 °C activates the film to  $6 \times 10^{20}$  cm<sup>-3</sup> P on level with the previously reported electrical activation limit for phosphorus. However, undesirable levels of diffusion occur during this spike annealing treatment. [68] The introduction of millisecond laser annealing to HDSiP thin films is able to all but mitigate this observed diffusion for temperatures below 1200 °C.[5] For laser fluences equivalent to temperatures between 1050 – 1200 °C, significant activation of dopants up to  $\sim 1 \times 10^{21}$  cm<sup>-3</sup> P was achieved.[5] [67] Higher temperatures and shorter time intervals of a

nanosecond pulsed eximer laser have been able to produce the highest performance electrical properties of an HDSiP film. The excimer laser annealing done by Rosseel et al. was in the melt fluence regime and through melting and epitaxially re-growing of the film, complete activation of a  $2.3 \times 10^{21}$  cm<sup>-3</sup> P HDSiP film was possible. This type of thermal process is not useful beyond a scientific environment, however, as melt processes are not compatible with modern finFET transistor technology.

With this capability to achieve significant activation of dopants with the laser DSA, it is important to ensure strain stability. Film strain preservation is necessary for device performance. X. Li et al. studied the effects of the non-melt millisecond laser DSA on film strain. For DSA temperatures below 1000 °C no appreciable effect on strain can be observed.[5] Temperatures of 1250 °C and above exhibited a significant degradation in straining level. This indicates that higher millisecond anneal temperatures should be avoided on account of strain loss. During these high temperature DSA anneals diffusion of dopants causing broader dopant concentration profiles for the finished source and drain were also noticed. An interesting effect of unknown origin occurs for intermediate DSA temperatures between 1050 °C and 1150 °C where an increase in the tensile strain of the film occurs. Though small, this effect is reproducible and counter to what conventional logic would dictate. Between the strain preservation, diffusion minimization and dopant activation, DSA temperatures between 1150 °C and 1200 °C appear to be optimal.

### 1.3.2.2 Contact resistance of HDSiP

The primary reason for the investigation of HDSiP films over Si:C and Si:CP films is due to its ability to form lower contact resistance junctions. All three films are able to achieve similar degrees of tensile strain, however dopants in HDSiP do not need to compete with carbon for substitutional lattice sites like in the carbon containing films. Due to this, and the ability to

achieve extremely high levels of phosphorus in HDSiP films, record setting low nMOS contact resistance values approaching  $1 \times 10^{-9} \Omega \text{cm}^2$  have been obtained for HDSiP/silicide junctions.[6], [7], [69] This is important for transistor design as the resistance of the source/drain to silicide contact resistance currently dominates device series resistance.

Traditionally, contact resistance measurements are conducted using the transmission line measurement (TLM) technique where several contacts are made with different spacings on a material of uniform resistivity.[28] By extrapolating the distance between contacts to zero, the contributions to the overall resistance measurement from the substrate material is negligible and contact resistance can be measured.

$$R_{measured} = R_{substrate} + 2R_c \tag{1-23}$$

Two different silicide materials are being considered for use in transistor design with HDSiP: titanium (TiSi<sub>2</sub>) and nickel (NiSi) silicide. Titanium typically exhibits superior performance from a device standpoint but requires higher temperature to undergo the silicide reaction (~800 °C). Nickel is beneficial from a thermal budget standpoint as the reaction temperatures required for silicide formation are below 550 °C, but the obtained contact resistance values are almost an order of magnitude higher than TiSi around  $1 \times 10^{-8} \Omega \text{cm}^2$ .[70], [71]

#### 1.3.2.3 Strain in HDSiP

Much discussion has been entertained in the literature as to the nature of the strained state of epitaxially grown HDSiP layers. Strain in HDSiP is typically measured and reported using high resolution X-ray Diffraction (HR-XRD). In place of reporting strain values in percentages or the deviation in epi-layer lattice parameter from that of the substrate ( $\Delta a_0$ ), oftentimes units of equivalent %C<sub>sub</sub> are used. Equivalent %C<sub>sub</sub> refers to strain measurement in the film being comparable to that of an Si:C film with x percent carbon. This is not the best way of reporting strain as different authors in prior literature have found different strain dopant calibration factors

for carbon in silicon. However it can make for facile comparison to current industry Si:C stressors. In addition, due to the nature of a strained film, the measured lattice parameter in the epitaxial growth direction  $a_{\perp}$  will differ from  $a_{rel}$ , the lattice parameter of the material free from epitaxial constraints. These two parameters can be related through the stiffness coefficients of silicon C<sub>11</sub> and C<sub>12</sub> via equation 1-24. In this case,  $a_{\parallel}$  is the lattice constant of the unit cells parallel to the surface (perpendicular to the growth direction) which is approximately equal to the substrate lattice constant for non-relaxed, pseudomorphic films.

$$a_{\perp} = \left[a_{rel}(y) - a_{||}\right] * \left(1 + 2\frac{C_{12}(y)}{C_{11}(y)}\right) + a_{||}$$
(1-24)

Different approaches can be used to arrive at an equivalent %C<sub>sub</sub> from HR-XRD measurements, though typically conversion is done through applying the relation determined from a mixture with  $\beta$ -SiC (equation 1-26). This approach is favored to the approach of using Vegard's law with diamond (equation 1-25).[72]  $a_C = 3.567$  Å and  $a_{SiC} = 4.360$  Å were used for these calculations.

$$a_{rel} = a_{Si}(1 - y) + a_C(y) \tag{1-25}$$

$$a_{rel} = a_{Si}(1 - 2y) + a_{SiC}(2y) \tag{1-26}$$

Many experimental claims have been made suggesting that the strain of HDSiP films is greater than what would be predicted given the smaller atomic radius of P alone. As a way of outlining the degree of this variation, Figure 1-18 compiles data from various sources in the literature showing the deviation in measured lattice parameter,  $\Delta a_0$ , as a function of phosphorus concentration. For literature sources that only reported a trendline, or a value of dopant strain calibration factor,  $\beta$ , these trends have also been reported.[73]–[75]

Purely mathematical calculations for the expected strain behavior based on the smaller covalent radius of phosphorus can be predicted from the tetrahedral covalent radius determined by L. Pauling.[76] Pauling determined tetrahedral covalent radii for phosphorus and silicon as 1.10 Å and 1.17 Å respectively. A lattice parameter for phosphorus bonded in a diamond cubic configuration (equation 1-27) needs to be calculated despite phosphorus not forming into this type of compound in nature. This would be expected to introduce significant error into the calculation. This trend from equation 1-28 is shown for comparison with experimental data.

$$a_{DC} = \frac{8r}{\sqrt{3}} \tag{1-27}$$

$$\Delta a_0 = 5.431 - (1 - x)a_{Si} + x\frac{8r_P}{\sqrt{3}}$$
(1-28)

Experimentally obtained lattice parameter deviation with respect to incorporated phosphorus concentration has been plotted showing negative deviation from the lattice parameter of silicon (5.431 Å). In all cases, phosphorus doping was found to induce tensile strain into the doped layers. Conventionally doped samples measured with XRD (Cohen, Yagi et al and Pearson & Bardeen) exhibited the lowest degrees of tensile strain. [49], [50], [73] Phosphorus doping was conducted by solid source diffusion for all three of these works. Phosphorus precipitation of these doped regions would be expected for doping concentrations above  $\sim 1 \times 10^{21}$ cm<sup>-3</sup> and has not been accounted for. Precipitation would cause strain relaxation in the measured values obtained by Cohen and Yagi et al. The work of Celotti et al. used XRD to measure the lattice constant of highly phosphorus doped crystals grown using the Czochralski method rather than thin doped layers. [74] They obtained a higher value of tensile strain with respect to phosphorus concentration, however as their highest doped sample was 8.05x10<sup>19</sup> cm<sup>-3</sup>, this trend has been greatly extrapolated.[74] The data shown in Figure 1-18 from McQuhae & Brown was obtained from stress measurements conducted through wafer-bending experiments rather than XRD.[75] This difference in measurement technique may give rise to higher experimental error.

The trends observed here clearly delineate the difference in reported strain of the HDSiP samples (Li et al, Weeks et al.) and conventional phosphorus doped silicon. Weeks et al. were able to model their experimental data well by implementing Vegard's law with an additional bowing parameter  $\theta_{SiP}$ .[3] The trend they found can be seen in equation 1-29. This relation assumes a lattice constant  $a_P$  for a phosphorus as if it were to form into a

$$a_{SiP}(y) = (1 - y)a_{Si} + ya_P + y(1 - y)\theta_{SiP}$$
(1-29)

diamond cubic compound similarly to described above in equation 1-27, however using a different value for the atomic radius of phosphorus. This value is arrived at through using equation 1-27 with the covalent radius of P in a P-P bond as 2.14 Å (double the covalent homonuclear radius of phosphorus).[3]



Figure 1-18. Reported values for strain as a function of phosphorus concentration in silicon for both conventional phosphorus doped methods and HDSiP. Covalent radius estimate included for comparison.[3], [5], [49], [50], [73]–[77]

It can be seen that deviations in layer strain exist between HDSiP and reported values for conventionally phosphorus doped silicon. These deviations form a central part of the argument that proposes an Si<sub>3</sub>P<sub>4</sub> dispersed phase that is grown into HDSiP accounting for the grown-in inactive dopant. Lattice parameters were predicted by Huang et al. for Si<sub>3</sub>P<sub>4</sub> of a = b = 5.027 Å and c = 4.998 Å which agree with the experimental HDSiP HR-XRD strain measurements by Li et al. when used with Vegard's law.[52] It should be noted that other computational works on the same material have reported slightly different values for the lattice parameters of Si<sub>3</sub>P<sub>4</sub>.[54], [78] Lu et al. derived lattice constants for Si<sub>3</sub>P<sub>4</sub> of a = b = 4.9862 Å and c = 4.9861 Å using the local density approximation (LDA) and a = b = 5.0908 Å and c = 5.0907 Å using the generalized gradient approximation (GGA).[78] M. Xu et al. determined Si<sub>3</sub>P<sub>4</sub> to have a cubic structure where a = b = c = 5.038 Å.[54]

More recently, it has been suggested through further DFT work by Dhayalan et al. that similar strain values can be obtained through DFT for a given level of phosphorus doping whether the phosphorus exists in P<sub>4</sub>V complexes or is dispersed substitutionally without vacancies.[79] This draws into question the validity of previously reported experimental strain measurements for conventionally phosphorus doped material. As HDSiP is able to obtain significantly higher than solid solubility levels of phosphorus in an epitaxial film, it is difficult to compare to conventional doped values without significant extrapolation. For this reason, future studies on lattice parameter are needed for phosphorus doping concentrations above 1x10<sup>21</sup> cm<sup>-3</sup> where all of the phosphorus resides on substitutional lattice sites with minimal excess point defects. Such a doping situation can be obtained through melt laser annealing.

### **1.3.2.4 Simulation work regarding HDSiP**

In addition to the lattice parameter predictions using DFT, ab-initio methods have been employed to evaluate the stability of various clusters of phosphorus with silicon and other point

defects. By predicting thermodynamic properties of a materials system with DFT, stable clustering configurations can be predicted. Sahli et al. used DFT to calculate theoretical binding energies and formation energy values for a large number of possible phosphorus clusters.[51], [53] These findings suggest that vacancy clusters decorated by 3 or 4 phosphorus atoms would exhibit the highest degree of stability in silicon.[51], [53] This result agrees with the ab-initio results obtained by Dhayalan et al. [80]

Cluster Type	Formation Energy (eV)	Binding Energy (eV)
V	+3.55	N/A
Ι	+3.45	N/A
$\mathbf{P}_2$	+0.07	+0.07
$P_3$	+0.13	+0.13
PV	+2.35	-1.21
$P_2V$	+1.06	-2.49
$P_3V$	+0.22	-3.33
$P_4V$	-1.12	-4.67
PI	+2.60	-0.85
P <sub>2</sub> I	+1.41	-2.04
P <sub>3</sub> I	+1.42	-2.03
$PI_2$	+4.32	-2.58

Table 1-1. Formation energies and binding energies of phosphorus clusters in silicon [53]

Several groups have focused specifically on DFT analysis these vacancy clusters. When P<sub>4</sub>V clusters are looked at as a uniform material, the result is what is referred to as Si<sub>3</sub>P<sub>4</sub>. The groups that have simulated Si<sub>3</sub>P<sub>4</sub> have determined lattice parameters of the material using DFT. Lattice parameter simulation for this material has been discussed in above in section 1.3.4.3.[52], [54], [78] Band structure and mechanical property predictions have also been made which can be useful for future experimental analysis. Band gap for Si<sub>3</sub>P<sub>4</sub> has been predicted to be within a range from 0.10 eV to 0.93 eV through various groups using LDA or GGA[52], [54], [78] Bulk moduli for Si<sub>3</sub>P<sub>4</sub> were found to range from 74.28 to 78 GPa.[52], [54], [78].

### 1.3.2.5 Analytical characterization of HDSiP

The primary focuses thus far in the field of HDSiP have been to demonstrate the enormous potential that this material has for improving transistors and how it can be integrated into existing transistor process flow. M Bauer et al. and J.M. Hartmann et al. have also contributed significant works studying the effects of growth conditions on the resultant HDSiP films.[56]–[60], [62], [63] As far as fundamental studies go, there has been some analytical characterization of HDSiP films conducted which will be overviewed in this section. It is important to understand the results of what characterization has been already completed. That way studies already done conclusively are not repeated and the current findings may build off of previous results.

One of the first aspects of HDSiP that was characterized was the concentration of grownin phosphorus in the HDSiP films. As HDSiP is a silicon phosphorus alloy, obtaining accurate concentration values for chemically incorporated phosphorus is not facile. Secondary ion mass spectrometry (SIMS) data could not be initially relied on as there are no adequate standards with known phosphorus dose for this type of matrix material ( $>1x10^{21}$  cm<sup>-3</sup> P). Thus SIMS data was correlated with data from HR-XRD strain data and RBS.[3] As has been mentioned in section 1.3.2.3, the strain that has been observed for HDSiP in HR-XRD does not closely match the expected values for strain. These expected values are based off of the concentration of phosphorus in SIMS and the lattice parameter contraction that has been reported previously. [50][73] At this point, it could be suggested that this observation points to inaccurate ion yields from SIMS, thus it is important that the concentration data from SIMS be correlated with RBS. An RBS study was conducted by Weeks et al. on an HDSiP sample with 5.9 % phosphorus measured by SIMS which confirmed that this SIMS measurement was accurate.[3] Further RBS work was done by Dhayalan et al., however, the data obtained was not reported on except for changes in channeling yield with respect to annealing.[80] An RBS/SIMS correlation study of several different concentration HDSiP films could be useful in assuring SIMS concentration accuracy.

Positron annihilation spectroscopy has yielded possibly the most conclusive experimental evidence of dopant-defect interactions in HDSiP thus far. Analysis was conducted on HDSiP to understand changes in the vacancy population with respect to annealing conditions.[80][67] A reduction in the vacancy concentration of a 4.6% phosphorus sample was observed after exposure to two pulses of a 1200 °C 0.5 ms laser anneal.[80] The degree of reduction was such that after annealing, the doppler broadening S/S<sub>B</sub> parameter was close to 1. This sort of vacancy concentration suggests that phosphorus-vacancy clusters are breaking up or being filled in and that this is related to the observed increase in active carrier concentration.[79], [80] Corresponding with this decrease in the vacancy population is the observation of an increase in the RBS minimum yield for phosphorus from 7.9% to 17.6%. This data suggests that more phosphorus resides on interstitial sites after ms annealing.[79] However, when the experimental results presented are analyzed, the RBS plots in the region for phosphorus are too noisy to draw decisive conclusions from. The reactions mechanisms responsible for these effects were not addressed. It was suggested that P<sub>4</sub>V clusters break up and some of the remaining inactive phosphorus occupies interstitial sites or forms into P<sub>2</sub> substitutional clusters.[79][81]

Another technique used in the same study was electron spin resonance spectroscopy (ESR). ESR was conducted on as-grown and ms laser annealed samples by Dhayalan et al.[80] No reliable data could be obtained for as-grown HDSiP films due to excessively lossy nature. Comparison of the annealed films to a phosphorus doped control confirmed electrical data that only about 50% of the total phosphorus concentration was active after the ms laser anneal.

Through review of the existing literature on HDSiP it can be seen that comprehensive fundamental understanding of HDSiP is incomplete. Further work in this area is needed prior to incorporation of HDSiP into transistor process flow. The work completed in this document aims to fill gaps in the collective fundamental knowledge on HDSiP.

### **1.4 Dopant-Defect Interactions in Phosphorus Doped Silicon**

Phosphorus is one of the two most commonly used n-type dopants in silicon. In nature, phosphorus tends to form into compounds where it can either have three single bonds and a lone pair of electrons or have an expanded valence forming five bonds.[82] In silicon it has a similar level of solubility to arsenic, though it has a higher diffusivity and a smaller atomic radius. These properties can be beneficial or detrimental to usage depending on the application. The atomic radius of phosphorus is smaller than silicon resulting in tensile strain for highly doped regions.[77] Phosphorus located on a substitutional lattice site (Figure 1-19) in silicon tends to donate an electron to the conduction band of the semiconductor and thus is used as an n-type



Figure 1-19. Substitutional phosphorus atom (purple) takes the place of a silicon atom in the lattice.

dopant. Substitutional phosphorus will occupy an energy state below the conduction band by just 39 meV such that it exists in an ionized state at room temperature.[49]

# 1.4.1 Native Silicon

At room temperature and standard pressure, silicon can exist in any of three solid variants: amorphous silicon, polycrystalline silicon and single crystalline silicon. For the purposes of this document, the single crystalline variant will be dealt with exclusively. In its crystalline form, silicon exhibits a diamond cubic crystal structure (Figure 1-20). Also visualized as an interpenetrating face-centered cubic structures, diamond cubic is within the Fd-3m space group. In this structure, each atom is covalently bonded to its four nearest neighbors in a tetrahedral geometry. Through advances with purification techniques and crystal growth methods, silicon ingots of 99.9999999% (9N) purity and lacking in extended defects can be grown routinely using the Czochralski method. These ingots are then sliced and polished into 300 mm wafers which become the basis for the epitaxially grown films studied herein.



Figure 1-20. The diamond cubic unit cell.

### **1.4.2 Intrinsic Point Defects in Silicon**

Despite the incredible purity of crystalline silicon that is able to be achieved, these crystals still are defective in nature. Zero-dimensional defects in the silicon crystal are referred to as point defects. These sub-nanometer sized defects cannot be resolved in silicon with conventional microscopy methods. However, the motion of these point defects and the reactions that point defects undergo can be observed indirectly through diffusion and clustering phenomena.

There are two main classifications of intrinsic point defects which will be discussed here: the self-interstitial and the vacancy. For all temperatures above 0 K, even the highest quality silicon crystals that can be grown possess these types of defect in an equilibrium state. An equilibrium exists between intrinsic point defects and the material surfaces which act as a source and sink. Due to the higher energy associated with surface atoms' bonding environment, at times it can be energetically favorable for the atom to reside in the bulk as an interstitial or for a bulk atom to move to the surface creating a void.

Self-interstitial atoms in silicon can exist in two different configurations, as a splitinterstitial and as a true interstitial. A split-interstitial is where two silicon atoms share occupation of a single lattice site. This configuration can exist with the two atoms in any of



Figure 1-21. A depiction of a split interstitial in silicon in the [001] direction.

multiple angular configurations with respect to the lattice. When one of the two split interstitial atoms is a dopant species, this gives rise to the interstitialcy diffusion mechanism for dopants which will be discussed later.

True interstitials are where the extra atom takes on a position external to the silicon crystal lattice in a non-bonding configuration. This typically takes place on one of two different sites within the crystal lattice. The tetrahedral interstitial sites occupy the quarter sites left vacant in the diamond cubic structure as well as the edge sites and unit cell center. Energetically, this position is favorable to a hexagonal interstitial site which exists at a (3/8, 3/8, 3/8) location within the crystal. For a self-interstitial to migrate between the (1/4, 1/4, 1/4) tetrahedral site to the (1/2, 1/2, 1/2) tetrahedral site it must pass through the hexagonal interstitial site. This movement is associated with a migration energy of 1.4 eV.[83], [84]

The diffusion of self-interstitials in silicon can be measured through means such as radioactive tracer studies however different experiments have reported several orders of magnitude different diffusivity values for a given temperature.[85] Regardless, diffusion of self-interstitials in silicon occurs many orders of magnitude faster than dopant species.

Even though the definition of a point defect is a zero-dimensional impurity, various higher order configurations of di- and tri-interstitials have been suggested to form and can also be classified as point defects. At room temperature, it has been suggested through ESR measurements made by Corbett et al. that these higher order interstitial clusters are stable where single interstitials are not.[86] It is unknown what geometric configuration these clusters would possess or if it is even required that two interstitials be associated with adjacent sites.

Vacancies are the other main type of intrinsic point defect in silicon. Vacancies exist where a silicon atom is missing from its respective lattice site (Figure 1-22). Vacancy related

defects are also theorized to exist in higher order clusters of multiple vacancies at room temperature which can disperse and diffuse more rapidly at elevated temperature. These



Figure 1-22. A depiction of a mono-vacancy within a silicon lattice.

vacancies facilitate diffusion of larger dopant impurities through the lattice. Similar to interstitials, the diffusivity of vacancies in silicon is many orders of magnitude faster than that of dopant species. Higher order vacancy clusters also form at room temperature where monovacancies are not stable.[86] When a vacancy collides with an self-interstitial, recombination will occur.[87], [88]

$$V_{Si} + Si_i \to Si_{Si} \tag{1-30}$$

In certain scenarios such as ion implantation or high temperature thermal oxidation, these point defects (particularly interstitials) can exist in much higher concentrations than the value at thermal equilibrium. In certain situations where the concentration of one or the other type of point defect is supersaturated, extended defects such as dislocation loops or stacking faults can precipitate.[89]

### 1.4.3 Phosphorus Solubility in Silicon

Samples annealed in the sub-melt recrystallization regime have reported levels of activation up to  $6 \times 10^{20}$  cm<sup>-3</sup>, however the solubility limit of phosphorus in silicon has been reported at a higher value around  $1 \times 10^{21}$  cm<sup>-3</sup> at around 1100 °C.[65], [66], [68], [85], [90]–[92] This discrepancy arises due to the ability of phosphorus to be driven in via infinite source

diffusion above its solid solubility limit atypical of most diffusion processes.[93] At these high concentrations, soluble substitutional phosphorus exists in an equilibrium state with submicroscopic inactive SiP defect clusters that are too small to be resolved in TEM. The phosphorus-silicon phase diagram shows that the maximum solubility for phosphorus in silicon is around  $1.25 \times 10^{21}$  cm<sup>-3</sup>.[65]

### **1.4.4 Phosphorus Clustering in Silicon**

Several different reports on highly phosphorus doped systems have suggested the presence of certain types of clusters formed by inactive phosphorus in silicon. A cluster in this case is defined as a sub-microscopic defect in the silicon lattice containing one or more dopant species as well as zero or more additional point defects. The distinction made here between a cluster and a precipitate is that a cluster does not possess long or short range order. On the other hand a precipitate takes on an observable lattice structure of its own, the cluster in this case exists within the silicon lattice and is insufficiently large to have a quantifiable crystal structure.

Clusters types can be broken down into three subgroups: interstitial clusters, vacancy clusters and phosphorus substitutional clusters. Phosphorus interstitial clusters (PICs) are defects consisting of n inactive phosphorus and m silicon atoms occupying a space greater than n+m lattice sites within the matrix. As early as the 1980's phosphorus was theorized to form SiP sub microscopic clusters during in-diffusion doping along with substitutional phosphorus due to the fugacity of the diffusion source.[93]–[95] The breakup of these clusters partially explained the emitter push effect (discussed in the following section) and the source of extra interstitials during the diffusion of high phosphorus concentration regions.[95], [96] In addition to this, the formation of PICs was more recently reported in the work of Keys et al.[97], [98] It was observed that by implanting silicon with P<sup>+</sup> instead of Si<sup>+</sup>, formation of {311} type defects could be suppressed.[97]–[99] This was explained by a portion of the interstitial species resultant from

the implant forming into interstitial clusters decreasing the concentration of free interstitials. Phosphorus vacancy clusters have also been proposed to form through the work of Takamura et al.[100], [101] Here a factor of  $2x10^6$  enhancement in the diffusion of buried boron marker layers was observed. This diffusion enhancement was concurrent with the deactivation of a high dose phosphorus implant sample that had undergone liquid phase epitaxial regrowth. The epitaxially regrown layers were observed to have very low concentrations of point defects. Therefore, the interstitial species responsible for the enhanced marker layer diffusion were generated upon deactivation and phosphorus-vacancy clusters were formed as a result.

### 1.4.5 Phosphorus Diffusion in Silicon and the Emitter Push Effect

Phosphorus diffusion in silicon takes place with several concurrent phenomena which at the time of their first observation were not well understood and gave rise to much controversy in the field. Two different effects were noticed that do not occur with other dopants. The first is called the emitter push effect. The emitter push effect was named for an anomalous diffusion effect of the base region of a bipolar junction transistor (BJT) during emitter predeposition and drive-in steps.[96][102]–[106] Typically, BJTs were made with a highly phosphorus doped emitter and a boron doped base. As the emitter predeposition and drive-in steps were being conducted, greatly enhanced diffusion of the boron base region directly under the emitter was observed. It was concluded that this effect was not due to pileup or rejection of the boron by the phosphorus, but rather by point defect injection during the phosphorus diffusion. As the diffusivity of both vacancies and self-interstitials in silicon are very high, enhanced diffusion of a buried boron marker layer as deep as 12 microns beneath the BJT base could be noticed.[85], [96] As boron diffuses by a mixed interstitialcy and vacancy mechanisms ( $f \sim 0.85$ ) the nature of the point defects being injected by the phosphorus diffusion was the subject of much controversy.[85] Several contrasting mechanisms were proposed to explain the type of point

defect released as well as how that type of point defect would be produced in a diffusion process. This all was combined with theories to describe the second anomalous diffusion behavior observed by phosphorus: kink & tail diffusion.[93], [95], [107]–[111]

Kink and tail diffusion describes the way phosphorus diffuses from a high concentration layer (Figure 1-23). The high phosphorus concentration plateau region diffuses slowly while a



Figure 1-23. Theoretical SIMS dopant concentration profile showing deviations in the diffuse profile from error-function behavior during phosphorus predeposition. Concentrations below  $\sim 2x10^{20}$  cm<sup>-3</sup> P will be electrically active (solid lines) while concentrations above that level will be clustered (dotted line). [93]

lower concentration "tail" region diffuses orders of magnitude faster. These two regions are separated by a kink in the dopant concentration profile which is related to the diffusion temperature.[108] Various mechanisms have been proposed to explain this anomalous diffusion behavior. The first widely accepted model for phosphorus kink and tail diffusion in silicon was developed by Fair and Tsai in the 1970's, but was later rejected on account of future evidence supporting a contrary mechanism.[107] The Fair and Tsai model was based around the theory that phosphorus diffused primarily through a vacancy mediated mechanism. It suggested that inactive  $P^+V^=$  clusters were formed in the high concentration plateau region during predeposition. These P<sup>+</sup>V<sup>=</sup> clusters then dissolve at the kink concentration during the diffusion step yielding phosphorus atoms and an excess of free vacancies. These vacancies would then be injected into the material bulk responsible for the emitter push. This conclusion was later rejected by the scientific community in favor of an interstitial diffusion mechanism and formation of interstitial clusters in the highly doped plateau region. Several concurrent processes can account for both anomalous diffusion observations wrapping up phosphorus diffusion into one unified theory.[93], [95]

Kink and tail diffusion and the phosphorus diffusion mechanism in silicon are described as follows. First, SiP precipitates form during phosphorus incorporation above the soluble concentration regardless of which method of incorporation is used. (diffusion source, ion implantation, CVD, etc). When the material is heated, these SiP clusters are relatively immobile. This accounts for the low apparent diffusivity of the plateau region. At the kink concentration between the plateau region and the tail these clusters undergo a dissolution reaction forming substitutional phosphorus and a self-interstitial. This self-interstitial then diffuses into the bulk. This self-interstitial oversaturation in the post-kink region is what causes the emitter push effect

as well as the enhanced diffusivity of phosphorus in tail. Phosphorus in this region diffuses from substitutional sites via a purely interstitialcy mechanism (f = 0.99).[93], [94] However, it has been noted that upon cooling the tail region activates close to 100%, indicating that the diffusing phosphorus species must be occupying substitutional sites. This suggests that the fraction of phosphorus atoms that exist as inactive split interstitials at any given time is less than 1%, alluding to a very high atomic jump frequency of this split interstitial species. If these processes were all that were taking place however, it would still not explain the situation where a kink and tail diffusion profile can be noted even for a completely activated layer with no SiP precipitates. The kink is formed even in this scenario due to phosphorus interstitialcy atoms diffusing in [100] silicon having a maximum transport capacity dependent on temperature and independent of anneal time.[108], [112] The lattice simply cannot support greater than the kink concentration flux of interstitialcy phosphorus and self-interstitial species. Thus, phosphorus concentrations above the kink concentration effectively act as an infinite source for the diffusing species. It should be noted that non-clustered substitutional phosphorus in the high concentration region can still exhibit diffusion. This high concentration region diffusion takes place through a vacancy mediated mechanism in direct contrast to what has been predominantly studied for phosphorus diffusion at lower concentrations.[93], [94] The diffusivity of phosphorus through this mechanism is inherently orders of magnitude smaller than that for interstitialcy diffusing phosphorus of the tail region, but the contributions to the overall diffuse profile cannot be excluded. These phosphorus diffusion processes combine to form a very complex mechanistic model. This model accurately depicts the given observations and anomalous effects while being in line with all of the fundamental laws logic.[93], [94]

### **1.4.6 Phosphorus Precipitates in Silicon**

As opposed to a cluster, a precipitate in this work is defined as an agglomeration of atoms within the single crystal bulk that possesses its own long or short scale ordering. A precipitate will take on its own crystal structure which is unique from that of the silicon matrix. This precipitate can exist within the matrix either with or without a preferred orientation in the silicon crystal lattice. Above the solubility limit of phosphorus in silicon, precipitates such as these have been observed. These observations have typically been reported for high phosphorus concentration predeposition from P<sub>2</sub>O<sub>5</sub>, POCl<sub>3</sub> or PBr<sub>3</sub> sources. The types of defects that have been observed are wide ranging and without standardized nomenclature. Dot like defects and rod-like or "needle" defects  $\sim 20$  nm in size have been observed by a number of sources and may be classified more like extended defects rather than ordered precipitates.[66], [113]–[115] Larger micron sized orthorhombic SiP precipitates have been classified to be structurally similar to macroscale SiP.[116] Monoclinic crystal structure SiP has also been reported for high dose phosphorus samples doped via ion implantation.[117] It is interesting that none of these types of precipitates have been observed for HDSiP alloys. Even though HDSiP can have a phosphorus concentration well above the solubility limit in silicon, the lack of precipitates indicates the presence of additional stabilizing phosphorus clusters.

### **1.5 Statement of Research Objectives**

As it can be seen from the preceding sections, HDSiP is a novel material intended for use as a source and drain in nMOS transistor technology for future device nodes. HDSiP shows promise for improving transistor performance and decreasing power consumption by imparting uniaxial tensile strain on the channel and decreasing device series resistance. These potential performance gains are inconsequential unless it can be shown to be compatible with current transistor manufacturing processes. In order to demonstrate compatibility, the properties of

HDSiP must be well understood such that they will evolve in a controlled manner during process flow. The ability to achieve record setting activation and contact resistance after a laser DSA is not helpful unless this activated state can be stable throughout the additional thermal processes that take place after activation. The ability to impart a high degree of tensile strain on the channel is inconsequential if this strain is relieved before the product is finished. Therefore, it is important to understand the stability and property evolution of HDSiP after subsequent thermal treatments.

To understand the way properties evolve with respect to annealing conditions it is imperative to understand the underlying fundamental science behind this evolution. By studying phenomena such as deactivation kinetics, point defect release and defect formation, a wholistic picture can be formed about the behavior of the material. Once fundamental understanding of the dopant-defect interactions within HDSiP is obtained, incorporation into transistor process flow will be possible. At this point, the beneficial properties of the material will be able to be realized for improving transistor performance and decreasing power consumption.

### CHAPTER 2 EXPERIMENTAL METHODS

#### 2.1 Experimental Methodology

The experimental approach utilized for gaining fundamental understanding of HDSiP in this work followed the scientific method. As opposed to an engineering approach where properties and performance are sought to be optimized, the scientific approach taken in this work seeks to purely understand the phenomena taking place in this novel material. Without having control over the growth process and the majority of relevant growth parameters, experiments were constrained to post-growth characterization and studying the effects of various post-growth annealing conditions on electrical properties and microstructure. As the clustering theorized to be present in HDSiP layers is too small to be resolved in TEM, and in too low of concentration to be probed and characterized directly with routine analytical methods, indirect methods were used to gain knowledge about the HDSiP material system. Point defects were introduced to shift reaction equilibriums which can be quantified electrically. Defect formation and evolution was used as another such method of acquiring indirect evidence of atomic processes. Once several pieces of indirect evidence all start pointing towards similar findings, broader conclusions can be drawn about the fundamental material processes at play.

# 2.2 Thin Film Growth

Epitaxial HDSiP films were grown in a reduced pressure chemical vapor deposition (RP-CVD) system on nominally p-type substrates. The growth mechanism used followed the co-flow method roughly as described in section 1.3.1 using precursors of DCS and PH<sub>3</sub>. Growth temperature was maintained below 650 °C for films of all phosphorus concentration. HDSiP film thicknesses and incorporated phosphorus content for the wafers used in this study have been listed in table 2-1. In this case, HDSiP phosphorus concentration and thickness values were obtained through correlation to HR-XRD. Concentration values were correlated from strain data using the relation described by Li et al. [5] Samples grown with sub  $1 \times 10^{21}$  cm<sup>-3</sup> phosphorus content in the surface layer have been termed as low-doped Si:P (LDSiP). These wafers possess relatively low doping concentrations in comparison to what can be attained using the co-flow process to make HDSiP and can exhibit complete activation of dopants upon annealing indicating the lack of clusters that define HDSiP.

HDSiP Phosphorus	Surface HDSiP layer	Contains Buried Marker
Concentration (cm <sup>-3</sup> P)	Thickness (nm)	Layer (yes/no)
5.0x10 <sup>20</sup> (LDSiP)	40	no
$1.9 \times 10^{21}$	47	no
3.6x10 <sup>20</sup> (LDSiP)	54	no
4.5x10 <sup>20</sup> (LDSiP)	55	no
$1.9 \times 10^{21}$	62	no
$3.0 \times 10^{21}$	75	no
$4.4 \times 10^{21}$	41	no
$1.6 \times 10^{21}$	38	no
Control Marker Layer	N/A	yes
5.0x10 <sup>20</sup> (LDSiP)	No measurement	yes
$4.4 \times 10^{21}$	55	yes
5.0x10 <sup>20</sup> (LDSiP)	57	yes
$1.0 \times 10^{21}$	80	yes
$2.0 \times 10^{21}$	79	yes
$2.5 \times 10^{21}$	75	yes

Table 2-1. List of HDSiP wafer information

Several of the wafers used in this work were grown with an in-situ doped 5 x  $10^{19}$  cm<sup>-3</sup> P buried marker layer as depicted in Figure 2-1. The marker layer wafers used in this study were grown using SiH<sub>4</sub> and PH<sub>3</sub> up until the HDSiP surface layer. The HDSiP layer is grown using the same co-flow method as above. The purpose of this marker layer is to be able to analyze the point defect injection of the surface layer by monitoring diffusivity enhancements of the marker layer. Phosphorus is used as the marker layer dopant as it is a purely interstitial diffuser and thus, diffusivity enhancements can be attributed to excess interstitial populations. These phenomena are described in further detail in section 2.7.



Figure 2-1. Diagram showing the epitaxial film layers of the control (top) and HDSiP containing buried marker layer wafers. Marker layer depicted thickness has been exaggerated for figure clarity.

Figure 2-2 outlines an example of the phosphorus concentration profile with respect to

depth for a specific marker layer wafer sample. A control sample with no HDSiP surface layer

was also grown such that a baseline for phosphorus marker layer diffusion could be calculated.



Figure 2-2. Phosphorus concentration profile showing 55 nm thick surface HDSiP layer and a buried  $5 \times 10^{19}$  cm<sup>-3</sup> P buried marker layer with a peak position of 220 nm.

### 2.3 Annealing Techniques

A variety of methods are used to conduct annealing for thermal processes within transistor process flow. The decision to use one method or another is based on the time and temperature scales targeted for the anneal. Time scales used for this work range from millisecond annealing with a scanning laser to multiple day long annealing in a tube furnace. Control of the temperature and ambient atmosphere are of upmost importance for consistency of results.

#### **2.3.1 Furnace Annealing**

Furnace annealing is used for the longest time scale thermal processes within semiconductor manufacturing. For the tube furnace used in this work, timescales were limited to greater than 5 minutes to ensure the sample is at thermal equilibrium at the set temperature for the majority of the anneal time. This ensures that the contributions to the thermal budget from the heat up ramp and cool-down ramps are minimal. Heating is accomplished in a tube furnace by heating coils which surround the fused silica tube. Temperature is measured before and after each anneal manually with a thermocouple placed at the annealing position of the samples. The maximum attainable temperature of this tube furnace is  $\sim 1200$  °C before the fused silica tube and carrier will start to fuse together, and the temperatures used for this work were below 900 °C. Flow rate of the flow gas is maintained at 5 normal L / min for short time anneals (<4h). For long time inert anneals (>4h) a bubbler system is used to prevent backflow of atmospheric  $O_2$  and water vapor. Flow rates of the flow gas are minimized while maintaining a slight overpressure in the tube. Samples are placed on a silicon carrier wafer (face up for oxidizing anneals, upside down for inert anneals). For reproducibility of results it is necessary to maintain samples at the same position along the tube as gradients in temperature exist between the coils of the furnace. After the designated anneal time, samples are pulled out of the furnace area and left to sit in the end of the tube for 5 minutes. Samples are still exposed to the ambient of the flow gas during this

time. After 5 minutes, samples have cooled sufficiently to have negligible effects to the surface upon cooling the rest of the way to room temperature under normal atmosphere.

## 2.3.2 Rapid Thermal Annealing

Rapid thermal annealing (RTA) and rapid thermal oxidation (RTO) are conducted using an AG Associates Heatpulse 4100 system. By using radiative heating, significantly faster heating ramps can be achieved compared to a furnace anneal. Heating rates on the order of 200 °C/s can be obtained with a maximum achievable temperature of 1100 °C limited by lamp power. RTA and RTO are advantageous for use in various semiconductor manufacturing processes as very accurate temperature control can be obtained. Temperature control is conducted using a proportional integral derivative (PID) controller to determine lamp input power. Parameters for this lamp intensity are based off of temperature measurements from a thermocouple sandwiched between silicon carrier wafers. Coefficients for the PID are different for each temperature and optimized through trial and error.

### 2.3.3 Dynamic Surface Annealing

Similar to how flash lamp annealing can achieve faster temperature ramp rates than furnace annealing, laser annealing gives access to by far the shortest time scale anneal durations. This allows for laser anneals to access higher temperature regimes while maintaining a low thermal budget. This allows for maximum dopant activation with negligible diffusion.[118] An added benefit to laser annealing is that only a selected area of the surface layer of the silicon wafer is heated at one given time. This means that heat dissipation can take place through the wafer bulk rather than having to dissipate through mostly radiative means. In effect, extremely high cooling rates can be obtained with the potential for achieving high dopant activation levels while staying in the sub-melt regime. The laser anneal utilized in this study is an Applied Materials Vantage® Astra<sup>TM</sup> dynamic surface annealing (DSA) system. In this system, an 810
nm laser with a spot size of 22.4 mm is scanned across the wafer section in question. Fluences used for this setup correlate to temperatures between 900 and 1250 °C. The raster speed is equivalent to a 0.25 ms exposure time at this temperature.

For some wafers, a range of DSA anneal temperatures were desired. In these cases, the wafer was either broken up into pieces or annealed in laser stripes. In the former case, a section of wafer ranging from a half wafer sample to a 30 mm x 50 mm coupon was annealed over several beam raster cycles. No stitch line resistivity differences could be observed within measurement error for the electrical characterization techniques used. For stripe anneal samples, a single raster of the beam was completed a set distance (5 mm) away from another raster line at a different temperature (Figure 2-3). Due to the small amount of energy imparted on the sample within an anneal, areas not directly exposed to the beam did not exhibit the effects of the anneal. All areas of stripe annealed wafers were exposed to a 450 °C substrate heater. Samples for testing were harvested from completely within the bounds of the given anneal stripe.



Figure 2-3. Diagram of a series of DSA stripe anneals on a 300 mm (001) silicon wafer.

### 2.4 Thermal Oxidation of Silicon

Thermal oxidation of silicon can be a very useful tool in analyzing a novel material. Oxidation can be a reliable method of removing material through consuming crystalline silicon from the surface and etching with buffered oxide etch (BOE) or dilute hydrofluoric acid (HF). Perhaps more importantly to this project, oxidation represents a facile method of conducting point defect engineering. When a sample is being oxidized, silicon self-interstitial species get injected into the bulk by the advancing oxidation front. This effect can be taken advantage of for studying atomic reactions at play within thin surface films through the application of Le Chatelier's principle.[119]

Le Chatelier's principle dictates that for the chemical reaction listed as equation 2-1, the addition of more species A will cause the forward reaction to proceed. This will continue until K reaches its equilibrium value,  $K_{eq}$ . Equilibrium is defined as when the rate of the forward

$$aA + bB \leftrightarrow cC + dD \tag{2-1}$$

$$K = \frac{[C][D]}{[A][B]} \tag{2-2}$$

$$K = K_{eq} \Big|_{R_{forward} = R_{reverse}}$$
(2-3)

reaction is equal to the rate of the reverse reaction. As atomic scale reactions are being considered within this work, consumption or generation of point defects will be the limiting step of the reaction. For activation mechanisms, a dopant-defect cluster, AX, dissolves yielding a substitutional dopant species, A, and a point defect, X. For this case, first order decomposition rate kinetics can be assumed as the limiting rate of reaction is the dissolution of the cluster. For

$$R_{activation} = \frac{d[A]}{dt} = k_{activation}[AX]$$
(2-4)

deactivation mechanisms, a substitutional dopant species A combines with a point defect X to cause clustering. In this case, second order rate kinetics are involved as the limiting step requires that both independent species collide with one another.

$$R_{deactivation} = \frac{-d[A]}{dt} = k_{deactivation}[A][X]$$
(2-5)

The important feature to note with these rate equations is that Le Chatelier's principle can be used to understand the nature of activating and deactivating reactions taking place in a material. Given that the activation and deactivation reaction limiting steps are described as above (equations 2-4 and 2-5), changes in reaction rate can be directly linked to the introduction of selfinterstitial point defect species.[119] For an interstitial mediated reaction, addition of extra interstitial species will increase the deactivation rate causing the formation of dopant-interstitial clusters. For a vacancy mediated reaction, the addition of extra interstitial species will decrease the deactivation rate. This is due to self-interstitials recombining with free vacancies in the material. This will cause a decrease in the concentration of vacancies available for participation in clustering reactions.

These effects are important to realize even when dealing with annealing that takes place in inert atmosphere. Even in the most well controlled inert annealing environment, it can be extremely difficult to completely prevent oxidation. As these effects described above cannot be realistically prevented it is important to understand and account for rather than neglect these effects.

## **2.4.1 Thermal Oxidation Kinetics**

The films in this study are only several tens of nanometers thick. It is important to understand oxidation kinetics such that a reasonable amount of the layer is consumed by the

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oxidation reaction. Thermal oxidation of silicon occurs following the Deal-Grove model (equation 2-6). This model accounts for thermal oxidation being reaction limited for thin oxide

$$t = \frac{x^2}{B} + \frac{x}{(B/A)} + \tau$$
(2-6)

layers (linear rate dependence) while being diffusion limited at larger oxide thicknesses (parabolic rate dependence).[120] The Deal-Grove model is typically robust for thick oxide formation, however does not capture the initial stages of oxidation where a rapid oxide formation has been observed. This initial rapid oxidation tends to progress with a linear dependence and has been observed for oxide layer thicknesses below ~ 30 nm. For this initial stage of oxide growth, empirical models have been used to predict oxidation progress with success.[121], [122]

Oxidizing time frames studied in this work range from several seconds to 1 hour, at temperatures between 700 and 900 °C resulting in the growth of oxides that do not exceed 45 nm (Figure 2-4). It can be seen that under these conditions, oxidation will occur primarily in the rapid growth regime. As such, much faster oxidation than predicted by the Deal-Grove model is to be expected.



Figure 2-4. Thermal oxidation progress of a silicon surface at 700 °C under dry ambient showing the difference between traditional Deal-Grove linear model and the initial stages of oxidation.

In addition, other important factors have an influence over oxidation rate. Oxidation rate is a function of chemical dopant concentration, active dopant fraction, and strain.[123]–[125] All of which are present in the HDSiP layers oxidized within this work. Prior to utilizing oxidation as a method of influencing dopant reaction equilibrium by interstitial injection, empirical knowledge of the oxidation kinetics for these HDSiP films is required.

## **2.4.2 Oxidation Injection of Interstitials**

Knowledge of the growth rate of a thermal oxide on silicon and HDSiP is very important as interstitial injection during oxidation is proportional to the oxidation rate.[126] This dependence can be written out as a mathematical expression derived from the Deal-Grove model for the linear regime (equation 2-7) and for the parabolic oxidation regime (equation 2-8).[126] Coefficients B and A are the Deal-Grove oxidation rate constants.[120] As was stated in the previous section, this work will focus on oxidation in the initial oxidation regime which follows

$$R_{gen} = \theta\left(\frac{B}{A}\right) \tag{2-7}$$

$$R_{gen} = \theta B^{1/2} t^{-1/2} \tag{2-8}$$

a linear trend with respect to time. The associated rate of this trend will be determined empirically. It is still assumed that the rate of interstitial generation,  $R_{gen}$  at the oxidizing interface will be proportional to this oxidation rate through a factor  $\theta$ .  $\theta$  is the ratio between silicon atoms injected into the bulk as self-interstitial species and silicon atoms consumed by the oxidation reaction. Experimental values for this parameter measured with a buried loop detector range from 2.4x10<sup>-3</sup> to 5.9x10<sup>-3</sup> atoms/atom at temperatures ranging from 850 to 950 °C.[127] Translated into a interstitial flux with respect to time, this is equivalent to values on the order of  $10^{10}$  atoms/cm<sup>2</sup>s.



Figure 2-5. Compiled data from D. Skarlatos et al. estimating interstitial flux as a function of oxidation rate for a thermally grown oxide on (001) silicon at various growth temperatures.[127]

The purpose for the inclusion of Figure 2-5 is to provide a reference point for observed interstitial fluxes. The oxidation experiments done within this work have been predominantly carried out at lower temperature (700 °C), and thus it could be expected that the interstitial flux would be below  $10^9$  atoms/cm<sup>2</sup>s however similar oxidation rates for HDSiP were observed at 700 °C to the rates reported here at higher temperature. The effects of biaxial tensile strain on interstitial injection factor  $\theta$  are unknown and thus deviations from these estimates of interstitial injection could be possible.

# **2.5 Electrical Characterization Techniques**

Characterization of any semiconductor material would not be complete without electrical characterization. Ultimately it is the electrical properties that result from material modifications that are of interest for use in transistor applications. In addition to this, many times electrical measurements can be much more sensitive to minute changes in structure or local chemistry than

more specific analytical techniques. For the purposes of this project, it was of utmost importance to use electrical characterization of active dopant fraction to determine dissolution and clustering reactions within HDSiP. Four-point probe measurements and Hall-effect measurements were used extensively for this purpose.

## **2.5.1 Four-Point Probe**

Used for obtaining sample resistivity values and creating wafer resistivity maps, the fourpoint probe measurement setup was an integral part of characterizing the electrical properties of samples from this work. Meaningful data can be obtained in a matter of seconds using the fourpoint probe where a Hall-effect sample run would require upwards of 10 minutes to obtain data with significant statistical relevance. In taking a four-point probe measurement, four tungsten carbide tips are contacted to the wafer surface with a constant pressure being applied through a spring preload system. These probe tips are of identical tip curvature, radius and spacing, S, from one another to minimize measurement errors. A current source is attached to the outer probes while a volt-meter is used to take measurements from the inner two probes as can be seen in Figure 2-6. From here, it needs to be determined that the sample exhibits ohmic behavior given



Figure 2-6. Schematic showing four-point probe configuration on a sample surface. Outer tips are connected to a current source and inner tips are connected to a volt meter. Probe tips are separated by spacing s.

the value of the current being applied. To do this, the current is varied over a window from approximately 100  $\mu$ A to 10 mA. Once a current region where the sample exhibits ohmic behavior is found, measurements are taken at the upper current limits of this region to enhance significant figures of the voltage measurement. These readings are taken with the sample and probe tips in the dark to eliminate photo-excited current contributions to the measured voltage.

The benefits to using four probe tips over just a two-probe system is that the four-probe system eliminates contributions from contact resistance,  $R_c$ , spreading resistance,  $R_{sp}$ , and the probe resistance itself,  $R_p$ .[128] These resistance types are shown with their corresponding physical locations in Figure 2-7. These resistances still exist in the outer current carrying probes however do not impact the voltage measurements due to the negligible amount of current that passes from the sample into the voltage measuring probes.



Figure 2-7. Physical locations that correspond to the three different types of resistivities involved with carrying out four-point probe measurements.

The expression for measuring sample resistivity in a four-point probe configuration can be derived from the relationship between resistivity, current density and electric field. It can be assumed that the current introduced to the sample of uniform resistivity will spread out evenly in all directions according to equation 2-10.

$$E = J\rho = -\frac{dV}{dr} \tag{2-9}$$

$$J = \frac{I}{2\pi r^2} \tag{2-10}$$

Integrating the above expression gives the voltage at a distance, r, away from the probe which can be simplified to equation 2-12.

$$\int_{0}^{V} dV = \int_{0}^{r} -\frac{I\rho dr}{2\pi r^{2}}$$
(2-11)

$$V_{point} = \frac{I\rho}{2\pi r} \tag{2-12}$$

In a system where the current is flowing to another probe, the current flowing to the second probe needs to be accounted for and a second term to the equation is introduced using r' the distance from the point in question to the other probe.

$$V_{point} = \frac{I\rho}{2\pi r} - \frac{I\rho}{2\pi r'}$$
(2-13)

Given a four-point probe situation with equidistant probes at spacing S, the voltage at the probe tip adjacent to the current input (probe 2 in Figure 2-6, referenced to the voltage at probe 1) can be described by the following in equation 2-14. Probe spacing, S, for the Jandel system used in this study is 0.1588 cm.

$$V_{2} = \frac{l\rho}{2\pi(S)} - \frac{l\rho}{2\pi(2S)} = \frac{l\rho}{4\pi S}$$
(2-14)

The voltage at probe tip 3 can also be computed in a similar fashion.

$$V_3 = \frac{l\rho}{2\pi(2S)} - \frac{l\rho}{2\pi(S)} = -\frac{l\rho}{4\pi S}$$
(2-15)

The voltage, V, measured by the volt meter then becomes equation 2-16 which can be solved for resistivity.

$$V = V_2 - V_3 = \frac{l\rho}{4\pi S} + \frac{l\rho}{4\pi S} = \frac{l\rho}{2\pi S}$$
(2-16)

$$\rho = \frac{2\pi SV}{I} \tag{2-17}$$

The above equation 2-17 assumes that the dimensions of the sample are infinite in length and width as well as thickness which for the purposes of this work cannot be assumed. When dealing with real samples which are typically silicon wafers, a correction factor, F, needs to be introduced.

$$\rho = \frac{2\pi SFV}{I} \tag{2-18}$$

This method of introducing a correction factor requires that measured samples be thinner than the probe tip spacing. All samples analyzed for this work fulfilled this condition. Three different independent factors play into computing F, the sample thickness ( $F_1$ ), sample lateral dimensions ( $F_2$ ) and the distance from the probes to the sample edges ( $F_3$ ).[129], [130]

$$F = F_1 F_2 F_3 \tag{2-19}$$

For samples with a conductive layer on an oppositely doped substrate, the built-in junction at the interface is sufficient to electrically isolate the conductive layer giving rise to the following expression for  $F_1$  (equation 2-20). For samples with thin conductive layers (t < 400 µm for 0.1588 cm probe spacing) The equation for  $F_1$  can be further simplified to equation 2-21.

$$F_{1} = \frac{t/s}{2\ln\left(\frac{\sinh t/s}{s}/(\sinh t/2s)\right)}$$
(2-20)

$$F_1 = \frac{t/s}{2\ln(2)}$$
(2-21)

The lateral dimension correction factor  $F_2$  can be computed in a similar manner. Data from the calculations for  $F_2$  result in the following plot for both circular as well as rectangular samples (Figure 2-8).



Figure 2-8. Correction factor plot for sample thickness for a four-point probe measurement system with probe tip spacing s.[128]



Figure 2-9. Correction factor plot for sample lateral dimensions for a four-point probe measurement system with probe tip spacing s.[128]

The correction factor  $F_3$  for placing the probe tips near the edge of a semiconducting sample can be determined through the following Figure 2-10. This factor is negligible for placement of tips greater than ~3 times the probe spacing dimension.



Figure 2-10. Correction factor plot accounting for edge effects. F31 is used for when probe tips are set up perpendicularly to close sample edge. F32 is used for when probe tips are set up parallel to close sample edge.[128]

For the situation where  $F_2$  and  $F_3$  need not be accounted for through careful selection of sample size and measurement collection location, the conductive layer resistivity can be calculated through equation 2-22.

$$\rho = \frac{\pi t}{\ln(2)} \left( \frac{V}{I} \right) \tag{2-22}$$

In the case where a value for sheet resistance (equation 2-23) is desired instead of resistivity, knowledge of the layer thickness is unnecessary.

$$R_S = \frac{\rho}{t} = \frac{\pi}{\ln(2)} \left(\frac{V}{I}\right) \tag{2-23}$$

## 2.5.2 Hall Effect

Of particular interest to this project is the ability to quantify dopant atoms which sit on substitutional lattice sites as well as those that exist in various clustering configurations. Conventional analytical techniques do not possess the ability to quantify dopants in their various bonding environments with the sensitivity necessary for studying this material. Hall-effect measurements have the capability to quantify the electrically active dopant species. Through manipulation of the conditions of activating and deactivating reactions, fundamental understanding about inactive dopant species present in the material can be obtained. A few key requirements are necessary for doing Hall effect of which the HDSiP samples measured in this work satisfy. First, the samples need to be planar and with uniform resistivity across the measured layer. Second, the material in question needs to be able to form an ohmic contact with the lead wires in the four corners of the sample. Finally, to minimize error in the measurement values, the contact size needs to be less than one tenth the side length of the square sample.

To prepare samples for Hall-effect measurements, sample surfaces are cleaned by etching the native oxide followed by a three-step solvent rinse. Pressed on indium contacts are then created on the corners of each 1 cm x 1 cm sample and braided copper lead wires attached to these contacts.

Prior to acquiring Hall-effect data, it is important to obtain the resistivity of the material studied which is typically measured using a van der Pauw measurement setup. In a van der Pauw



Figure 2-11. The two different van der Pauw measurement wiring configurations. Biases will be reversed for the volt meter and current source to give a total of four measurements.

setup, two adjacent contacts are connected to a current source and the opposing two adjacent

contacts are connected to a volt meter (Figure 2-11).[131], [132]

The bias on these connections is then reversed for another measurement and then two more measurements are taken by switching the current source and volt meter and using positive and negative bias. These four measurements are then repeated using the opposing configuration of adjacent contacts (Figure 2-11, right). This leads to two sets of four voltage measurements from which bulk resistance values can be obtained through Ohm's law. As in equation 2-24, R<sub>43,12</sub> indicates the bulk resistance value that corresponds to a voltage measured between contacts 1 and 2 given a current supplied between contacts 4 and 3.

$$R_{43,12} = \frac{V_{12}}{I_{43}} \tag{2-24}$$

These sets of bulk resistances are then averaged to obtain a resistance for configuration A,  $(R_A)$  and a resistance for configuration B,  $(R_B)$ .

$$R_A = R_{43,12} + R_{34,21} + R_{21,34} + R_{12,43}$$
(2-25)

$$R_B = R_{23,14} + R_{32,41} + R_{41,32} + R_{14,23}$$
(2-26)

To obtain a sheet resistance value,  $R_S$ , from these bulk resistivity values, the van der Pauw equation (equation 2-27) is employed.

$$\exp\left(\frac{\pi R_A}{R_S}\right) + \exp\left(\frac{\pi R_B}{R_S}\right) = 1$$
(2-27)

Values for  $R_A$  and  $R_B$  should be very similar for a square sample of uniform resistivity, in which case if  $R_A = R_B$  equation 2-27 simplifies as follows in equation 2-28.

$$R_S = \frac{\pi R_A}{\ln(2)} \tag{2-28}$$

As equation 2-28 requires nontrivial differential equations to solve, practically a modified approach is used to calculate  $R_S$  from averaged bulk resistance values  $R_A$  and  $R_B$  using numerical methods. A ratio term X is determined and from this, a new parameter z is defined as being equal to X or equal to the inverse of X.[133]

$$X = \left| \frac{R_A}{R_B} \right| \tag{2-29}$$

$$z = X \text{ if } X \le 1 \tag{2-30}$$

$$z = \frac{1}{X} if X > 1$$
 (2-31)

From this, the form factor F of the sample is computed using equation 2-32 and equation 2-33 where parameter a is defined by parameter z and is solved via an iterative process until convergence is met.[133]

$$F = \frac{-2\ln(2)}{\ln(a) + \ln(1-a)}$$
(2-32)

$$a^z = 1 - a \tag{2-33}$$

Using the value F for form factor, sheet resistance of the sample can be determined by the following equation 2-34.[133]

$$R_{S} = \frac{\pi F(R_{A} + R_{B})}{2\ln(2)}$$
(2-34)

Sample resistivity can be determined through equation 2-35 if the conductive layer thickness d is known. For this work, layer thickness values are determined by SIMS, XRD or XTEM.[133]

$$\rho = R_s d \tag{2-35}$$

Using resistivity data, additional useful electrical properties of the sample can be determined after some electrical measurements are collected in the Hall-effect configuration. The Hall-effect measurement configuration differs slightly from the van der Pauw configuration in that opposing contacts are connected to the current source and volt meter respectively. In addition to this, a magnetic field perpendicular to the sample surface is introduced as shown in Figure 2-12.[133]–[135]



Figure 2-12. The two different Hall-effect measurement setups. Voltage polarity will be reversed for both the current source and volt meter to permit a total of four different measurements. Measurements will be taken both with magnetic field in the up and down directions.

The principle behind the Hall-effect measurement is that the applied magnetic field will deflect charged carriers as they flow across the sample. This magnetic force on the carriers acts in accordance with the right-hand rule. This force is then countered by a Lorentz restoring force (equation 2-36).

$$F_L = -q(E + v x B) \tag{2-36}$$

Carriers affected by the Lorentz force build up on one side of the sample resulting in a measurable voltage across the other pair of opposing contacts. This voltage can be used to determine carrier type as well as calculate carrier mobility and sheet number. In practice this is done by calculating the difference in measured voltage between forward and reverse bias current directions with respect to magnetic field direction.

$$\Delta R_{13,24} = \frac{V_{24,+B} - V_{24,-B}}{I_{13,+B} - I_{13,-B}}$$
(2-37)

From this, mobility can be calculated with the sheet resistance value obtained previously and a measurement for the upwards and downwards magnetic fields supplied by a sensor in the unit.

$$\Delta B = B_{up} - B_{down} \tag{2-38}$$

$$\mu = \frac{10^8 \left( \Delta R_{13,24} + \Delta R_{24,31} \right)}{2R_S \Delta B} \tag{2-39}$$

A negative value for mobility is indicative of electrons being the majority carrier in the sample, where a positive mobility value indicates holes as the majority carrier. Sheet number is calculated alongside the mobility value using the same set of raw data following equation 2-40.

$$n_{sheet} = \frac{1}{R_s e\mu} \tag{2-40}$$

Once the sample sheet number has been calculated, a sample carrier concentration can be determined by correlating to the sample thickness, d.

$$n = \frac{n_{sheet}}{d} \tag{2-41}$$

### 2.6 Chemical Analysis Techniques

In order to determine clustering configurations of phosphorus within HDSiP, techniques that are sensitive to the chemical bonding environment and or give speciation information about elements are of critical concern. Few of the typical array of analysis techniques have the sensitivity to analyze a thin film of HDSiP due to the low concentrations of clustered versus active phosphorus. Surface sensitive techniques or techniques which can be done on a crosssection with a sub 100 nm probe size are necessary. The techniques discussed here fit these criteria despite some of these methods not yielding meaningful information on the local chemistry of HDSiP. Not discussing these null results is to waste the time and energies of the scientific community by not relaying to others that these methods have been attempted already.

## 2.6.1 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) is a surface sensitive technique used for compositional analysis of a material with a focus on understanding the local bonding environment. Monochromated Al K<sub>a</sub> X-rays (1486 eV) are directed at the sample surface causing the emission of core electrons. Based on the energy of these detected electrons, the surface material composition as well as its speciation can be probed. While the penetration depth of this energy of light is several microns, only the excited photoelectrons from the surface layer escape resulting in an effective probe depth of a few angstroms. When excited with sufficient energy above the vacuum energy level for the electron, a core electron and or a valence electron may be ejected. These ejected electrons, called photoelectrons (due to it being ejected by the absorption of a photon) are then collected by a detector which measures its energy. Energy discrimination is done through sweeping the voltage on a hemispherical collector throughout the desired photoelectron energy range. Electrons which have too high of energy collide with the outer wall of the hemisphere while electrons with insufficient energy collide with the inner wall.

For each core electron of each element except for hydrogen and helium which cannot be detected using XPS, there exists a standard value of energy which detected photoelectrons possess. This energy identifies the core electron that was emitted and the corresponding element. Bonding environment is evaluated through analysis of the shifts in these signal peaks. Spectra are normalized to the adventitious carbon 1s peak which exists for samples that have not been prepared in-situ. Samples that have been prepared in-situ have been normalized to the Si 2p 3/2 peak position.

### 2.6.2 Electron Energy Loss Spectrometry

Electron energy loss spectrometry (EELS) can yield important information about sample speciation and the bonding environment of a chemical species. EELS is typically conducted in a

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transmission electron microscope (TEM), where a beam of electrons is directed through the sample. The energy of the electrons which inelastically scatter are measured with a detector. Based on the atomic species, the local bonding environment of the absorbing atom and the local density of states (DOS), certain spectral features will be resolved.[136]

In a typical energy loss spectra, several main features may be resolved as shown in Figure 2-13. The first noticeable peak of the EELS spectra at 0 eV corresponds to the zero-loss peak (ZLP). This peak is constituted of electrons which have not inelastically scattered with the sample. At low energy loss values, scattering of the beam electrons by free or loosely boundelectrons in the specimen has occurred. These spatial oscillations in electron density are called plasmons and to obtain the most detailed chemical information from the sample their effects can be lessened by preparing extremely thin samples (<20 nm). Following this plasmon



Figure 2-13. Low energy EELS spectra for a silicon sample obtained from the EELS atlas. The silicon L edge can be clearly defined as well as the ridge to the right of the absorption edge which is due to plural scattering (scattering off of a core electron and a plasmon). [137]

peak, the probability of a beam electron scattering with slightly higher energy values decreases dramatically, as ionization cross-section decreases with increasing energy transfer. At higher energy loss values, inelastic scattering off of core shell electrons in the sample can occur yielding a sharp rise in the spectra. This loss peak occurs at the energy value where an incident electron from the beam is able to excite a core shell electron to the vacuum level. Just above this edge, the excited core electron behaves like a wave and will undergo plural scattering with the electrons of the adjacently surrounding atoms. This quantum effect reflects itself in the absorption behavior just above the absorption edge. The probability that an electron with energy  $E > E_{edge}$  will interact with a core electron is related to the energy landscape of unfilled states which the core electron can occupy.[136] This gives rise to the EELS near edge structure of the plot (ELNES) approximately 0-50 eV above the absorption edge which effectively mirrors the local density of states around the absorbing species. For thicker samples, plural scattering can dominate this energy range. Plural scattering is where the energy lost by the beam electron is due to an ionization event in addition to a plasmon interaction.

At slightly higher energies  $E > E_{edge} + 50$  eV the ejected core electron has sufficient energy to interact with the adjacent atoms atomic nuclei. These single-scattering events are related to the local bonding environment of the absorbing species. Study of the extended fine structure of the spectra after an absorption edge (EXELFS) can yield nearest neighbor information for the absorbing atom.[136] Use of these techniques (ELNES, EXELFS) can be complemented with simulations such as the FEFF9 software which can predict this behavior for a theoretical structure.[138] Comparison between theoretical structure spectra and experimental data is used to verify models.

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## 2.6.3 Secondary Ion Mass Spectrometry

Within this work, secondary ion mass spectrometry (SIMS) has been used extensively for dopant concentration depth profiling. SIMS is the primary method of conducting this type of analysis as it can be sensitive to dopant concentrations as low as  $1 \times 10^{13}$  cm<sup>-3</sup> and can obtain nanometer depth resolution. This type of profiling capability is necessary to measure diffusion of the HDSiP layers as well as monitor the diffusion of marker layers to understand point defect flux during annealing. There are two variants of SIMS that are conducted for sample analysis, static SIMS and dynamic SIMS. The former invokes the use of extremely low beam current over a large area and nonreactive primary ion species to undertake surface analysis without sputtering through more than the surface monolayer. The latter is what has been conducted for this work as a method of depth profiling. Dynamic SIMS uses a high primary beam current such that substantial sputtering of the sample surface occurs over time eroding a crater several hundred nanometers deep during the course of the analysis. Compared to static SIMS where the surface monolayer lifetime t<sub>m</sub> may be several minutes, dynamic SIMS bombards the surface with such high primary ion beam current I<sub>P</sub> that deeper monolayers within the substrate will be being sputtered concurrently with the surface layer. The more important metric for dynamic SIMS is

$$t_m = 1.09 x 10^{-4} I_P Y \tag{2-42}$$

$$t_{dp} = \frac{8.08 \times 10^5 d}{Y I_P} \tag{2-43}$$

The depth profile time, t<sub>dp</sub>, which can be expressed as a function of depth, d, the ratio of secondary ions generated per primary ion, Y, and the primary beam current, I<sub>P</sub>.[139]

SIMS works on the principle that when an ion is directed towards the sample with sufficient energy, atoms from the substrate matrix will be sputtered off. While the majority of these ejected species are neutral atoms or clusters, a small fraction is ejected as secondary ions. It is these secondary ions that come off at an angle towards the detector that are measured. The detector used is any of several types of mass spectrometers where mass-to-charge ratio of the secondary ion is counted. These ion counts, or the beam current of the selected secondary ion mass to charge ratio,  $I^q$ , is correlated with the sputter time to obtain the beginnings of a concentration profile. To convert from secondary ion beam current to concentration, the following equation 2-44 is used. I<sub>P</sub> and Y are as described above, C(A,z) is the concentration of species A with respect to depth, z, within the sample,  $\alpha^q(A)$  is the probability of sputtering an atom of A in charge state q, and  $f^q(A)$  is the detection efficiency of the detector for A in charge state q. Even when all of the process related variables are set, the secondary ion counts need to

$$I^{q} = I_{P}YC(A, z)\alpha^{q}(A)f^{q}(A)$$
(2-44)

be calibrated to a standard because of the ion sputtering probability  $\alpha^q(A)$ . Standards used for this purpose are typically ion implanted samples with a known dose of dopant species.

To convert the x-axis of the obtained profile from sputter time to depth within the sample, it is necessary to know the sputter rate. This can be difficult, particularly when dealing with samples that have multiple layers as sputter rates through different layers will be different. For a uniform material with an unknown sputter rate, profilometry can be employed to measure the depth of the SIMS crater. For the purposes of HDSiP, it is assumed that despite being a semiconductor alloy that the sputter rate is similar to that of native silicon. This is an assumption that would be interesting to test in the future.

For analysis of HDSiP samples, it is important to note that the ion sputter probability  $\alpha^q$  for phosphorus in HDSiP may be vastly different than for phosphorus in silicon. As there exists no reasonable standard for count normalization, additional techniques such as Rutherford

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backscattering spectroscopy (RBS) and HR-XRD have been used to complement SIMS concentration data.

## 2.6.4 Atom Probe Tomography

Atom probe tomography (APT) is a very specialized analysis technique that can net speciation and chemical information as well as structural information of a sample. This detailed analysis comes at the expense of a large amount of sample preparation, complex and expensive analysis and potentially difficult data manipulation. As an instrument, the APT is essentially a combination of a field ion microscope, a laser and a 2-dimensional detector with time of flight capabilities. The specific instrument used in this work was a Cameca local electrode atom probe (LEAP 5000) system which introduces an additional local annular electrode to aid in analysis.

Sample preparation consists of mounting the sample of interest onto a very high aspect ratio spire and using the annular milling feature of a focused ion beam (FIB) lithography tool to sharpen the sample into a very fine tip. For analysis, the tip is inserted into the ultra-high vacuum chamber of the APT where it is positioned with the tip center in line with the center of the local electrode (Figure 2-14). Liquid helium is used to maintain the tip at a very low temperature for more precise local position of the atoms and to decrease the probability of surface reconstruction. A constant voltage is applied to the tip during the duration of the experiment. A highly controlled applied voltage at the local electrode acting in combination with the pulsing of a 355 nm laser serves to field evaporate a single ion from the tip. The tip shape acts and the local annular electrode act as lenses for the released ion as it moves towards the detector. The original (x,y) position of the atom within the tip is related to the (x,y) coordinates where the ion impacts the detector. Mass-to-charge ratio (m/n) of the emitted ion can be determined through time of flight calculations. These calculations are based on the time that passes between the field evaporation of the ion and the ion impinging on the detector as shown in the following equations.

$$\frac{m}{n} = -\frac{2qV_{DC}}{v_{ion}^2} \tag{2-45}$$

$$v_{ion} = \frac{d}{t} \tag{2-46}$$

 $V_{DC}$  is the voltage applied to the tip, that nets field evaporation of an ion at velocity,  $v_{ion}$ .  $v_{ion}$  can be determined through correlation with the time between the evaporation event and the.



Figure 2-14. Schematic of a LEAP 5000 atom probe system. An annular electrode causes ionized species to diverge such that x-y coordinates on the position sensitive detector can achieve good spatial resolution.

ion impinging on the detector and a known distance of the flight path. Depth of the ion is related

to original atom z position through the assumption that evaporation of the tip is completed

atomic layer by atomic layer. Thus, when ions are being detected at repeating x,y coordinates,

the program assumes that these ion counts are from the next atomic layer deeper in the tip

# 2.7 Structural Characterization Techniques

Traditionally, chemical analysis techniques are interested in things such as speciation,

bonding environments and oxidation state of elements. Structural characterization is defined as

understanding about the configuration and spatial layout of the materials system including such phenomena as strain and extended defect formation. In modern times, the distinction between chemical and structural analysis techniques has become blurred. Techniques such as APT and SIMS are able to yield spatial information as well as speciation. X-ray diffraction is able to obtain atomic species concentration values through strain analysis. For the purposes of this work, both types of information are very valuable. The structural analysis techniques used in this work were primarily used to understand the strain evolution and monitor defect formation within HDSiP. These types of spatial and morphological information is then combined with electrical data and chemical analysis to yield a comprehensive view on the clustering configuration of dopants within HDSiP.

#### 2.7.1 High Resolution X-ray Diffraction

X-ray diffraction (XRD) experiments can be extremely useful for determining crystal structure and orientation of crystalline and polycrystalline species. To obtain crystal structure information from an unknown sample, a coupled scan is typically used. This is completed by changing the incident angle  $\omega$  of a coherent Cu k $\alpha$  x-ray source with respect to the sample while maintaining the same angle between the sample and the detector  $\omega = \theta$ . Data is analyzed by



Figure 2-15. When the conditions of Bragg's law are met, constructive interference between atomic planes with spacing d occurs. This manifests itself as a sharp peak of detected x-ray intensity.

applying Bragg's law (equation 2-47) to the constructive interference peaks of the XRD spectra to yield the d-spacing between atomic planes for a given incident beam angle which fulfills the Bragg condition,  $\theta_B$  (Figure 2-15). In this case, h, k and l are the Miller Indices of the respective lattice plane for which the Bragg condition is being met.[140]

$$n\lambda = 2\mathrm{d}sin(\theta_B) \tag{2-47}$$

$$d = \frac{a}{\sqrt{h^2 + k^2 + l^2}}$$
(2-48)

Much more in-depth analysis can be conducted on single crystalline samples with known -composition. These methods are of particular use for analysis of epitaxially grown thin films. Variations of XRD such as transverse scans and coupled scans can be conducted on epitaxially grown layers to obtain information about crystal quality, film thickness, strain, layer tilt and mosaic structure. For these studies, fine angular resolution is necessary to achieve detail in the resultant spectra. To obtain this level of detail on the arc second scale, high resolution XRD (HR-XRD) is employed. HR-XRD includes additional x-ray optics elements to condition the beam. Incident beam energy spread and collimation are controlled for using monochromators, Soller slits Goebel mirrors, and analyzer crystals to obtain <12 arcsec divergence.[141] Nickel can be used as a monochromator as it strongly absorbs copper  $K_{\beta}$  radiation. Specifically grown single crystals or sets of single crystals set up in their own Bragg condition can also be used. For strain analysis of the thin films used in this study two operating setups may be used: double axis diffractometry or triple axis diffractometry as seen below in Figure 2-16. A double axis transverse scan, or rocking curve, utilizes an open detector while the sample is tilted relative to the incident beam. This type of scan measures the diffuse scatter around a specific Bragg plane which is used as a baseline for angular measurements. Tilt magnitudes typically are  $\sim 1-2^{\circ}$  or up to 7200 arcseconds. Alternatively, for more precise measurements, a triple axis coupled scan can



Figure 2-16. Two different mechanisms of conducting strain analysis. (Top) in a double-axis transverse scan sample is tilted while detector is in the open position to maximize counts. (Bottom) in a triple-axis coupled scan additional beam conditioning optics are implemented in the reflected beam path to increase sensitivity for optimal strain analysis.

be used. This type of measurement, also called a longitudinal scan, places beam conditioning optics in the diffracted beam path as well as the incident beam path. A set of four symmetric or asymmetric Ge crystals as shown below can be used to decrease the allowed divergence angle of the diffracted beam to 35 arcsec and help absorb background radiation from the sample.

For data analysis, the derivative of Bragg's law can be used with an XRD rocking curve to measure the level of strain  $\epsilon$  in the film. In practice, experimental XRD strain data is analyzed by comparing the output plot to a simulation. However, it is important to understand the fundamental origins of these simulations. Strain in this case is defined as the deviation of thin film measured lattice parameter from the lattice parameter of the

$$\frac{d}{dd}(n\lambda) = \frac{d}{dd} \left( 2dsin(\theta_B) \right)$$
(2-49)

$$0 = 2\sin(\theta) + 2d\cos(\theta_B)\frac{d\theta}{dd}$$
(2-50)

$$\epsilon = \frac{d\mathbf{d}}{d} = -\cot(\theta_B) \,\mathrm{d}\theta \tag{2-51}$$

substrate.[141] The appearance of a broad peak to the right or left of the Bragg angle is indicative of a thin strained layer. Tensile strain will cause the broad peak to appear for greater measures of  $\theta$  (d $\theta$  is positive), where compressive strains will cause the broad peak to appear for smaller angles (d $\theta$  is negative). For silicon epitaxially grown films, this analysis is conducted on the (004) series of planes as this creates a non-zero value for the structure factor in a diamond cubic structure. With this strain measurement, compositional analysis of the thin film can be conducted using Vegard's law. For typical doping concentrations the effect of concentration on lattice parameter is close to linear. Dopant calibration factors,  $\beta$ , are used to convert strain measurements into dopant concentrations (N) or atomic percentages (at%). These values can be found in literature for select dopants in silicon.[141]

$$a_{A_{(1-x)}B_x} = (1-x)a_A + xa_B \tag{2-52}$$

$$N = -\frac{\epsilon}{\beta} \tag{2-53}$$

$$at\% = -\frac{\epsilon}{\beta N_{Si}} * 100 \tag{2-54}$$

For a strained layer, epitaxially grown layer thickness can also be easily determined through analysis of the HR-XRD spectra. For a high quality epitaxially grown film, on either side of the broad layer peak should exist a number of repeating satellite fringe peaks. The crystalline quality of the layer can be qualitatively related to the clarity of these fringes. The strained layer thickness can be determined through use of equation 2-55 where P<sub>1</sub> is the angular position of a fringe peak and P<sub>2</sub> is the angular position of the adjacent fringe peak. In this case,  $\theta_B$  for the substrate Bragg angle is used.[71]

$$t = \frac{\lambda}{(P_1 - P_2)\cos(\theta_B)}$$
(2-55)

### 2.7.2 Ellipsometry

Several of the processes which are conducted as a part of this project involve steps where it is desired to grow or limit the growth of oxide. In the case of oxidation studies, it is unnecessary and inefficient to image every particular sample in TEM to measure oxide thickness. For inert anneals even for short times it is extremely difficult to completely negate oxide growth and thus rather than neglect oxidation it is better to be able to monitor its progression. Ellipsometry represents an efficient method of determining oxide growth on silicon and HDSiP substrates.

Ellipsometry has many capabilities for thin film characterization, however for the purposes of this work it has been exclusively used to measure oxide thickness. It does this through comparing experimental intensity of polarized light with models. When linearly polarized light interacts with a sample surface, it becomes elliptically polarized and the phase and amplitude of the reflected light changes. These changes are compared to the polarization of the input rotating polarized light source to measure the complex reflectance ratio  $\rho$ . Defined as the ratio of p to s polarized light, this can be used to extract  $\Psi$  and  $\Delta$  parameters of the film.  $\tan(\Psi)$  corresponds to the amplitude ratio between the input and reflected signal, and  $\Delta$  corresponds to the resultant phase shift. These values are obtained as a function of wavelength and fit to a model of SiO<sub>2</sub> on Si to determine oxide thickness. [142], [143][144]

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$$\rho = \frac{r_p}{r_s} = \tan(\Psi) \exp(i\Delta)$$
(2-56)

As HDSiP possesses phosphorus concentrations of up to 9% and is a semiconductor alloy it cannot be assumed that the optical properties of HDSiP and Si are sufficient to be well suited for the SiO<sub>2</sub> on Si model. In addition, it is likely that despite the high segregation coefficient of phosphorus during thermal oxidation, the oxide that forms will still have a high concentration of phosphorus as well.[120], [145] To obtain the most accurate measurements of thermally grown oxide thickness on HDSiP, a new model would need to be made. However, XTEM



Figure 2-17. Experimental setup for conducting ellipsometry measurements. Light travels through a rotating polarizer, is incident upon the sample and then the reflected light which takes on an elliptical polarization is directed through another polarizer and measured with a detector.

measurements of several different thicknesses of oxidized HDSiP have been made in this work to

confirm that the SiO<sub>2</sub> / Si model still can give accurate measurements of oxide thickness.

### 2.7.3 Raman Spectrocopy

The scattering effects of a monochromatic light source as it interacts with a material can

give information about the vibrational states within the material. This effect was first described

by C. V. Raman and is the basis of Raman spectroscopy. When a photon with insufficient energy

to raise an electron to an electronic excited state scatters off an atom, this scattering event can be

broken down into a two-step mechanism. First, a photon with appropriate energy for interaction

with the atom must be intercepted by the scattering cross-section of the atom, exciting a bonding electron from its ground state into a higher energy "virtual state". From here, predominantly this electron will return to the same ground state from where it came and a photon of equal energy to the incident photon is emitted. This type of elastic scattering is called Rayleigh scattering, but is not the only mechanism for scattering to occur. Inelastic scattering or Raman scattering can also take place as a fraction of the excited electrons will either be excited from or relax into higher energy vibrational states. This is due to the interactions between the electric field of the incident laser and the polarizable nature of the material.[146]

For a given frequency of incident light  $v_0$ , the electric field of the electromagnetic wave can be expressed as an oscillating function (equation 2-57). The vibrations of the scattering atom can also be expressed similarly as changes in displacement from a center point,  $q_0$ , with frequency,  $v_m$  (equation 2-58).

$$E = E_0 \cos(2\pi v_0 t)$$
 (2-57)

$$q = q_0 \cos(2\pi \nu_m t) \tag{2-58}$$

The effect of this light on a semiconductor substrate is that polarization of the electron density of the material will occur. This polarization can be described as an electric dipole moment where  $\alpha$ 

$$P = \alpha E \tag{2-59}$$

is the polarizability of the material and is a function of displacement of the atomic nucleus, q.

$$\alpha = \alpha_0 + \left(\frac{\partial \alpha}{\partial q}\right)q\tag{2-60}$$

Taking into account these preceding relations, the electric dipole moment of the illuminated material can be expressed as equation 2-61 which can be expanded into equation 2-62.

$$P = \alpha_0 E_0 \cos(2\pi v_0 t) + \left(\frac{\partial \alpha}{\partial q}\right) E_0 q_0 \cos(2\pi v_0 t) \cos(2\pi v_m t)$$
(2-61)

$$P = \alpha_0 E_0 \cos(2\pi v_0 t) + \frac{1}{2} \left(\frac{\partial \alpha}{\partial q}\right) E_0 q_0 [\cos(2\pi (v_0 - v_m t) + \cos(2\pi (v_0 + v_m t))]$$
(2-62)

From this oscillating electric dipole moment, three different varieties of re-emitted light can be observed from the frequency of the incident light and the vibrational frequency of the absorbing species. The first term is the Rayleigh scattering, followed by the Raman scattering terms which can be separated into Stokes ( $v_0 - v_m$ ), and anti-Stokes ( $v_0 + v_m$ ).[146] These observed scattered frequencies are associated with the various vibrational ground energy states of the valence electrons that are being interacted with and can be seen in Figure 2-18. For analyzing a silicon sample, at room temperature a Raman shift ( $\Delta \omega$ ) typically reported in units of wavenumber can be observed at 520.7 cm<sup>-1</sup>. An anti-Stokes peak would also be observed at -520.7 cm<sup>-1</sup>, however, as the intensity of this peak is less than that of the Stokes it is customary to only report on the Stokes peak. Raman shift can be converted to the frequency,  $v_1$ , and wavelength,  $\lambda_1$ , of the Raman scattered light by equation 2-63. The energy,  $E_m$ , associated between vibrational states can be determined through equation 2-64.

$$\Delta\omega = \left(\frac{1}{\lambda_0} - \frac{1}{\lambda_1}\right) = \frac{(v_0 - v_1)}{c}$$
(2-63)

$$E_m = hc\Delta\omega \tag{2-64}$$

The interpretation of shifts in the Stokes Raman scattering peak can be somewhat difficult. It is important to select a laser wavelength for the incident light source that will be effective in probing the depths within a sample required for study. In this work, a 325 nm ultraviolet laser was used as this has an absorption depth of ~ 10 nm in silicon. For HDSiP samples, the doping concentration and the stress level are the factors that will predominate the Raman peak shift. For n-type dopants in silicon a linear dependence between active fraction of

dopants and Stokes peak values has been determined for dopant concentrations up to  $1.5 \times 10^{20}$  cm<sup>-3</sup>.[147][148]



Figure 2-18. Diagram showing the effect of different light-matter interactions on electron energy states. Raman spectroscopy incident light source is chosen such that the energy of the incoming light is insufficient to excite ground state electrons to electronic excited states.

Stress analysis can be conducted using Raman spectroscopy relating shifts in peak

position to uniaxial or biaxial stress in in the substrate. For a measurements taken using a

backscattered Raman system, uniaxial stress,  $\sigma$ , in Pascals in the [001] crystal direction can be

related to Raman shift peak position by equation 2-65. Biaxial stress with components  $\sigma_{xx}$  and

 $\sigma_{yy}$  can be predicted through using equation 2-66.[149]

$$\Delta\omega = -2x10^{-9}\sigma \tag{2-65}$$

$$\Delta\omega = -4x10^{-9} \left(\frac{\sigma_{xx} + \sigma_{yy}}{2}\right) \tag{2-66}$$

## 2.7.4 Transmission Electron Microscopy

As the microstructural features of interest in this work are smaller than 100 nm, this precludes their observation using optical microscopes due to the resolution limit of the visible light spectrum. To circumvent this issue, an electron beam can be used as an imaging probe to resolve nanoscale features as the wavelength of an electron can be as small as 2.7 pm when accelerated at 200kV. This beam can be directed through a sufficiently thin (electron transparent) section of sample in order to create a 2-dimensional projection of 3-dimensional thin sample.[136] As the microstructural elements of interest in this work consist of defects present within the bulk crystal as opposed to on the surface of the sample, transmission electron microscopy is the most efficient method for imaging these features.

Two different methods can be used to obtain transmission micrographs with useful information on the specimen. The first involves looking through a sample with the beam orthogonal to the thin film, termed plan-view TEM (PTEM) and the second involves looking through a sample in cross-section (XTEM) such that the beam direction is in plane with the thin film. These two imaging methods require very different sample preparation techniques. For PTEM samples, a thin cylindrical section of wafer (3.5mm diameter, 675 µm thickness) is cut from the (001) silicon wafer. This section is then thinned down to ~50 µm thickness through mechanical polishing from the wafer backside. Next, the sample is covered with wax to protect it from wet chemical etching excluding a pinhole sized area in the center. The sample is then exposed to a 1:3 HF:HNO<sub>3</sub> wet chemical etch until light can be transmitted through the etch pit indicating that the etch has progressed through the entirety of the sample. A diagram of how this process is conducted can be seen in Figure 2-19. Once finished, a 4-step solvent rinse is used to dissolve any excess wax and ensure a clean surface for imaging.



Figure 2-19. In PTEM sample preparation, a thin disk of the silicon wafer with the layer of interest facing down is covered with protective wax. This sample is exposed to an acid etch of HF:HNO3 until the sample has been etched through the entire thickness. Imaging is conducted on the edges of this etch pit where the sample contains the region of interest and is electron transparent.

The XTEM sample preparation process involves extensive use of a focused ion beam

lithography (FIB) tool in a dual beam arrangement with a scanning electron microscope (SEM). Prior to placing the sample into the FIB vacuum chamber, a carbon based protective coating is applied to temporarily protect the sample surface from ion beam damage before a more permanent platinum layer may be deposited with the ion beam as shown in Figure 2-20. The FIB is used to cut into the top wafer surface such that a section of the bulk silicon containing the thin film of interest can be removed from the wafer entirely using a micromanipulator. Once removed from the wafer surface, the lamella is mounted to a molybdenum TEM grid post where it is sequentially thinned with the FIB using decreasing ion beam voltages until it is <100nm thick. This enables imaging of the cross-section of the thin films studied in this work. The procedure used for this thinning is roughly as outlined in the work by Schaffer et al.[150]



Figure 2-20. brief sample preparation procedure for a XTEM sample. After mounting to a molybdenum TEM grid, sample is thinned using the ion beam until it is less than 100 nm thick.

## 2.7.4.1 High resolution transmission electron microscopy

The goal of High Resolution TEM (HR-TEM) is to maximize detail in the image while still preserving as much signal as possible. This is done by selecting only low spatial frequency rays of electrons from the diffraction pattern (DP) without including contributions to image signal from high spatial frequency rays. High spatial frequency rays of electrons will have experienced more spherical aberration due to having traveled larger distances from the optic axis which results in a distorted image. The objective aperture can be used to filter these contributions and only allow the innermost spots on the DP surrounding the direct beam to generate the image.
By doing this, image detail can be maximized and clear interpretation of the micrographs can be conducted.

#### 2.7.4.2 Annular dark field scanning transmission electron microcopy

In some cases, it can be of interest to generate an extremely high-resolution image by converging the beam on the sample rather than having a parallel beam condition impinging upon the sample. This beam can then be used to conduct analytical studies of the chemistry of certain specified areas or it can be used to scan across the sample generating an image. A scanning TEM (STEM) micrograph results as the beam is rastered across the sample area and the intensity of the transmitted electrons is monitored by a detector. This intensity combined with the original beam location can be converted to an x-y position to form the image. For the purposes of this work, an annular detector is employed to measure the intensity of electrons which are highly scattered by the material. This technique is called annular dark field STEM (ADF-STEM) as elements of the sample which diffract electrons more will appear bright on the micrograph. By changing the distance between the sample and the annular detector, the inner collection angle can be changed and the contributions to the measured intensity can be biased toward higher or lower spatial frequency electrons. By moving the detector close to the sample, a large collection angle is achieved and the conditions for high-angle annular dark field STEM (HAADF-STEM) can be met.

## 2.7.5 Rutherford Backscattering Spectroscopy

Similar to Dynamic SIMS, Rutherford Backscattering Spectroscopy (RBS) can yield important information about the chemical composition of thin film crystalline layers. Without requiring standards, RBS obtains information about the chemical species present as well as the depth by accelerating 1-2 MeV alpha (He<sup>2+</sup>) particles at an angle to the wafer surface. Collisions with atomic nuclei in the crystal result in some of the alpha particles being backscattered rather than implanting into the material. The energy of the backscattered alpha particles reveals the mass of the scattering nuclei through a kinematic scattering factor (equation 2-67). In this equation, M is the mass of the target nucleus, m is the mass of the alpha particle and  $\theta$  is the scattering angle. Using this information, the energy of the scattered alpha particle can be related to incident atomic species as well as the depth of the scattering atom from the surface.

$$K_M = \frac{E_M}{E} = \left(\frac{\sqrt{M^2 - m^2 \sin(\theta)} + m\cos(\theta)}{M + m}\right)^2$$
(2-67)

Structural information can be obtained with RBS by aligning the primary beam of alpha particles with a low-density crystal plane. This exposes the crystalline channels to the alpha particles and dramatically decreases the probability of interaction with any but the surface layer of atoms. In this type of study, a comparison of two materials can qualitatively yield information about increases or decreases in the concentration of interstitial species. It should be noted that variations in the distribution of interstitial species can cause changes in the backscattered yield as well as concentration changes.

### 2.8 Marker Layer Diffusion Analysis

Analysis of the diffusion of grown-in buried marker layers constitutes an important method which can be used to learn about dopant behavior in crystalline solids. Using a buried marker layer as a detector of point defect flux and has been well documented in the literature by the like of P.A. Stolk, H.J. Gossmann and K.S. Jones as well as various others.[95], [151]–[155], [155] This method is used to understand dopant diffusion mechanisms as well as to quantify point defect flux through the marker layer. Knowledge of this point defect flux can be important to determine initial point defect concentrations in the material. To properly conduct a marker layer diffusion analysis study, special wafer samples need to be prepared. Typically, from the surface of a nominally undoped wafer, a certain thickness of undoped silicon is grown via CVD or molecular beam epitaxy (MBE). This is to provide a buffer layer from the starting growth interface in which the marker layer can diffuse. From this point, a thin layer of moderately doped silicon is grown. This constitutes the buried marker layer. Next, another layer of undoped silicon is grown on top of this marker layer to provide a buffer layer on the top side of the sample for the marker layer to diffuse. For a control sample, this completes the growth process. For a non-control sample, the epitaxially grown layer of interest is grown on top of this undoped silicon layer. Diagrams of these superlattices can be seen in Figure 2-1. For implant studies, the ion implant projected range would be such that it is a significantly shallower than the buried marker layer depth.[156]

The theory for marker layer diffusion analysis stems from the fundamental view of atomistic diffusion in crystalline solids. The diffusivity of a species in a crystal is determined by the linear combination of diffusivity contributions through vacancy mediated mechanisms and interstitial mediated mechanisms. Most dopant species in silicon diffuse through both

$$D = \frac{f_I D_I C_I}{C_I^*} + \frac{(1 - f_I) D_V C_V}{C_V^*}$$
(2-68)

mechanisms to some degree and the coefficient of fractional diffusivity can differ based on the conditions (e.g. temperature) where the dopant is diffusing. For point defect injection analysis, marker layers are typically constructed using antimony (pure vacancy diffuser in silicon) or phosphorus (pure interstitial diffuser in silicon at low concentrations) as the marker layer dopant species. Boron marker layers have also been frequently used to model interstitial flux as boron diffusion is more easily modeled compared to phosphorus and also primarily diffuses interstitial means.

### 2.8.1 Interpretation of Results

For the purposes of this work, marker layer diffusion analysis was used to quantify injection of point defects by HDSiP during annealing. As the diffusivity of point defects in silicon is several orders of magnitude higher than that for dopants, any point defects released by the layer will flow through the buried marker layer despite it being 150 nm deep within the bulk crystal. These point defects can be quantified by measuring diffusivity enhancements or retardations of the marker layer sample with the HDSiP layer on the surface compared to a control. As a phosphorus marker layer was used for these experiments, diffusion enhancement is indicative of interstitial injection by the layer, where diffusion retardation would suggest vacancy injection. The degree of enhancement can be determined through use of diffusion simulation tools such as the Florida Object Oriented Process Simulator (FLOOPS). Diffusivity enhancements of a phosphorus marker layer can be correlated to increased concentrations of interstitials within the marker layer. The concentration of interstitials can be determined through use of the following equation 2-68. D<sub>P</sub> and D<sub>P</sub>\* are obtained through simulation analysis of

$$\frac{D_P}{D_P^*} = \frac{C_I}{C_I^*}$$
(2-69)

SIMS data and are the marker layer diffusivity for the sample containing HDSiP on the surface and for the control samples respectively. They can be related to the concentration of interstitials present in the marker layer for the HDSiP sample and the control respectively as phosphorus is a purely interstitial diffuser. This information can then be used to understand point defect injection by the HDSiP layer.

## 2.8.2 Florida Object Oriented Process Simulator

The FLorida Object Oriented Process Simulator (FLOOPS) software is a very useful tool for predictive modeling of processes in semiconductors. FLOOPS has the ability to predict behavior of dopants, clusters and point defect species in semiconductors through a wide range of relevant processing steps such as ion implantation, thermal oxidation, inert annealing, deposition and etching. For the purposes of this work, the FLOOPS software has been used to model data obtained from SIMS analysis to determine diffusivity values. Phosphorus diffusivity values from both the HDSiP layer as well as the buried phosphorus marker layer are obtained using the FLOOPS software. FLOOPS acquires these values through solving partial differential equations using finite element analysis techniques. A constant time averaged diffusivity is assumed for the cases here and checked against the plotted diffused profile. This process is iterated until a satisfactory fit is converged upon. This diffusivity value, D, is used in the following equation 2-69 to produce a gaussian diffusion profile maintaining a constant

$$\frac{\partial C_P}{\partial t} = \nabla \cdot \left( D * \nabla (C_P) \right) \tag{2-70}$$

integrated dose as would be expected for the epitaxially grown layers within this work. Here, C<sub>P</sub> refers to the concentration of mobile phosphorus within the matrix.

As mentioned in section 1.4.5, phosphorus diffusion is a complex, multicomponent phenomenon which can be very challenging to model. At low concentrations below the kink in the diffusion profile, phosphorus diffuses very rapidly through a purely interstitialcy mechanism. At higher concentrations above the kink in the diffusion profile, phosphorus diffuses through a predominantly vacancy mediated mechanism. To model this behavior, a truncation method is employed. Given two SIMS plots before and after an anneal which have already been normalized for dose and shifted for marker layer peak position, the annealed profile is truncated at the kink concentration as shown in Figure 2-21. The integrated dose of the truncated profile is then calculated for the depth range in consideration. Next, the profile for the sample before the anneal is taken over the same depth range and the marker layer peak is truncated to obtain the same integrated dose. These two truncated profiles are then incorporated into the FLOOPS software and by doing this only the contributions to diffusion of the tail which have diffused through interstitialcy means are factoring into the diffusivity value obtained. For some select samples, the



Figure 2-21. Experimental data obtained for a marker layer sample showing diffusion after an anneal (right). Truncation of before and after data sets to account for only the tail diffusion of phosphorus and FLOOPS simulated tail diffusion profile. (left)

amount of interstitialcy diffusion can only be observed on one side of the marker layer sample due to the broad decline of the marker layer on the other side of the sample as can be seen on the left side of the plot in Figure 2-22. For these cases, one directional diffusion was modeled by selecting the depth range studied to start at the peak of the original marker layer. Using these methods, marker layer diffusion can be modeled and diffusivity values for phosphorus diffusion can be obtained.



Figure 2-22. For marker layer samples that have a broad post marker layer concentration decline, one directional diffusion analysis is required to extract diffusivity values for short time anneals.

## CHAPTER 3 STABILITY OF ACTIVATED HDSIP

#### **3.1 Background and Purpose**

Prior to incorporation of the selective epitaxy process used to create HDSiP into transistor fabrication process flow, it is important that the bigger picture be considered. There are several strengths of using in-situ doped HDSiP over Si:CP or Si:C doped with ion implant. As an in-situ doping method, steep dopant concentration profile cutoffs can be established. With HDSiP, the phosphorus dopant atoms do not need to compete with carbon for substitutional lattice sites, thus lower resistivity source/drain regions can be attained. Finally, record low contact resistances have been obtained with HDSiP, ultimately allowing for higher performance transistors.

With all this considered, there is still the issue of stability. HDSiP is a material created in a far from equilibrium growth process. In this process, higher than solid solubility limit levels of phosphorus can be incorporated into epitaxially grown films. As this is not an equilibrium state for the material system, it is important to probe the stability of these superior properties. The laser DSA process which has been reported to efficiently activate dopants leads to another metastable state with active dopant concentrations reported as high as  $\sim 1 \times 10^{21}$  cm<sup>-3</sup>. This value is far higher than what has been reported previously for conventional phosphorus doped silicon when only non-melt techniques are employed. At the start of this work, it was unknown as to the stability of these electrical properties and strain of HDSiP after laser DSA.

For the successful incorporation of HDSiP into transistor process flow, it is important to have a fundamental understanding of its behavior after post DSA thermal processing. nMOS selective epitaxial growth typically takes place after pMOS SiGe:B RSD epitaxial growth. Following the growth of pMOS SiGe:B, pMOS areas are masked, nMOS source and drain areas

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are opened up, HDSiP is grown, and then an activating DSA is completed to attain desired low contact resistance of the HDSiP. Following this step, a metal layer is deposited on the source/drain regions and a silicidation reaction takes place. Silicidation requires annealing the wafer again at a temperature dependent on the type of silicide being formed. For TiSi formation, temperatures up to 800 °C can be used.[30] It is important to understand how the post DSA activated HDSiP properties will be affected by this and other subsequent thermal anneals. Focuses of this study will be on electrical properties, strain as well as microstructural stability after DSA annealing and subsequent thermal annealing.

#### **3.2 Experimental Methods**

HDSiP films were grown several tens of nanometers thick onto nominally p-type 300 mm silicon (001) wafers. This growth process was conducted in a horizontal RP-CVD reactor. Precursor gasses used were dichlorosilane and phosphine gas with precursor partial pressures dependent on the desired film concentration. Upon receiving sample wafers, four-point probe resistivity maps were created to determine resistivity uniformity with respect to position on the wafers. For samples exposed to the ms laser DSA, sections of wafer were cleaved and annealed using Applied Materials Vantage® Astra<sup>TM</sup> DSA system. This system uses a continuous wave laser which rasters over the sample surface resulting in a total exposure time of 0.25 ms.

Prior to electrical measurements with the Hall-effect system, wafer coupons with dimensions 10 mm x 10 mm were cleaved from the substrate. Coupons were prepared by etching the native oxide from the surface with dilute HF followed by a standard 3-step solvent rinse to remove any surface contamination. Indium metal was used to form ohmic contacts in the corners of each sample in van-der Pauw geometry as described in section 2.5.2. For obtaining anneal time series electrical measurements, a single sample coupon was used to obtain data for each time point for the given temperature. Rather than use a different section of wafer annealed at

each desired time, one wafer was annealed, measured, then re-annealed to produce the electrical data as a function of total time annealed. This was done to eliminate error based on HDSiP layer thickness and resistivity nonuniformities on the wafer. Prior to each anneal, pressed on indium metal contacts were removed.

Dynamic SIMS studies were performed at Evans Analytical utilizing a Cs<sup>+</sup> primary ion beam. HR-XRD analysis was performed using a triple axis coupled scan of the substrate (004) Bragg reflection. X-TEM micrographs were obtained using a Tecnai F20 microscope with samples prepared on a Helios dual beam FIB lithography tool as discussed in section 2.7.4

### **3.3 Experimental Results**

### **3.3.1 DSA Activation of HDSiP**

A millesecond laser dynamic surface anneal (DSA) has been used extensively within this work. Prior literature has reported that effective resistivity decreases can be achieved for HDSiP with the DSA using correlated sample surface temperatures ranging from 1150 °C to 1200 °C. At the time of this work, no Hall-effect measurements of active carrier concentration had been conducted on these films post anneal. Therefore, in order to establish a baseline for the activation levels attainable with the DSA, a Hall-effect study of activation with respect to laser anneal temperature has been conducted.

This study confirms the trends in literature that had been established for a  $1.9 \times 10^{21}$  cm<sup>-3</sup> P sample of HDSiP. It was assumed that no change in layer junction depth occurred during the DSA anneal at these temperatures as observed by Li et al. and Ye et al.[2][5] Sheet number values have been converted to carrier concentrations by dividing by the layer thickness which was attained through HR-XRD measurements. Activation of phosphorus dopant species up to  $-9 \times 10^{20}$  cm<sup>-3</sup> P can be observed after ms laser DSA at 1200 °C. A trade-off occurs during this activation process however as with increasing activation a corresponding decrease in the carrier

mobility can be observed (Figure 3-1). This effect is due to increased ionized impurity scattering within the HDSiP layer. Despite this decrease in carrier mobility, a decreased sheet resistance of the HDSiP layer was observed for laser anneal temperatures of 1150 °C and 1200 °C. The effect of phosphorus concentration on electrical properties after a laser DSA has been studied for 1200 °C DSA and will be discussed in section 5.3.



Figure 3-1. Hall effect derived values for sheet resistance, active carrier concentration and electron mobility for thin film HDSiP samples. Through this data it can be observed that DSA temperatures above 1150 °C achieve significant activation.

# 3.3.2 Diffusion During Post DSA Secondary Annealing

The stability of HDSiP has been studied with regards to electrical dopant activation level. In order to obtain reliable measures of carrier concentration within a thin film sample, an accurate measure of junction depth is required. The samples here were exposed to a ms laser DSA followed by an RTA, therefore knowledge about the effects of these anneals on junction depth is required. Dynamic SIMS measurements were used to determine the degree of diffusion with respect to the anneal times considered within this work.

For the 2x10<sup>21</sup> cm<sup>-3</sup> P HDSiP samples, no observable diffusion took place after the 1200

°C DSA during which substantial activation of dopants was attained (Figure 3-2). For a sample

which was annealed for up to 2 minutes at 700 °C using the RTA, negligible diffusion in

comparison to the total layer active dose was observed. With these observations, the sheet number values in the following section obtained through Hall-effect measurements can be directly correlated with the constant layer thickness to obtain carrier concentration values. For samples that underwent secondary annealing at temperatures higher than 700 °C, shorter anneal times were used. Diffusion time tag calculations using standard values of phosphorus diffusivity were conducted with these shorter



Figure 3-2. Dynamic SIMS was used to monitor diffusion of the HDSiP layer during anneal times used for the stability studies.

anneal times to predict diffusion lengths for these annealing conditions. Times were chosen such that the predicted diffusion lengths stayed below what was predicted for a 700 °C 2 minute anneal as those conditions demonstrated negligible diffusion. This was done as it is beyond the scope of available resources to conduct SIMS analysis on every sample studied with Hall-effect.

### 3.3.3 Stability of Activated HDSiP During Post DSA Secondary Annealing

Dopant stability experiments were undertaken by exposing samples of HDSiP to the ms laser DSA to activate dopants followed by a secondary RTA between 600 °C and 900 °C to study thermal stability. The temperatures and times chosen for this study were roughly representative of a silicidation process typically used for contact formation. HDSiP epitaxially grown layers were shown to exhibit negligible diffusion for anneals up to 30 minutes at 700 °C as can be seen in Figure 3-2, and thus changes in active dopant concentration in this study cannot be attributed to an increasing junction depth. Calculations using P diffusivity values from literature suggest that the higher temperature and time annealing conditions used in this study would exhibit similarly insignificant diffusion. By monitoring the sheet number determined by Hall-effect and taking a layer thickness value from SIMS, active carrier concentration values can be compared. It was found that both  $5 \times 10^{20}$  cm<sup>-3</sup> P LDSiP and  $2 \times 10^{21}$  cm<sup>-3</sup> P HDSiP layers readily deactivate after a period of seconds to minutes at temperatures above 600 °C. Figure 3-3 shows the observed deactivation characteristics of HDSiP as a function of temperature and time. A similar series of curves was created for the LDSiP which can be seen in Figure 3-4. Figure 3-5 compares the stability of HDSiP layers to LDSiP layers activated by DSA and subsequently annealed at 700 °C. For HDSiP, dopants were found to deactivate back to as-grown levels after 60 s at 700 °C. LDSiP maintains its enhanced electrical properties for a significantly longer anneal duration. The deactivation kinetics for both HDSiP and LDSiP followed an exponential decay relationship and were fit accordingly to equation 3-1.

$$n = y_0 + Aexp(-kt) \tag{3-1}$$

From this relation, a rate constant k was obtained for each post DSA annealing temperature. These rate constants were then plotted versus inverse temperature following the Arrhenius relation for temperature dependence as seen in Figure 3-6. An activation energy for the deactivation process was calculated from the slope of the Arrhenius plot to be 2.1 eV for LDSiP. The activation energy for HDSiP, however, was lower, around 1.3 eV. This indicates a possible shift in the mechanism for deactivation as a function of dopant concentration.



Figure 3-3. Deactivation behavior of DSA annealed HDSiP after a secondary RTA. Hall-effect carrier concentration evolution is shown as a function of RTA time and temperature. As-grown concentration levels can be observed after 60s at 700 °C.



Figure 3-4. Deactivation behavior of DSA annealed LDSiP after a secondary RTA. Hall-effect carrier concentration evolution is shown as a function of RTA time and temperature.



Figure 3-5. Comparison of deactivation behavior of HDSiP and LDSiP annealed with a ms laser DSA. Hall-effect carrier concentration is plotted as a function of secondary RTA time at 700 °C.



Figure 3-6. Arrhenius plot showing the temperature dependence of the deactivation process. Activation energy values for deactivation can be obtained through calculating the slope of a best fit line. Activation energy values of 1.3 and 2.1 eV were obtained for LDSiP and HDSiP respectively

### **3.3.4 Reversibility of Activation**

The previous section outlines how the state of dopants in HDSiP and LDSiP evolves with respect to the DSA and secondary thermal anneals. In the as-grown state, approximately  $2x10^{20}$  cm<sup>-3</sup> phosphorus atoms occupy substitutional lattice sites and the remaining phosphorus exists in inactive clusters. After the DSA, activation occurs and a fraction of these clusters breakup to yield an increase in the concentration of substitutional phosphorus in the film. During the deactivation observed during secondary thermal annealing of DSA exposed HDSiP, these additional substitutional phosphorus atoms are forming into clusters again. Whether the inactive clusters that are grown into the film are the same type of clusters that are formed during deactivation was unknown.

It is important to understand whether the HDSiP film reverts from the activated "DSA state" back to the "as-grown state" during secondary annealing or if the secondary anneal

produces a third state which has a different variety of clusters. Analytical methods of probing the various states of HDSiP are discussed in Chapter 4, however a practical method of studying this question can be found by examining the impacts of DSA annealing on the deactivated films.

To understand the effects of DSA annealing, a series of anneals were conducted on a  $1.6 \times 10^{21}$  cm<sup>-3</sup> P HDSiP wafer. Samples were exposed to a 0.25 ms DSA at various temperatures and hall effect measurements were taken. The samples were then exposed to a 900 °C spike anneal where deactivation of the laser annealed films was observed in agreement with the results in section 3.3.3. Following this, the samples were re-exposed to the DSA again with the same conditions as the first exposure. Hall-effect measurements of these samples were taken and shown in Figure 3-7.

At 1100 °C the DSA is seen to have little effect on the sheet resistance of HDSiP compared to the as-grown sample. For this particular sample the RTA effectively activated the film to a small degree. At 1150 °C the deactivating effects of the RTA were minimal as the activation level of the film has not been saturated by the DSA. What can be seen in Figure 3-7 is that at high temperatures, the second DSA exposure is able to restore the electrical properties which were lost during the deactivating spike anneal. This is an indicator that the DSA has similar activating effects when the HDSiP has already been deactivated. Deactivation with the spike anneal returns the state of HDSiP to that of the as-grown film rather than creating a new state with a different type of clusters. It is suggested that the deactivation reaction during DSA.



Figure 3-7. Hall effect measurement data for a  $1.6 \times 10^{21}$  cm<sup>-3</sup> P HDSiP sample exposed to a series of anneals. Effective activation can be obtained through DSA annealing at temperatures of 1150 °C and above. Deactivation occurs during secondary spike annealing which shows marginal activation for samples not exposed to the primary DSA anneal. A second DSA following the spike anneal restores electrical properties to similar values as after the first DSA.

# 3.3.5 Strain Stability of HDSiP During Post DSA Secondary Annealing

I. De Wolf outlined a method of using Raman spectroscopy as a way of determining

biaxial film strain in a silicon sample.[149] This method has been applied here to HDSiP as an

attempt to use Raman as an alternative to HR-XRD to measure strain changes within the film. As was expected, negative shifts from the control silicon peak at 520.7 cm<sup>-1</sup> were observed for all samples of  $2x10^{21}$  cm<sup>-3</sup> P indicating tensile strain (Figure 3-8). In Raman, a negative peak shift is indicative of tensile strain in the film, however doping also produces an effect on peak shift as well which needs to be parsed out.



Figure 3-8. Raman scattered peak for  $2x10^{21}$  cm<sup>-3</sup> P HDSiP after exposure to various activating and deactivating anneals. Control silicon Raman peak shift is 520.7 cm<sup>-1</sup>.

In addition to strain, two additional impacts of doping silicon can manifest as Raman peak shifts. First, the difference in mass can have an effect on the phonon vibrational modes within the solid. For phosphorus doping of silicon, this effect was mathematically predicted as well as experimentally shown to be negligible due to similarities in mass. The second impact of dopant species is due to the electronic effects of higher active carrier concentration on the polarizability of the material. This effect was measured as a function of carrier concentration by F. Cerdeira et al. and has been replicated below as equation 3-2.[147] It should be noted that this relation was experimentally derived and possesses a large degree of variance. When applying

$$\Delta\omega = (4.7 \pm 1.6) * 10^{-21} n \tag{3-2}$$

this equation 3-2 with the relation between Raman peak shift and biaxial stress from De Wolf, one obtains the following equation 3-6.

$$\Delta\omega = -4 * 10^9 \left(\frac{\sigma_{xx} + \sigma_{yy}}{2}\right) \tag{3-3}$$

$$\sigma = \sigma_{xx} = \sigma_{yy} \tag{3-4}$$

$$\Delta\omega = -4 * 10^9 \sigma \tag{3-5}$$

$$\Delta a_0 = 0.0174 * \left( \Delta \omega - (4.7 * 10^{-21} n) \right)$$
(3-6)

Once these relations have been applied to the peak positions from Figure 3-8 defined with a Voight function, the strain values as reported in table 3-1 are obtained. However, once these values of lattice contraction are compared with those obtained through XRD, it can be seen that Raman spectroscopy is not a valid method of determining HDSiP layer strain evolution. Too many additional factors which cannot be controlled for contribute to peak position shifts in Raman spectroscopy. Given this, the strain of the layer cannot be accurately predicted with Raman, and HR-XRD measurements should be relied on exclusively.

Table 3-1. Values for measured strain in HDSiP layer in terms of lattice parameter contraction through Raman spectroscopy and HR-XRD with respect to annealing conditions of  $2x10^{21}$  cm<sup>-3</sup> P HDSiP sample.

Annealing conditions	Measured $\Delta \omega$ (cm <sup>-1</sup> )	Raman $\Delta a_0$ (Å)	HR-XRD ∆a <sub>0</sub> (Å)
As-grown	2.4	0.021	0.018
1200 °C DSA	4.1	0.027	0.018
1200°C DSA + 2m 700°C	2.9	0.030	0.018
1200°C DSA + 30m 700 °C	1.7	0.0092	N/A
1200 °C DSA + 4h 700 °C	1.5	0.0057	0.017

HR-XRD is the standard method of determining thin film layer strain. Coupled-scans of

the (004) Bragg reflection were conducted for an anneal series of a  $2x10^{21}$  cm<sup>-3</sup> P HDSiP film.

As can be observed in Figure 3-9, strain remained nominally unchanged after the ms DSA where activation of the layer occurs. After DSA followed by a 700 °C inert deactivating anneal for 2 minutes, no strain degradation can be observed. Despite significant changes in active carrier concentration  $(2.5 \times 10^{20} \text{ cm}^{-3} \text{ to } 5.5 \times 10^{20} \text{ cm}^{-3} \text{ and back to } 2.5 \times 10^{20} \text{ cm}^{-3})$  no strain loss occurs. This suggests that complexes responsible for strain in the HDSiP layers do not participate in activating or deactivating reactions. After a 4 hour inert secondary anneal where diffusion of the HDSiP layer occurs, strain loss can be observed. This indicates the stability of tensile strain during thermal annealing processes that would be used for transistor fabrication.



Figure 3-9. HR-XRD of 2x10<sup>21</sup> cm<sup>-3</sup> P HDSiP sample during activating DSA (1200 °C), deactivating secondary anneal (2m, 700 °C) and where diffusion of HDSiP layer is observed (4h 700 °C)

# 3.3.6 Microstructure Stability of HDSiP During Post DSA Secondary Annealing

During deactivation of HDSiP it was possible that precipitation was occurring as the phosphorus concentration is higher than where precipitation has been previously observed.[66], [117] To study this further, microstructural analysis of HDSiP films was conducted. In Figure 3-

10, HR-TEM images of the  $2x10^{21}$  cm<sup>-3</sup> P samples show a lack extended defects or precipitation throughout DSA and deactivating secondary anneal. Despite significant increases in active P level after DSA and significant deactivation following a secondary RTA at 700 °C for 2 minutes, no change in crystal quality was observed. This is confirmed by the presence of well-defined satellite fringes to the HDSiP strained layer peak in the HR-XRD spectrum (Figure 3-9).



Figure 3-10. Cross-sectional TEM micrographs of (a) as-grown 2x10<sup>21</sup> cm<sup>-3</sup> P HDSiP (b) post 1200 °C DSA 2x10<sup>21</sup> cm<sup>-3</sup> P HDSiP and (c) 2x10<sup>21</sup> cm<sup>-3</sup> P HDSiP exposed to 1200 °C DSA followed by 2m 700 °C RTA. A defect free layer is observed in all cases. Epitaxial layer interface is marked by the arrow.

# 3.3.7 Rutherford Backscattering Spectroscopy

Rutherford backscattering spectroscopy was used to qualitatively characterize changes in the interstitial population of HDSiP layers after DSA annealing and secondary thermal treatment. The work of Dhayalan et al. concluded that an increase in the concentration of phosphorus on interstitial sites resulted after ms laser annealing.[79] However this conclusion was based off of excessively noisy data with relatively few counts. With RBS, alpha particles that scatter off of a phosphorus nucleus may have a slightly higher measured energy. This can be seen in the small tail of the plot in Figure 3-11. Similar RBS analysis to what was conducted by Dhayalan et al is shown in Figures 3-12, 3-13 and 3-14. As in the previous study, no clear results were able to be obtained as the signal to noise ratio for these plots was also too low.



Figure 3-11. RBS spectra for HDSiP showing a small tail region from 375-400 channel numbers which corresponds to the signal from phosphorus. The black curve is for a randomly oriented incident beam, the red curve corresponds to the aligned beam condition.



Figure 3-12. RBS spectra of the phosphorus region of as-grown HDSiP. Randomly oriented sample (left) and aligned sample (right) The aligned sample counts are 15.7% of the random sample counts.



Figure 3-13. RBS spectra of the phosphorus region of DSA annealed HDSiP. Randomly oriented sample (left) and aligned sample (right) The aligned sample counts are 11.5% of the random sample counts.



Figure 3-14. RBS spectra of the phosphorus region of HDSiP exposed to 1200 °C DSA followed by 30m 700 °C thermal anneal. Randomly oriented sample (left) and aligned sample (right) The aligned sample counts are 10.2% of the random sample counts.

# **3.4 Discussion and Conclusions**

### **3.4.1 Discussion of Experimental Results**

The activation energy for deactivation observed in this study for HDSiP is relatively low compared to many processes that involve the motion of a substitutional atom escaping from its lattice site.[85], [93], [94] Taking this into account, two possible mechanisms are considered. The first mechanism involves the breakup and reforming of vacancy clusters. This type of mechanism has been proposed in the literature to be responsible for ms laser activation of HDSiP.[67], [79] For this mechanism, P<sub>4</sub>V clusters fully or partially dissociate during laser annealing. Deactivation would proceed via the reverse reaction as no precipitation is observed in TEM. Physical mechanisms for P<sub>4</sub>V dissociation during activation would require that outside point defects mediate the reaction. Due to how P diffuses via an interstitialcy mechanism it is probable that P<sub>4</sub>V dissolution would be an interstitial mediated process.[85], [93], [94] At high temperature, a free interstitial recombines with the central vacancy of a P<sub>4</sub>V cluster causing a

reduction in the vacancy population as seen by Dhayalan et al.[79]The resulting cluster would resemble a zincblende Si-P compound which will be termed a P<sub>4</sub> substitutional cluster (Figure 3-15). A second interstitial would be required to disassociate a phosphorus atom from the P<sub>4</sub> substitutional cluster causing activation of the dissociated phosphorus atom. Deactivation would follow by reforming phosphorus substitutional clusters, where the limiting step is interstitialcy diffusion to form P<sub>4</sub> substitutional clusters. The exact mechanism and driving force for this process is not known. Frenkel pair formation within a P<sub>4</sub> cluster would be spontaneous due to the energetic favorability of P<sub>4</sub>V predicted with DFT.[51]–[54], [78]



Figure 3-15. Schematic representation of a theoretical filled in P<sub>4</sub> substitutional cluster, the result of the reaction between a self-interstitial and a P<sub>4</sub>V complex.

A second deactivation mechanism proposed here does not require the activation of phosphorus from P<sub>4</sub>V clusters and can be consistent with the theory that P<sub>4</sub>V clusters are necessary to explain the high layer tensile strain. It is proposed that phosphorus-interstitial clusters (PICs) are grown into the HDSiP layer existing concurrently with P<sub>4</sub>V clusters. PICs have been previously reported in the work of Keys et al.[98], [99] Dissolution of PICs during the ms anneal creates substitutional phosphorus and self-interstitials that form into self-interstitial clusters or fill in the vacancy of  $P_4V$  clusters. The reverse then takes place during secondary thermal treatment as free interstitials combine with substitutional phosphorus preventing electron donation. Free interstitials causing deactivation could either be from self-interstitial clusters or spontaneous Frenkel pair formation within a  $P_4$  cluster forming a  $P_4V$ . The equilibrium between these types of clusters that exists in the as-grown state is reestablished after sufficient time of secondary annealing. It should be mentioned that this mechanism and the previously discussed  $P_4V$  dissolution mechanism involve a high concentration of interstitials. The effects of these interstitials on strain is not well understood.

For the  $5x10^{20}$  cm<sup>-3</sup> P LDSiP sample, more possibilities exist for deactivation mechanisms. Activation and deactivation of LDSiP may stem interstitial mediated mechanisms similar to HDSiP. However, given that a higher activation energy of 2.1 eV was observed for deactivation of LDSiP, it is suggested that the concentration of interstitials present in the LDSiP layer during deactivation has substantially decreased. This is demonstrated experimentally in section 5.3.5. As LDSiP has a significantly lower concentration of vacancy clusters, it can be theorized that a higher concentration of free interstitials diffuse into the bulk before reacting with a vacancy cluster.

#### 3.4.2 Summary of HDSiP Stability

The electrical dopant activation level observed in post DSA HDSiP is inherently unstable upon low temperature secondary annealing. DSA activated  $2x10^{21}$  cm<sup>-3</sup> P HDSiP was shown to return to as-grown carrier concentration levels after a 700 °C RTA for 60 s. The deactivation process was suggested to be reversible and HDSiP could be reactivated with a second DSA anneal. Deactivation behavior follows an Arrhenius behavior with a single activation energy. Deactivation kinetics were determined for  $5x10^{20}$  cm<sup>-3</sup> P LDSiP as well as  $2x10^{21}$  cm<sup>-3</sup> P HDSiP.

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Activation energies of 2.1 eV and 1.3 eV, respectively, were obtained for the deactivation processes. Microstructure stability was analyzed using HR-TEM demonstrating that HDSiP layers remained defect free after DSA and post DSA thermal treatment. No significant change in the strain state of HDSiP was observed after activating or deactivating anneals. It is proposed that activation and deactivation in HDSiP involves an interstitial mediated mechanism.

# CHAPTER 4 CLUSTERING CONFIGURATIONS IN HDSIP

#### 4.1 Background and Purpose

Understanding the dopant-defect interactions in HDSiP is critical to being able to assign root causes for the changes in electrical properties, strain, and microstructure of the material. In this instance, dopant-defect interactions are defined as the clustering configurations, reactions, and motion of phosphorus dopant species due to interactions with point defects. This study is primarily interested in understanding the clustering configurations of phosphorus present in HDSiP in the as-grown state and the activated state after laser DSA.

DFT work presented in section 1.3.2.4 is compelling evidence for the presence of a high concentration of vacancy clusters. However as incomplete activation is observed for the laser DSA, it is unknown whether only a fraction of available clusters dissolve or if there are multiple varieties of clusters present within the film. Entropy dictates that multiple cluster varieties will exist in HDSiP in any given state.

For the time being, conventional logic on dopant clusters and carrier donation will be applied. This logic states that for a phosphorus atom to donate its electron it must occupy a substitutional lattice site and be hydrogenic in nature. This requires that the phosphorus atom be only adjacent to silicon matrix atoms and no adjacent point defect species may exist. Phosphorus atoms that do not fulfill this condition are considered to be clustered and do not donate their electron. The effects of these clusters can still be observed through a decrease in the electron mobility of the material due to impurity scattering.

There are three main cluster types that will be considered for the purposes of this investigation: vacancy clusters, interstitial clusters and substitutional clusters. Vacancy clusters are bonding situations where one or more phosphorus atoms are directly adjacent to a vacancy.

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Interstitial clusters are where n phosphorus atoms and m silicon atoms occupy greater than m+n lattice sites. Finally, substitutional clusters exist where multiple phosphorus species occupy adjacent substitutional lattice sites and do not donate their electrons to the matrix. In reality it is not known what degree of separation is required for a dopant and a point defect before that dopant loses its hydrogenic nature. DFT simulations have suggested that dopant species as far apart as fifth nearest neighbor configuration cannot be completely considered isolated from one another energetically or through lattice relaxations.[53], [80] The minimum distance between a dopant species and a point defect before the dopant species is considered to be in a deactivated state is likewise unknown. Typical doping concentrations below ~ $10^{20}$  cm<sup>-3</sup> levels are well below the concentration where this effect needs to be considered. For HDSiP where up to 12% of the atomic species are dopants, the average spacing between atoms becomes significant. In this manner, the understanding of dopant-defect interactions in HDSiP can be used to understand the physical limitations and proximity effects of dopant and point defect species on the hydrogenic nature of carrier donation.

### **4.2 Experimental Methods**

HDSiP films were grown several tens of nanometers thick onto nominally p-type 300 mm silicon (001) wafers. This growth process was conducted in a horizontal RP-CVD reactor. Precursor gasses used were dichlorosilane and phosphine gas with precursor partial pressures dependent on the desired film concentration. Upon receiving sample wafers, four-point probe resistivity maps were created to determine resistivity uniformity with respect to position on the wafers. For samples exposed to the ms laser DSA, sections of wafer were cleaved and annealed using Applied Materials Vantage® Astra<sup>TM</sup> DSA system. This system uses a continuous wave laser which rasters over the sample surface resulting in a total exposure time of 0.25 ms.

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A number of analytical characterization techniques were conducted during this work each with individualized sample preparation and methods of obtaining data. XPS was carried out on a ULVAC PHI XPS system. Samples in the as-received state without solvent rinse or etching were prepared in-situ before analysis. A 2kV argon sputter was conducted on the surface to remove any native oxide. Spectra were obtained using a monochromatic aluminum  $k_{\alpha}$  x-ray source. EELS and HAADF-STEM work were carried out on a FIB thinned cross-section sample created using the procedure described in section 2.7.4. Spectra collection and imaging was conducted on a JEOL JEM ARM-200cF aberration corrected TEM. Atom probe reconstruction was done using the commercial IVAS software from data obtained using a LEAP 5000 APT. Samples were prepared by etching off the native oxide, followed by deposition of a 50 nm thick nickel capping layer using an electron-beam evaporator. FIB lithography was used to lift out a cross section of the underlying HDSiP including the substrate and the resultant lift-out was placed on top of a specialized silicon wafer with existing silicon spires. From this, the sample tip was then sharpened using the FIB with an annular shaped milling pattern until only a thin layer of nickel was remaining. This sample tip was then analyzed with APT.

Oxidation studies for understanding oxidation rate of HDSiP and LDSiP were carried out on several different sections of similar wafers. Annealing was done in an atmosphere of dry  $O_2$ in a tube furnace or RTO. Oxide thickness measurements were taken predominantly with ellipsometry, although several oxide thickness values were confirmed using XTEM to ensure reliability of the ellipsometry models for oxides grown from HDSiP. Studies monitoring electrical property evolution during oxidation used a corner etch process to ensure a consistent thickness of oxide underneath electrical contacts. To accomplish this, the four corners of a 10 mm x 10 mm coupon sample were covered using Kapton tape. Next, the exposed center of the sample was covered in hot parrafin wax. The tape was removed from the corners exposing them, and then the samples were dipped in dilute HF to etch the corner areas. n-heptane was used to dissolve the wax after etching followed by a standard three-step solvent rinse process. Electrical contacts were made for conducting hall effect measurements by pressing on indium metal into the corner areas. After successful measurement, the contacts were removed using a lint-free wipe. The sample would then be exposed to RTO again and the process is repeated.

Marker layer diffusion studies were conducted on special samples which had buried marker layers grown in during epitaxy. Prior to the epitaxial growth of HDSiP or LDSiP, a ~5nm thick  $5x10^{19}$  cm<sup>-3</sup> phosphorus doped layer was grown using silane and phosphine gas precursors. Following this layer, a 150 nm thick nominally undoped silicon layer was grown to serve as a spatial diffusion buffer for the phosphorus HDSiP layer and the marker layer. Following this buffer layer, a layer of HDSiP was grown on the surface 50-85 nm thick. An additional control sample with the same structure except missing the HDSiP surface layer was also grown. For a diagram of these wafers, refer to section 2.2 Figures 2-1 and 2-2. Annealing of these wafers was carried out in a tube furnace under inert ambient using a bubbler in the exhaust to limit oxygen and water vapor intrusion into the annealing system. Diffusion was quantified using SIMS to obtain dopant concentration depth profiles and the FLOOPS software using standard Fickean diffusion models. For SIMS analysis, a Cs<sup>+</sup> primary ion beam was used.

### **4.3 Experimental Results**

### 4.3.1 HDSiP Phosphorus Oxidation State Determination with XPS

The theory behind how XPS could be used to determine clustering configurations of phosphorus within HDSiP is based on the possibility that a substitutional phosphorus atom could exist in a different oxidation state than an inactive clustered phosphorus atom. Silicon peaks in XPS can exhibit a shoulder on one side indicating silicon bonded in an oxide compared to the peak signal which is from the crystalline silicon. It was theorized that the phosphorus peak of HDSiP would also be shifted due to high concentrations of clustered phosphorus.

When the analysis was conducted, as-grown samples were used that had no treatment done to the surface. Rinsing with a standard solvent process would have left adsorbates that would manifest in longer pump-down time as well as a stronger than desired carbon 1s peak. In order to obtain data from XPS, an in-situ surface 2kV argon sputter was required to strip the sample surface of native oxide. As the native oxide of HDSiP (~3 nm) is thicker than that of undoped silicon (1.4 nm) only a weak phosphorus signal could be detected from the  $4.4 \times 10^{21}$  cm<sup>-</sup> <sup>3</sup> P HDSiP sample tested before sputtering. This procedure was then conducted for all samples as a method of standardization.

Figure 4-1 overlays the XPS spectra for a sample of  $4.4 \times 10^{21}$  cm<sup>-3</sup> P HDSiP and a sample of  $4.5 \times 10^{20}$  cm<sup>-3</sup> P LDSiP. A pronounced doublet peak can be seen for the HDSiP sample which did not result for the LDSiP sample. This peak is due to the -3 oxidation state of phosphorus (phosphide peak) and exists as a doublet with spacing of 0.8 eV due to the two spin orbit components of the phosphorus 2p orbital (P2p<sub>1/2</sub> and P2p<sub>3/2</sub>). The lack of a corresponding peak for the  $4.5 \times 10^{20}$  cm<sup>-3</sup> P LDSiP sample is not indicative of a difference in chemical shift, just that the concentration of phosphorus in this sample is below the resolution limit for this XPS. It is possible that for a much longer exposure time a peak would be resolvable.

The difficulty of using XPS to determine clustering differences between HDSiP and LDSiP is that the resolution limit is approximately the same as the concentration threshold between HDSiP and LDSiP. A secondary method was devised to probe these clusters by comparing the XPS phosphorus 2p peak for two samples of HDSiP. Both samples possessed

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Figure 4-1. A phosphorus 2p doublet peak can be observed for a  $4.4 \times 10^{21}$  cm<sup>-3</sup> P HDSiP sample where no peak can be observed for a  $4.5 \times 10^{20}$  cm<sup>-3</sup> P LDSiP sample. The doublet present for HDSiP is not significantly shifted from its expected position and no shoulders appear which would be indicative of multiple oxidation states. The LDSiP sample lacking a P 2p peak is due to the phosphorus concentration being below the XPS resolution limit

 $1.9 \times 10^{21}$  cm<sup>-3</sup> phosphorus (~4%) which is above the resolvable concentration in XPS. One sample was in the as-grown state with  $2 \times 10^{20}$  cm<sup>-3</sup> active phosphorus and  $1.7 \times 10^{21}$  cm<sup>-3</sup> clustered phosphorus. The other sample had been exposed to a 1200 °C activating DSA with  $9 \times 10^{20}$  cm<sup>-3</sup> active phosphorus and  $1 \times 10^{21}$  cm<sup>-3</sup> clustered phosphorus. As can be seen in Figure 4-2 a single peak can be resolved for phosphorus in both the as-grown and DSA annealed HDSiP samples. No discernable peak shift can be observed between the two samples with vastly different concentrations of active versus clustered phosphorus. Further examination of HDSiP using XPS was not conducted as it did not appear to be a useful method in determining clustering configurations of HDSiP.



Figure 4-2. For as-grown (red) and DSA (blue)  $1.9x10^{21}$  cm<sup>-3</sup> P HDSiP samples that have dramatically different concentrations of clusters and active phosphorus, no observed peak shift can be detected.

# 4.3.2 HDSiP Local Bonding Environment Determination with EELS

Local bonding environment of an atomic species can be determined with EELS analysis and comparison of EELS spectra fine structure to simulations.[138] In this manner EELS can yield similar information to x-ray absorption spectroscopy without necessitating a synchrotron. For EELS analysis, a cross-sectional TEM sample is prepared as described in section 2.7.4. In order to maximize signal from clustered phosphorus in HDSiP, the highest concentration film available was used in its as-grown state.  $4.4 \times 10^{21}$  cm<sup>-3</sup> phosphorus HDSiP has been measured with Hall-effect to suggest that  $4.2 \times 10^{21}$  cm<sup>-3</sup> phosphorus atoms exist in clusters.

HDSiP is a uniform material in that active dopants as well as dopant clusters are randomly dispersed throughout the film. Due to this spatial uniformity, TEM-EELS was conducted instead of STEM-EELS to maximize signal. Analysis was conducted using a JOEL JEM ARM200cF aberration corrected TEM with an accelerating voltage of 200kV. In order to parse out effects of thickness, EELS measurements were conducted on both the substrate and the HDSiP layer sides of the substrate-layer interface for comparison. The energy loss range was chosen to capture the phosphorus L-edges at 132 ( $L_{2,3}$ ) and 189 eV ( $L_1$ ).

As can be seen in Figure 4-3, both the silicon substrate spectra and the HDSiP spectra show a sharp peak at 99 eV and a delayed maximum as is indicative of the silicon  $L_{2,3}$  edge. An additional small peak can be observed at 149 eV in both samples for the silicon  $L_1$  edge. Apart from these similarities, two key differences can be observed between the silicon substrate spectra and the HDSiP spectra. The first being the presence of a weak phosphorus  $L_{2,3}$  peak at 132 eV for the HDSiP sample. Comparing the HDSiP spectra and the substrate spectra, no difference in the fine structure can be distinguished in the energy range between 50 and 100 eV after the phosphorus  $L_{2,3}$  peak. The overlapping nature of the silicon  $L_{2,3}$  extended fine structure and the silicon  $L_1$  peak dominate the signal within this range for both HDSiP and the substrate. No phosphorus  $L_1$  peak could be observed. Plural scattering due to a beam electron scattering off of a core electron and a free electron in the material also dominated the signal in this range.

The other major distinguishing factor between the two spectra is that HDSiP produced a lower initial silicon  $L_{2,3}$  peak height as well as a lower delayed maximum number of signal counts. A potential cause for this is due to a lower effective concentration of silicon in the examined material (91.2% instead of 100%). When the silicon substrate spectra counts are scaled down by this factor within the range of 100 to 175 eV, good agreement can be seen between the two curves (Figure 4-4).

Overall, fine structure information of the phosphorus L edges was not able to be obtained using EELS. If this experiment were to be conducted again, improved peak resolution could be obtained through minimizing sample thickness. Thinner samples reduce plural scattering which

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gives rise to such a large broad area of the spectra after the initial silicon loss peak. Additionally, despite being a less intense absorption edge, fine structure data may be able to be obtained from the phosphorus K-edge at 2146 eV. At this energy loss value, silicon peaks would be expected to have a very low contribution to signal as the silicon K-edge is at 1839 eV.



Figure 4-3. TEM-EELS spectra of as-grown  $4.4 \times 10^{21}$  cm<sup>-3</sup> P. ELNES and EXELFS regions of the spectra are washed out by the plural scattering within the sample. Samples thinner than 15 nm are needed to obtain this data.



Figure 4-4. Good agreement in counts is obtained when the silicon substrate spectra counts are scaled down by a factor of 0.912 to account for the HDSiP having a significantly lower silicon concentration.

### 4.3.3 Atom Probe Tomography Cluster Analysis of HDSiP

As a technique, atom probe tomography can be a very powerful tool for cluster analysis. The preferred method of conducting this analysis is by computing the distance between each dopant atom and the closest dopant atom.[157] If dopant species are distributed randomly, a Poisson distribution would be predicted. However, if there are a large number of clusters of multiple dopants present within the atom-probe tip, the distance distribution would be bimodal.

Of six atom probe tips which were analyzed, meaningful data was only able to be obtained for one tip due to tip fracture. This tip had a layer of  $4.4 \times 10^{21}$  cm<sup>-3</sup> P HDSiP which had been exposed to a 1200 °C DSA. The reasoning behind using a post DSA film for this analysis was to increase the concentration of substitutional phosphorus in the film. According to Halleffect electrical data, the phosphorus in this sample was  $6 \times 10^{20}$  cm<sup>-3</sup> active and  $3.8 \times 10^{21}$  cm<sup>-3</sup> clustered. Originally this sample was supposed to be compared to a  $3.0 \times 10^{21}$  cm<sup>-3</sup> P HDSiP sample also exposed to the DSA which had  $1 \times 10^{21}$  cm<sup>-3</sup> active phosphorus and  $2 \times 10^{21}$  cm<sup>-3</sup> clustered phosphorus. This sample did not yield meaningful data.

To protect the surface of the HDSiP during the required annular milling, a thin film of nickel was deposited on the surface as a capping material. Nickel was chosen for its preferred field evaporation tendencies. Nickel is able to evaporate in a well-behaved manner such that a benign tip radius can form prior to evaporating through the region of interest.

From the reconstruction formed with this atom probe data set it can be seen that three layers result. Clear delineation can be observed between the silicon substrate and the HDSiP layer and nickel capping layer as seen in Figure 4-5. Silicon atoms were defined as ions with mass-to-charge ratios of 28 ( $^{28}$ Si+), 29 ( $^{29}$ Si+), 30 ( $^{30}$ Si+) as well as the doubly charged variants of these same ions and singly charged ion pairs. Contributions to the phosphorus signal were ions with mass-to-charge ratios of 31 ( $^{31}$ P<sup>+</sup>) 15.5 ( $^{31}$ P<sup>2+</sup>), 62 ( $^{31}$ P<sub>2</sub><sup>+</sup>) as well as 59 ( $^{28}$ Si<sup>31</sup>P<sup>+</sup>). No other peaks in the mass-to-charge spectra existed for possibilities of phosphorus above the noise level of the spectra. Nickel has several common isotopes which were considered in single charged, doubly charged, and singly charged ion pair states.

The problem that resulted from data analysis is that there is a mass-to-charge overlap between nickel which was used as the capping material and phosphorus.  ${}^{62}Ni^+$  and  ${}^{31}P_2^+$  both have a mass to charge ratio of 62. It is assumed that the ion signal for the 62 mass-to-charge ratio peak from phosphorus  ${}^{31}P_2^+$  species should be consistent throughout the layer, where the ion signal for  ${}^{62}Ni^+$  species should reside spatially above the HDSiP layer with a slight overlap into the layer. For the purposes of reconstruction, all ion counts with a mass-to-charge ratio of 62 were labeled as phosphorus  ${}^{31}P_2^+$  ion pairs. It has to be assumed then that the concentrations observed in Figure 4-6 between 0 nm and 20 nm have a mixture of  ${}^{62}Ni^+$  and  ${}^{31}P_2^+$  ions and that this is the reason for the resultant spike in concentration at 17 nm. This spike simply corresponds to the nickel/HDSiP layer interface.



Figure 4-5. 3-dimensional atom probe tip reconstruction using IVAS software. 4.4x10<sup>21</sup> cm<sup>-3</sup> P HDSiP sample can be seen. Points within this reconstruction correspond to labeled ion counts.

Data analysis can still be conducted without artefacts of the deposited nickel capping layer by examining the reconstruction data close to the HDSiP/silicon interface. Figure 4-6 shows that the data pipe phosphorus concentration obtained for the  $4.4x10^{21}$  cm<sup>-3</sup> P HDSiP sample is consistent with measurements from SIMS and HR-XRD. In this region, overlap with the <sup>62</sup>Ni<sup>+</sup> ion counts should not be an issue.



Figure 4-6. A vertical data pipe was used to measure concentration with respect to distance along the pipe. The concentrations obtained using this method are similar to what has been observed for SIMS analysis of the same sample. Phosphorus concentration values within the top 20 nm of the tip are inaccurate as there exists mass-to-charge ratio overlap between nickel and phosphorus.

As such a large percentage of phosphorus in HDSiP field evaporated as <sup>31</sup>P<sub>2</sub><sup>+</sup> ions (Figure

4-8), obtaining a dopant distance distribution such as described by Philippe et al. is not possible.[157] As the diatomic ion is detected as one count, the same (x,y,z) coordinate is assigned to both atoms within the ion. However, it can be assumed that these  ${}^{31}P_{2}^{+}$  ion species were field evaporated from a bonding situation of adjacent phosphorus atoms. At liquid helium temperatures in ultrahigh vacuum it is unlikely that significant surface reconstruction occurred, and the probability of a phosphorus ion combining with a neutral phosphorus species in route to the detector is extremely unlikely. The statistically most probable dopant distance for a concentration of  $4.4 \times 10^{21}$  cm<sup>-3</sup> P sample of HDSiP can be determined by equation 4-1. The result

$$d = 2\left(\frac{1}{2\pi C_0}\right)^{\frac{1}{3}}$$
(4-1)

is that if all the phosphorus in a  $4.4 \times 10^{21}$  cm<sup>-3</sup> HDSiP sample were randomly distributed on lattice sites, the most probable dopant distance would be 6.6 Å. This can be compared to the nearest neighbor distance for silicon which is 2.35 Å. Statistically, if all dopant species were assumed to be uncharged and were situated on lattice sites at random, only 14.1% of the phosphorus would exist in clusters with one or more phosphorus on adjacent lattice sites. The number of these clusters counted as P<sub>2</sub><sup>+</sup> ions would be further reduced from that number due to the imperfect detection efficiency of APT. In addition to that, there is a chance that that multiple phosphorus atoms on adjacent lattice sites could also be field evaporated separately. The observation that 64% of the total phosphorus concentration was field evaporated as <sup>31</sup>P<sub>2</sub><sup>+</sup> ions (Figure 4-9) suggests that the majority of phosphorus atoms are arranging themselves next to other phosphorus atoms in a nonrandom fashion. This is consistent with the presence of a dispersed Si<sub>3</sub>P<sub>4</sub> phase.



Figure 4-7. Phosphorus concentration profile within HDSiP obtained using a horizontal data-pipe is consistent with SIMS and HR-XRD measurements.



Figure 4-8. Total phosphorus concentration in HDSiP and the breakdown of ion counts by ion species. Phosphorus from  $P_2^+$  ions constituted the majority of signal. Phosphorus  $P^+$  ion counts (~2.5%, 1.25x10<sup>21</sup> cm<sup>-3</sup>) were greater than the carrier concentration of the film (6x10<sup>20</sup> cm<sup>-3</sup>). It is likely that 50% or greater of the P<sup>+</sup> ions came from clustered phosphorus. Distance corresponds to position along the horizontal data pipe in Figure 4-7.



Figure 4-9. Percentage of phosphorus concentration measured through  $P_2^+$  ion counts relative to the total phosphorus concentration. The average across all distances was 64%. Distance corresponds to position along the horizontal data pipe in Figure 4-7.

# 4.3.4 HAADF-STEM Analysis of HDSiP

HAADF-STEM was used to analyze films of HDSiP and LDSiP. Two XTEM samples were prepared from as-grown wafer samples. One sample was  $3.6 \times 10^{20}$  cm<sup>-3</sup> P LDSiP and the other was  $4.4 \times 10^{21}$  cm<sup>-3</sup> P HDSiP. From the images obtained of the layer/substrate interface, an

increase in the background intensity across the interface can be observed. For the HDSiP sample (Figure 4-10), this channel intensity visible from the micrograph itself. For the LDSiP sample, this increase in channel intensity can only be resolved using a line scan plot of HAADF intensity across a row of dumbbells (Figure 4-11). Channel intensity increases of 75% (HDSiP) and 15% (LDSiP) were recorded. An abrupt interface can be easily observed for the HDSiP sample in both the micrograph as well as in the line-scan. Neither the micrograph nor the line-scan of the LDSiP sample gave a clear indicator of the position of the LDSiP/silicon interface. Capturing the interface in the image was done by using the known layer depth extracted from HR-XRD



Figure 4-10. HAADF-STEM micrograph of the substrate/HDSiP layer interface of a 4.4x10<sup>21</sup> cm<sup>-3</sup> P HDSiP as-grown sample. An increase in the channel intensity between dumbbells can be observed in the HDSiP layer. Line-scan intensity plot shows a 75% increase in channel intensity across the interface.

calculations. No change in the intensity of the dumbbells themselves was noticed between the HDSiP or LDSiP and the respective substrate. This was to be expected due to the very minor difference in atomic mass between silicon and phosphorus.

This sort of channel intensity increase is likely to be caused by atomic species in the layer occupying off-lattice site positions while still maintaining single-crystal epitaxy. Interstitial species would occupy positions in the lattice structure which could potentially cause this sort of channel intensity in sufficiently high concentrations. Phosphorus in a vacancy cluster configuration has been suggested to relax slightly into the vacancy position which could also result in a variation in position from the respective column of atoms.



Figure 4-11. HAADF-STEM micrograph of the substrate/HDSiP layer interface of a 3.6x10<sup>21</sup> cm<sup>-3</sup> P LDSiP as-grown sample. No visible interface can be distinguished. Line-scan intensity plot shows a 15% increase in channel intensity across the interface.

A simulation of the HAADF-STEM micrograph in Figure 4-10 has been conducted given the relaxed structure of P<sub>4</sub>V from DFT simulations. In Figure 4-12, the degree of relaxation of a unit cell of pure P<sub>4</sub>V material was predicted. The four phosphorus atoms on the quarter sites are seen to relax into the central vacancy. When viewed from the [110] direction similar to how the HAADF-STEM was conducted, minor differences in the alignment of atomic columns can be visualized. For a material that possesses  $4.4 \times 10^{21}$  cm<sup>-3</sup> phosphorus with all of the phosphorus bonded in P<sub>4</sub>V dispersed clusters, a simulated HAADF-STEM image was generated. This image was generated given the microscope imaging parameters used for the micrographs obtained in Figures 4-10 and 4-11. It can be seen from Figure 4-14 that no difference in the HAADF-STEM channel intensity can be observed between this sample and a pure silicon sample with the same simulation conditions. Minor differences in dumbbell peak intensity were predicted, however the greater channel intensity of HDSiP experimentally observed with HAADF-STEM could not be replicated through simulations with P<sub>4</sub>V clusters. It is suggested that a high concentration of interstitial clusters present in  $4.4 \times 10^{21}$  cm<sup>-3</sup> P HDSiP are responsible for the observed channel intensity increase over the substrate.



Figure 4-12. Relaxed unit cell of P<sub>4</sub>V cluster obtained through DFT simulations viewed from the [001] direction. Blue circles represent silicon atoms and grey circles represent phosphorus.



Figure 4-13. Pure P<sub>4</sub>V theoretical material in relaxed state viewed from the [110] direction. Blue circles represent silicon atoms and grey circles represent phosphorus.



Figure 4-14. HAADF-STEM simulation of (a) pure silicon and (b)  $4.4x10^{21}$  cm<sup>-3</sup> P HDSiP assuming all phosphorus is bonded in P<sub>4</sub>V clusters. No difference in background intensity is observed. (c) Minimal difference in line-scan intensity can be noted.

## 4.3.5 Effects of Interstitial Injection on Deactivation of HDSiP

To investigate possible dopant clustering configurations in HDSiP, the effects of interstitial injection on deactivation were studied. This experiment entailed using oxidation as a method of interstitial injection. As discussed in section 2.4, thermal oxidation of a silicon surface is known to inject interstitials. The rate at which this process occurs is proportional to the rate of

oxidation. It had already been determined that inert thermal annealing causes deactivation of DSA activated HDSiP. Through comparing deactivation anneals in oxidizing versus inert ambient, knowledge about the clusters formed during deactivation can be obtained.

Prior to attempting to model deactivation under oxidizing conditions, it was important to understand oxidation kinetics of HDSiP. Thermal oxidation rate depends on many factors such as dopant concentration, active dopant concentration and strain state. As HDSiP is essentially a semiconductor alloy, it cannot be assumed that the oxidation of HDSiP will progress at a similar rate to silicon. Thin oxide growth was studied to quantify the oxidation rate of LDSiP and HDSiP. To do this, several samples of 3.6x10<sup>20</sup> cm<sup>-3</sup> P LDSiP and 3.0x10<sup>21</sup> cm<sup>-3</sup> P HDSiP were exposed to furnace anneals at 700 °C under dry O<sub>2</sub> ambient. Oxide film thickness values were obtained using ellipsometry. By executing a linear fit on the data in Figure 4-15, oxidation rates can be extracted for HDSiP and LDSiP. It can be seen that the dry oxidation of  $3.0 \times 10^{21}$  cm<sup>-3</sup> P proceeds at a rate of 0.53 nm/min during the initial stages of oxidation studied here.  $3.6 \times 10^{20}$  cm<sup>-</sup> <sup>3</sup> P LDSiP proceeds at a slower rate of 0.13 nm/min. These values when compared to the data obtained by D. Skarlatos et al. correspond to interstitial injection fluxes of  $1 \times 10^{11}$  cm<sup>-2</sup>s<sup>-1</sup> and  $2x10^{10}$  cm<sup>-2</sup>s<sup>-1</sup> for HDSiP and LDSiP respectively.[127] It will be assumed here that no obstruction of the interstitials at the HDSiP/substrate interface occurs. Average interstitial concentrations of  $1.3 \times 10^{18}$  cm<sup>-3</sup> and  $2.7 \times 10^{17}$  cm<sup>-3</sup> can be calculated within the HDSiP and LDSiP layers, respectively, for a three minute anneal at 700 °C. The diffusivity value (1x10<sup>-12</sup> cm<sup>-3</sup>/s) used for this calculation is the trap-limited interstitial value obtained by P.A. Stolk et al. and predicts a diffusion depth of 134 nm. [154]

To obtain the oxidation deactivation data for Figure 4-16, samples were annealed in an RTA for the allotted time in dry  $O_2$  ambient. Following this, ellipsometry measurements of oxide thickness were used to ensure consistency with the prior collected oxidation rate data in Figure



Figure 4-15. Thermal oxidation progress for 3.6x10<sup>20</sup> cm<sup>-3</sup> P LDSiP and 3.0x10<sup>21</sup> cm<sup>-3</sup> P HDSiP. Dramatically enhanced oxidation behavior can be observed for the HDSiP sample.

4-15 above. Prior to contact formation, the oxide on the corners of each sample below the contact region was etched off. This is due to how an increasing oxide thickness under the indium metal contacts with each successive Hall-effect measurement would lead to measurement errors. A nominally thinner HDSiP layer under this etched region is not expected to effect sheet resistivity measurements. This setup is preferable to etching the entire sample surface as the amount of native oxide grown (~4 nm for HDSiP) with each step is much higher than the amount of oxide grown through the thermal oxidation process when an existing oxide layer is present.

From analyzing deactivation of DSA activated HDSiP and LDSiP, it can be seen that interstitial injection due to thermal oxidation did not have a measurable effect on the deactivation rate (Figure 4-13). There are two potential reasons for this lack of effect. Firstly, it is possible that the ratio,  $\theta$ , of silicon atoms injected interstitially to silicon atoms consumed by the oxidation reaction in HDSiP is much less than for pure silicon. As HDSiP has a smaller effective lattice constant than silicon, less strain would be produced at the HDSiP/SiO<sub>2</sub> interface than at a silicon/SiO<sub>2</sub> interface. The other potential reason for not observing an effect of interstitial injection on deactivation rate is that the magnitude of interstitials injected was insufficient to cause an effect. The concentration of interstitials injected into the HDSiP layer is estimated to be  $1.3 \times 10^{18}$  cm<sup>-3</sup> assuming  $\theta_{Si} = \theta_{HDSiP}$ .



Figure 4-16. Deactivation behavior at 700 °C of 3.6x10<sup>20</sup> cm<sup>-3</sup>P LDSiP and 3x10<sup>21</sup> cm<sup>-3</sup> P HDSiP exposed to a 1200 °C DSA. The type of ambient flow gas during deactivating RTA or RTO had negligible effects on the rate of deactivation.

In order for thermal oxidation during deactivation to not produce an effect on

deactivation rate of HDSiP, the concentration of injected interstitials must be less than ~10% of

the point defect population in the layer. This supports the theory of a high concentration of interstitial clusters responsible for the deactivation behavior as outlined in Chapter 3. This would mean that a concentration of above  $1 \times 10^{20}$  cm<sup>-3</sup> interstitials and or interstitial clusters are present in HDSiP in the deactivated state.

### 4.3.6 Point Defect Injection Marker Layer Study of HDSiP

The oxidation interstitial injection study combined with the results from the original deactivation work in Chapter 3 suggests that interstitials may play a role in deactivation within the HDSiP layer. The theory that interstitials are causing activation and deactivation of HDSiP invokes a similar concentration of interstitial species around  $10^{20}$  cm<sup>-3</sup>. In addition to this, the theory that P<sub>4</sub>V clusters account for the inactive phosphorus that doesn't activate in HDSiP invokes a concentration of ~ $10^{20}$  cm<sup>-3</sup> vacancies present in the HDSiP layer. Given the potential for having such high concentrations of point defects in the HDSiP layer, studying the point defect release of HDSiP during annealing can give insight into the nature and quantity of these point defects grown into the HDSiP films.

Epitaxial HDSiP was grown with a buried  $\sim 5 \times 10^{19}$  cm<sup>-3</sup> phosphorus marker layer according to Figure 2-1 and Figure 2-2. Two samples will be considered for this study. The first is a control sample with no HDSiP layer on the surface. The second is a sample with 85 nm of  $2 \times 10^{21}$  cm<sup>-3</sup> P HDSiP grown onto the surface. By taking the ratio of the diffusivity values obtained for the buried marker layers (D<sub>P</sub>/D<sub>P</sub><sup>\*</sup>) one can determine the degree of interstitial over or under saturation. As phosphorus is a purely interstitial diffuser at low concentrations (f<sub>i</sub>=0.99), diffusivity enhancement of the sample with the HDSiP layer would indicate interstitial injection by the layer.[93], [94] Diffusivity retardation would indicate an oversaturation of vacancies being injected into the bulk by the HDSiP layer. In either case, the diffusivity values for both vacancies and self-interstitials in silicon are both several orders of magnitude higher than phosphorus such that point defects released by the layer will easily reach the buried layer.

Given an equilibrium concentration of point defects, phosphorus at 700 °C should exhibit a diffusivity value of  $7x10^{-19}$  cm<sup>2</sup>/s. Negligible diffusion of the marker layer can be observed after 4 hours at 700 °C in inert conditions (Figure 4-17). This observation agrees with the expected diffusivity value. For much longer anneal times of above 48h of 240 hours at 700 °C in inert conditions, a diffusivity of  $1.25x10^{-18}$  cm<sup>2</sup>/s can be estimated using the FLOOPS simulation software. This value agrees with previously reported data in the literature (Figure 4-18) and will be used for  $D_p^*$ , the equilibrium diffusivity of phosphorus in the following sections.



Figure 4-17. Buried marker layer diffusion for the control sample (no HDSiP layer on wafer surface). Negligible diffusion occurs within 4 hours at 700 °C in inert ambient. Significant diffusion occurs after 48 hours which can be modeled with FLOOPS.



Figure 4-18. Control Marker layer diffusivity value plotted with previously reported values from literature obtained from P. Pichler. [85] Obtained values show good agreement with previously obtained works despite the lower temperature diffusion studied within this work.

The buried marker layers of the samples with a  $2x10^{21}$  cm<sup>-3</sup> P HDSiP layer on the surface were shown to exhibit significant diffusion in a time span from 30 minutes to 10 hours. As can be seen from Figure 4-19 on the left, no diffusion can be observed during the ms laser DSA or during a 2 minute RTA at 700 °C. These two anneals correspond to activation of dopants from  $2.5x10^{20}$  cm<sup>-3</sup> to  $5.5x10^{20}$  cm<sup>-3</sup> (DSA) and then back to  $2.5x10^{20}$  cm<sup>-3</sup> after the secondary RTA. No diffusion can be observed in either case. This is partially due to the diffusion length of point



of the marker layer. At 30 minutes at 700 °C in inert atmosphere, tail formation can be observed on the right side of the marker layer

Figure 4-19. Annealing time series for 2x10<sup>21</sup> cm<sup>-3</sup> P HDSiP showing marker layer diffusion. Left plot shows time frames for activation and deactivation where no diffusion is evident. Right plot shows time frames where diffusion can be observed.

(Figure 4-19, right). The dopant concentration profile of these marker layers is sharper on the deeper side. For this reason, tail diffusivity has been modeled on this side has been modeled 1-directionally with the FLOOPS simulation software as described in section 2.8.2. It can be seen from a comparison of these diffused profiles to the diffused profiles of the control sample that a significant diffusion enhancement of the marker layer is occurring. This diffusion enhancement is indicative of interstitials being released from the HDSiP layer during annealing. After diffusivity values were obtained for each of the profiles for the right plot in Figure 4-18,  $D_P/D_P^*$ 

values were converted to  $C_I/C_I^*$  using equation 2-67. These values were then plotted as a function of time to understand the transient nature of the interstitial release (Figure 4-20).



Figure 4-20. The transient nature of the enhanced marker layer diffusion of a 2x10<sup>21</sup> cm<sup>-3</sup> P HDSiP surface layer sample. Interstitial oversaturation is seen to decay from 16 for a 30 m anneal to 3 where the diffusivity is seen to level off.

Interstitial oversaturation shown in Figure 4-19 is shown to decay from a factor of 16 observed for a 30 minute anneal to a factor of 3 where it levels off for anneal times ranging from 4 hours to 10 hours. This type of behavior can be linked to the transient nature of interstitial release by HDSiP. It suggests that a high concentration of interstitials are grown into the HDSiP layer. For longer annealing times, interstitial release can be considered to be negligible.

### **4.4 Discussion and Conclusions**

# **4.4.1 Discussion of Experimental Results**

From the work conducted in this Chapter, several key findings have been able to lend insight into the clustering configurations present within HDSiP. First, it should be discussed that several of the techniques utilized for analysis such as XPS and EELS were not able to divulge useful information. It is still possible that given significantly more resources or time that some of these techniques would have been able to yield valuable information and this should be kept in mind for future experiments.

The major finding from this section is the observation of interstitial release by HDSiP upon annealing. That interstitials are released from the HDSiP layer indicates the presence of excess interstitials grown into the layer. This observation backs up the theory from Chapter 3 that interstitials mediate deactivation of HDSiP. The diffusivity of free interstitials is sufficiently high such that if these grown-in interstitials were not associated with a cluster in the as-grown film, they would diffuse through the bulk during growth. During longer time anneals, the majority of free interstitials have already escaped the HDSiP layer.

In addition, the observation of higher HAADF-STEM background intensity within HDSiP and LDSiP layers supports theories that PICs are present in as-grown HDSiP and LDSiP. The lower observed background intensity for LDSiP suggests that PICs still exist in LDSiP only in much smaller quantities. This is consistent with the post DSA carrier concentration work for LDSiP in section 5.3.1. APT ion mass-to-charge data offers experimental evidence in support of the theory that a high concentration of grown-in P<sub>4</sub>V clusters exist in HDSiP. 60% of the phosphorus signal in APT came from field evaporated  ${}^{31}P_{2}^{+}$  ions for a  $4.4x10^{21}$  cm<sup>-3</sup> P HDSiP sample after 1200 °C DSA. These phosphorus atoms were situated on adjacent lattice sites insitu to allow for simultaneous field evaporation.

# 4.4.2 Summary on Clustering Configurations in HDSiP

Experimental evidence from analytical techniques supports the theory in Chapter 3 that the breakup and reforming of PICs is responsible for activation and deactivation in HDSiP. XPS and EELS did not yield meaningful information on clustering configurations present in HDSiP. HAADF-STEM showed an increased channel intensity compared to the silicon substrate suggesting cluster presence on interstitial sites. Buried marker layer studies showed that HDSiP samples inject interstitials upon annealing. APT ion yields determined that 60% of the phosphorus in the  $4.4x10^{21}$  cm<sup>-3</sup> P HDSiP sample exists on adjacent lattice sites. This is further experimental evidence to support of the theory of P4V clusters grown into HDSiP that are not a source of activation upon DSA annealing.

# CHAPTER 5 CONCENTRATION DEPENDENCE OF PROPERTIES IN HDSIP

#### 5.1 Background and Purpose

The uniaxial tensile strain that can be applied to the channel region of an nMOSFET from the HDSiP source/drain stressors is proportional to the phosphorus concentration in the film. A linear relation between strain and concentration has been established by Li et al.[5] This section seeks to establish a relation between incorporated phosphorus concentration in HDSiP films and other properties such as electrical activation, resistivity, effects of DSA annealing, oxidation, and microstructural evolution.

Thus far it has been determined that the maximum level of phosphorus incorporation possible to be grown in single crystal epitaxy is approximately  $6x10^{21}$  cm<sup>-3</sup>. Significant degradation of as-grown crystal quality appears to decrease for phosphorus concentrations around  $4.5x10^{21}$  cm<sup>-3</sup> as evidenced by a decrease in the quality of strain peak fringes in HR-XRD. A shift in properties occurs between  $5x10^{20}$  cm<sup>-3</sup> P LDSiP and  $1x10^{21}$  cm<sup>-3</sup> P HDSiP due to theorized clusters in HDSiP that exist in substantially lower concentrations for LDSiP. Probing transitions of film properties with respect to incorporated phosphorus concentration will be the focus of this Chapter.

#### **5.2 Experimental Methods**

The primary methods used to obtain the information in this section have were electrical measurements with Hall-effect, oxidation thickness measurements through ellipsometry, TEM and marker layer analysis with SIMS. The processes used for these methods will be discussed in this section. All analysis was conducted on HDSiP and LDSiP thin films 40 – 85 nm thick grown on nominally p-type silicon (001) wafers grown using a horizontal RP-CVD system. The growth precursors were DCS and PH<sub>3</sub> for silicon and phosphorus respectively. Samples that had buried

phosphorus marker layers were grown using  $SiH_4$  and  $PH_3$  gas for the marker layer growth and used a nominally undoped silicon region ~150 nm thick separating the marker layer from the surface HDSiP or LDSiP layer. Figure 2-1 is a diagram of these marker layer samples.

For Hall effect measurements of electrical properties, wafer surfaces were etched with dilute HF to remove surface contamination and native oxide. This was followed by a standard three-step solvent rinse to ensure a clean surface for making electrical contacts. Contacts were formed with pressed on indium metal at the corners of a 10 mm x 10 mm wafer sample. Sheet number values have been converted to carrier concentration values through correlation with layer thickness obtained through SIMS or HR-XRD.

Oxidation experiments were conducted on samples prepared in the same fashion as above using dilute HF to etch the native oxide and a three-step solvent rinse to remove surface contamination. Thermal oxidation was carried out in a tube furnace using dry O<sub>2</sub> as the oxidizing gas. Oxide thickness was determined through ellipsometry and comparison to SiO<sub>2</sub> on silicon models.[144] To ensure the validity of these models for measurements of SiO<sub>2</sub> on HDSiP, XTEM was also used on several samples to obtain an oxide thickness.

Defect evolution in HDSiP films was conducted using HR-TEM and weak-beam dark field TEM on cross sectional (XTEM) samples. XTEM lamella were created using the procedure outlined in section 2.7.4.

Samples for marker layer diffusion analysis were annealed in a tube furnace under inert argon ambient. An exhaust bubbler was used to prevent ingress of oxygen and water vapor during annealing. SIMS was used with a Cs+ primary ion beam to obtain dopant concentration profiles of the diffused HDSiP and marker layers respectively. These concentration profiles were

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then modeled with the FLOOPS diffusion software to extract a time-averaged diffusivity value for the buried phosphorus marker layer.

### **5.3 Experimental Results**

## **5.3.1 HDSiP Phosphorus Concentration Dependence of Activation**

Previous studies have reported that as-grown active carrier concentration of HDSiP and LDSiP layers grown with the co-flow epitaxial growth process ranges from  $1.5-2.5 \times 10^{20}$  cm<sup>-3</sup>. This value is independent of total phosphorus in the film. The findings of Figure 5-1 agree with this report.



Figure 5-1. Carrier concentration dependence on chemical phosphorus concentration. 100% activation can be achieved for LDSiP samples exposed to 1200 °C DSA. Active level peaks for the 3x10<sup>21</sup> cm<sup>-3</sup> P HDSiP sample.

The effects of DSA annealing at 1200 °C vary significantly as a function of incorporated phosphorus concentration. For some LDSiP samples, close to 100 % activation was able to be attained indicating that clusters present in the as-grown film are dissolving to allow phosphorus atoms to occupy substitutional lattice sites. At HDSiP concentrations, active concentration peaked for the  $3x10^{21}$  cm<sup>-3</sup> P HDSiP sample around  $9.5x10^{20}$  cm<sup>-3</sup>. The 1200 °C DSA was

observed to have a less substantial effect for the highest concentration HDSiP film. In this concentration of film, greater resistivity was observed for as-grown films as well as post 1200 °C DSA films. This higher resistivity is predominantly due to the observed higher mobility of HDSiP samples combined with a lower degree of activation. Deactivation characteristics at 700 °C were observed to be similar for HDSiP films irrespective of incorporated phosphorus concentration (Figure 5-2). This subject has been discussed in further depth in Chapter 3.



Figure 5-2. Deactivation behavior of LDSiP and HDSiP films after exposure to a 1200 °C DSA followed by a secondary RTA at 700 °C for the stated times.

Undesirable electrical properties result from increasing grown-in phosphorus concentrations in HDSiP films beyond  $3x10^{21}$  cm<sup>-3</sup>. There are two main explanations for this observed phenomenon. Firstly, at this high concentration of phosphorus, the average spacing between dopant species that are randomly distributed is 6.6 Å as calculated using equation 4-1. Statistics and entropy dictate that a large fraction of dopant species will be situated with a spacing much less than this. At this degree of separation, it has been shown by DFT calculations conducted by Dhayalan et al. that phosphorus atoms closer together than 6.6 Å cannot be considered isolated from one another energetically.[80] It is therefore possible that in the  $4.4x10^{21}$  cm<sup>-3</sup> P HDSiP sample a significant quantity of substitutional phosphorus atoms exist too close to one another to be isolated. In this theoretical situation, less than ideal donation of electrons would be assumed as phosphorus species closer than some critical spacing from one another would not donate their electrons. The other possibility is that for the  $4.4x10^{21}$  cm<sup>-3</sup> P HDSiP sample, dissolution of clusters becomes energetically unfavorable due to the high concentrations of substitutional and clustered phosphorus.

#### 5.3.2 Oxidation Enhancement of HDSiP

In transistor process flow, the selective epitaxially grown material for the source/drain regions such as HDSiP would never experience oxidation. However, for the use of oxidation as a method of investigating a novel material, it is necessary to know the rate at which oxidation takes place. This knowledge is useful for determining appropriate oxidation times in future experiments such that a reasonable amount of HDSiP layer can be consumed. Oxidation experiments in this work were conducted in a tube furnace at 700 °C in an atmosphere of dry O<sub>2</sub> for facile comparison to previously collected data.



Figure 5-3. Dry oxidation progression at 700 °C for HDSiP films as a function of incorporated phosphorus concentration and whether or not the samples were exposed to a ms laser DSA at 1200 °C.

As can be seen in Figure 5-3, the thermal oxidation of HDSiP proceeds at a vastly enhanced rate compared to normal control p-type silicon. This is not unexpected as oxidation rate is a function of dopant concentration and HDSiP samples possess extremely high concentrations of both active and inactive dopants. In addition to this, as HDSiP is a semiconductor alloy rather than just doped silicon, it was expected that the oxidation rate of this alloy may be different than that of doped silicon.

What was unexpected was the lasting dependence of oxidation rate on whether or not the sample had been exposed to a 1200 °C DSA prior to oxidation. Data points in Figure 5-3 each correspond to a unique sample rather than a repeatedly annealed sample demonstrating that this trend is repeatable. Despite deactivation of  $3.0 \times 10^{21}$  cm<sup>-3</sup> and  $4.4 \times 10^{21}$  cm<sup>-3</sup> P HDSiP occurring after ~3 minutes at 700 °C, extended effects of DSA exposure on oxidation time were observed.

This phenomenon is not well understood and was not pursued further as the oxidation behavior of HDSiP is not relevant for process integration.

# **5.3.3 Extended Defect Formation in HDSiP**

Coinciding with the observation of deteriorated electrical properties, the 4.4x10<sup>21</sup> cm<sup>-3</sup> P HDSiP sample has also been observed to form extended defects upon deactivation. A 30 minute inert furnace anneal at 700 °C resulted in the observation of a significant number of dislocation loops within the HDSiP layer. The loops that form are on average 4 nm in diameter and form predominantly within the lower half of the HDSiP film closer to the substrate. Dislocation loop formation during deactivating anneals is indicative of a point defect supersaturation in the layer consistent with the theory of grown in PICs in HDSiP presented in this work.



Figure 5-4. Weak beam dark-field ( $g_{220}$ ) TEM image of  $4.4 \times 10^{21}$  cm<sup>-3</sup> P HDSiP showing dislocation loop formation. Layer thickness is 40 nm. Loops nucleated predominantly in the lower half of the layer.

Determination of the character of these extended defects was important to understand the type of point defects responsible for their nucleation. Loops of this size are too small to analyze for their nature using inside-outside contrast methods.[158] Therefore oxidation of the layer was used to determine whether the dislocation loops were intrinsic (consisting of vacancies) or

extrinsic (consisting of interstitials). To accomplish this analysis, an initial 2 h inert anneal at 700 °C was conducted to nucleate loops followed by a secondary oxidizing anneal. Figure 5-5 shows the effects of this oxidizing anneal. After oxidation, dislocation loops grow in size and quantity suggesting that the interstitials injected by oxidation are absorbed by loops causing growth. Therefore, the original nucleated loops are extrinsic in nature and were formed by an initial excess of interstitial species in the HDSiP layer during inert annealing. This finding corroborates the marker layer diffusion studies of sections 4.3.3 which found that a large concentration of interstitials are grown into HDSiP. At a phosphorus concentration of  $4.4 \times 10^{21}$  cm<sup>-3</sup>, the concentration of grown-in interstitials is above the threshold for homogeneous loop nucleation. This suggests that greater than  $1.6 \times 10^{19}$  cm<sup>-3</sup> interstitials are present in the  $4.4 \times 10^{21}$  cm<sup>-3</sup> P HDSiP film.[89] A lack of observed dislocation loops in half of the HDSiP layer closer to the surface is due to the ability of self-interstitial species to annihilate on the surface. The concentration profile of interstitial species declines towards the sample surface with a peak in the bottom half of the HDSiP layer. At higher temperatures for the same 4.4x10<sup>21</sup> cm<sup>-3</sup> P HDSiP film, dislocation loops were observed to form into stacking faults (Figure 5-6).



Figure 5-5. HR-TEM micrographs showing dislocation loops in 4.4x10<sup>21</sup> cm<sup>-3</sup> P HDSiP increasing in size and quantity with longer thermal oxidation time.



Figure 5-6. Defect evolution of 4.4x10<sup>21</sup> cm<sup>-3</sup> P HDSiP from the as-grown film (a) to dislocation loop formation after a 30 m 700 °C inert anneal (b) and finally, substantial stacking fault formation after a 3 m 900 °C RTA.

HDSiP films with phosphorus concentrations below  $4.4 \times 10^{21}$  cm<sup>-3</sup> were shown to be resilient to defect formation. During all annealing conditions which had resulted in a prolific quantity of extended defects in the  $4.4 \times 10^{21}$  cm<sup>-3</sup> P HDSiP sample no defects were observed in lower phosphorus concentration films. In an attempt to promote defect formation in the lower phosphorus concentration HDSiP films, more extreme annealing conditions were used. An initial 700 °C 2h inert furnace anneal was followed by a 3 minute 900 °C RTO to inject a large quantity of interstitials. Despite these annealing conditions, the micrograph shown in Figure 5-7 (a) remains defect free.

Ultimately, the microstructure of HDSiP epitaxially grown films is quite stable for all annealing conditions considered in this work. At an incorporated phosphorus of  $4.4 \times 10^{21}$  cm<sup>-3</sup>, extensive extrinsic defect formation resulted after thermal annealing.



Figure 5-7. Inert furnace anneal of 2 h at 700 °C shown to nucleate dislocation loops in 4.4x10<sup>21</sup> cm<sup>-3</sup> P HDSiP sample followed by 3m RTO at 900 °C to inject interstitials. Defect free layer of 3.0x10<sup>21</sup> cm<sup>-3</sup> P HDSiP sample (a) can be observed while 4.4x10<sup>21</sup> cm<sup>-3</sup> P HDSiP sample (b) resulted in stacking fault formation.

## 5.3.4 HDSiP High Concentration Strain Stability

Strain stability of a  $2 \times 10^{21}$  cm<sup>-3</sup> P HDSiP film was studied in section 3.3.5. However, as the  $4.4 \times 10^{21}$  cm<sup>-3</sup> P HDSiP sample has been shown in this section to exhibit anomalous electrical properties and defect formation it cannot be assumed that similar strain behavior would be observed. A HR-XRD coupled scan was conducted on the (004) Bragg peak to measure the strain evolution of the  $4.4 \times 10^{21}$  cm<sup>-3</sup> P HDSiP sample with respect to thermal anneals. It can be seen from Figure 5-8 that strain in the HDSiP layer is observed to be stable during a 30 minute inert thermal anneal which is the same condition where dislocation loop formation was observed. After 4 hours, a slightly higher strain value was recorded. This variance is thought to be due to this particular sample originating from a different location spatially on the original wafer rather than due to the anneal itself, as the measured layer thickness from HR-XRD here is also significantly lower than for the other two samples. Ultimately, it can be seen that thermal annealing for the times where extensive defect formation is observed does not effectively change the tensile strain in  $4.4 \times 10^{21}$  cm<sup>-3</sup> P HDSiP. This finding is consistent with the strain evolution measured for the  $2 \times 10^{21}$  cm<sup>-3</sup> P HDSiP sample in section 3.3.5.



Figure 5-8. HR-XRD spectra showing 4.4x10<sup>21</sup> cm<sup>-3</sup> P HDSiP samples after inert thermal annealing. From this data it can be seen that negligible changes in layer strain were observed after 30 m at 700 °C and a slightly higher strain value is noticed after 4h.

## 5.3.5 HDSiP Concentration Dependent Point Defect Release

Section 4.3.6 outlined that a high concentration of grown-in interstitials exist in the  $2x10^{21}$  cm<sup>-3</sup> P HDSiP film. Despite this, the  $2x10^{21}$  cm<sup>-3</sup> P HDSiP sample remained defect free after deactivating anneals. For the  $4.4x10^{21}$  cm<sup>-3</sup> P HDSiP sample, interstitials were present in sufficient quantity to nucleate loops as seen in section 5.3.3. To understand the HDSiP system more fully, a relation between the concentration of grown-in point defects and incorporated phosphorus was studied.

A series of wafers were grown according to Figure 2-1 incorporating several different concentrations of HDSiP in the surface layer. Surface LDSiP and HDSiP layer phosphorus concentrations ranged from  $5 \times 10^{20}$  cm<sup>-3</sup> to  $4.4 \times 10^{21}$  cm<sup>-3</sup>. Several annealing times were chosen at 700 °C for inert furnace anneals based on predicted diffusivity values. For all different samples, a 4 h time anneal was conducted for facile comparison. This time point was the onset time where

a steady state diffusivity enhancement was observed for the  $2.0 \times 10^{21}$  cm-3 P HDSiP sample noted in Figure 4-16.



Figure 5-9 shows the SIMS results for buried marker layer diffusion of samples with

Figure 5-9. SIMS concentration profiles showing buried marker layer diffusivity for samples with different concentrations of phosphorus grown into a surface HDSiP layer. Diffusion enhancement compared to a control sample with no surface HDSiP layer (a) was observed for all HDSiP concentration films (b-e).

HDSiP surface layers of different concentrations. In all cases, enhanced diffusivity of the phosphorus marker layer was observed indicating interstitial release during annealing. For each of these annealed marker layer samples, a value for the time-averaged tail diffusivity was extracted using the FLOOPS simulation software as outlined in section 2.8.2. Diffusion enhancement compared to the control sample was calculated as  $D_P/D_P^*$ . Using formula 2-67 this can be converted into the interstitial oversaturation  $C_I/C_I^*$  at the marker layer depth. Plotted as a function of HDSiP phosphorus concentration, it can be seen that an interesting trend arises. A downward trend of interstitial oversaturation with respect to increasing phosphorus concentration is observed until the  $4.4 \times 10^{21}$  cm<sup>-3</sup> P HDSiP sample which exhibits a significantly higher value.



Figure 5-10. Interstitial oversaturation at the buried marker layer depth at 700 °C for a four hour anneal is plotted with respect to phosphorus concentration within the surface HDSiP layer.
This abnormal behavior of the  $4.4 \times 10^{21}$  cm<sup>-3</sup> P HDSiP sample is consistent with other exhibited abnormalities compared to lower concentration HDSiP films. It is unlikely that a lower concentration of grown-in interstitials is present in the  $1 \times 10^{21}$  cm<sup>-3</sup> and  $2 \times 10^{21}$  cm<sup>-3</sup> P HDSiP films compared to the  $5.0 \times 10^{20}$  cm<sup>-3</sup> P LDSiP film. It is instead suggested that in the  $5.0 \times 10^{20}$ cm<sup>-3</sup> P LDSiP sample, interstitials released from PICs during activation are less likely to react with P4V clusters due to there being significantly fewer P4V clusters in LDSiP compared to HDSiP. This is substantiated by a higher activation energy for deactivation observed in section 3.3.3 for LDSiP compared to HDSiP as more interstitials are able to diffuse out of the layer.

# **5.4 Discussion and Conclusions**

# **5.4.1 Discussion of Experimental Results**

For use as a source drain selective epitaxial material, HDSiP exhibited detrimental properties when the incorporated phosphorus concentration exceeded  $4.4x10^{21}$  cm<sup>-3</sup>. These detrimental properties included degraded active carrier concentration and resistivity. Poorer electrical performance such as this was observed for the as-grown state of the film as well as after ms laser DSA. This  $4.4x10^{21}$  cm<sup>-3</sup> phosphorus concentration HDSiP sample was the only sample to exhibit extended defect formation upon annealing. The same sample also exhibited the highest marker layer diffusivity enhancement and thus the highest interstitial release upon annealing. It is suggested that these anomalous properties are due to the presence of an excessive amount of grown-in PICs. It is speculated that for lower phosphorus concentration HDSiP samples ( $P \le 3x10^{21}$  cm<sup>-3</sup>) near complete activation of phosphorus in PICs occurs after a 1200 °C DSA. The  $4.4x10^{21}$  cm<sup>-3</sup> P HDSiP sample does not follow the trend of increasing activation with increasing chemical phosphorus concentration samples. This claim can be substantiated by the observation of loops during annealing and the higher released interstitial flux recorded in the

marker layer study. Rather than concluding that the interstitials are not associated with phosphorus it is suggested that at this high concentration of phosphorus, complete dissolution of phosphorus from PICs is not possible. This is likely due to such small distances between PICs in the layer. Interstitials that get released from one PIC that do not leave the layer or fill the central vacancy of a  $P_4V$  absorb into another PIC or loop embryo.

The change in activation after DSA annealing is due to the dissolution of PICs. For HDSiP films with phosphorus concentration below  $3x10^{21}$  cm<sup>-3</sup>, near complete activation of PICs is attained. Additional self-interstitials that are produced during PIC breakup do one of three things. First, they can form into self-interstitial clusters and remain in the HDSiP layer. Second, self-interstitials may fill in the vacancy of P<sub>4</sub>V resulting in the observed decrease in PAS Sparameter observed by Dhayalan et al.[79] Third, a smaller concentration of interstitials is released into the substrate and is responsible for the enhanced diffusivity of buried phosphorus marker layers observed in this work.

### 5.4.2 Summary

From this work, it is evident that deteriorated properties result in HDSiP films with concentrations of incorporated phosphorus that exceed  $3x10^{21}$  cm<sup>-3</sup>. For the  $4.4x10^{21}$  cm<sup>-3</sup> P HDSiP sample, anomalous properties resulted that are not beneficial to device performance despite the higher tensile strain that can be obtained with more phosphorus. Degraded electrical properties, extended defect formation and unexpectedly high interstitial release into the bulk were among anomalous behaviors. These behaviors result from a higher concentration of grown-in PICs. Despite these properties, strain remained stable in the layer. For lower concentration of HDSiP films, carrier concentration reached a maximum value of  $9x10^{20}$  cm<sup>-3</sup> between 1 and  $3x10^{21}$  cm<sup>-3</sup> P. Defect free layers resulted even after a 3 minute RTO at 900 °C. Interstitial release by HDSiP and LDSiP films into the bulk was shown to decrease with increasing total

phosphorus concentration due to a higher concentration of  $P_4V$  clusters likely to be present in the layer. It is proposed that PIC breakup causes activation of HDSiP while releasing self-interstitials that may react with  $P_4V$  clusters by filling in the central vacancy. As lower concentrations of HDSiP have fewer  $P_4V$  clusters, more interstitials are released to the bulk.

# CHAPTER 6 CONCLUSIONS AND FUTURE PROSPECTS

#### **6.1 Experimental Conclusions**

#### 6.1.1 Stability of HDSiP

HDSiP that has been exposed to ms laser DSA exhibits favorable electrical properties for incorporation into transistor process flow as a source/drain selective epitaxy material. Care needs to be taken in utilizing this process for building transistors as additional thermal processes have been demonstrated to decay the level of active carrier concentration substantially. After a 60 s anneal at 700 °C, the  $2x10^{21}$  cm<sup>-3</sup> P HDSiP sample returned from its DSA activated state to the as-grown active carrier concentration. This corresponds to a change in carrier concentration from  $5.5x10^{20}$  cm<sup>-3</sup> active phosphorus to  $2.5x10^{20}$  cm<sup>-3</sup> active phosphorus. Strain stability was demonstrated during this time frame for samples of HDSiP regardless of incorporated phosphorus concentration. Microstructural stability was observed for all concentrations of HDSiP below  $4.4x10^{21}$  cm<sup>-3</sup> P HDSiP where extrinsic dislocation loops and stacking faults were observed to form upon deactivation. Processing temperatures above ~650 °C should be avoided for thermal processes after post selective epitaxial growth activation of the source/drain regions. Provided that this sort of thermal budget is acceptable for the successive process steps, HDSiP exhibits sufficient stability for incorporation into transistor process flow.

#### 6.1.2 Clustering Configurations in HDSiP

Phosphorus exists in HDSiP in three different main configurations: substitutional phosphorus, phosphorus vacancy clusters and phosphorus interstitial clusters. Substitutional phosphorus has been measured through electrical properties. This phosphorus exists in a hydrogenic nature sufficiently isolated from other dopant and defect species such that it may donate its extra electron. The quantity of phosphorus that is situated in substitutional sites has been recorded with respect to a multitude of annealing conditions as discussed above in section 6.1.1.

The second bonding environment for a fraction of the total phosphorus present in HDSiP is in clusters with a vacancy. Conventional logic dictates that the number of phosphorus atoms that decorates a single vacancy can be no more than four and that the maximum number of phosphorus that could decorate a divacancy could be no more than six. Therefore, the ratio of phosphorus atoms in vacancy clusters to total vacancies can be no greater than 4:1. In nature, phosphorus tends to make three or five bonds. By situating next to a vacancy, extra electron density of the phosphorus atom can occupy the vacancy space while the phosphorus atom exists in a low energy state bonded directly to three adjacent silicon atoms.

The PAS data obtained by Dhayalan et al. is a clear indicator that open volume defects such are P<sub>4</sub>V that are grown into HDSiP are not present in significant quantities after DSA annealing. This suggests that self-interstitials released during PIC dissolution are filling in the central vacancies of P<sub>4</sub>V creating P<sub>4</sub> substitutional clusters. It is not suggested that these P<sub>4</sub> substitutional clusters further dissolve and separate in HDSiP as this would create a state where reforming P<sub>4</sub>V would be entropically unfavorable and precipitation is likely. As the microstructure remains defect free for HDSiP concentrations below  $4.4 \times 10^{21}$  cm<sup>-3</sup> P, it is suggested that spontaneous Frenkel pair formation occurs within filled in P<sub>4</sub> substitutional clusters to re-form P<sub>4</sub>V upon deactivation. The reversibility of this reaction provides a clear mechanism for why no orthorhombic or monoclinic precipitates can be observed.

The remaining phosphorus present in HDSiP that does not exist in a substitutional state or in a PV complex exists in PICs. PICs are likely the result of collisions of diffusing PI pairs and have been the primary observed clustering type of inactive phosphorus in silicon from solid

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source diffusion as well as ion implantation. The reason for the formation of PICs in silicon doped via traditional means such as ion implantation or solid source diffusion is that these doping mechanisms both introduce phosphorus with an oversaturation of interstitial species. For HDSiP, these PICs break up to yield substitutional phosphorus and interstitials during the DSA. It is these clusters that are responsible for activation and deactivation of HDSiP.

## 6.1.3 Strain in HDSiP

Tensile strain measured for HDSiP samples is beneficial to nMOS device performance as HDSiP source/drain stressors impart tensile strain on the channel region. It is important that the strained state of HDSiP be well behaved and stable throughout the transistor process flow. Strain evolution during activating and deactivating anneals was studied and the underlying origins for tensile strain and strain evolution have been determined. During DSA annealing, HDSiP samples are exposed to high temperature for very short times. Within this process, strain increases have been reported by Li et al. for temperatures below 1250 °C.[5] This observation which takes place concurrently with significant activation can be attributed to the moving of phosphorus atoms in interstitial clusters to substitutional lattice sites. The effect of interstitial species on the lattice parameter is less than a 1% expansion predicted with DFT.[159] For species with a smaller atomic radius than the matrix, it is expected to be negligible. [160] However, the effect of substitutional species with a smaller atomic radius is not negligible. The increase in strain during DSA annealing can be attributed to the exchange of 2 - 8 x 10<sup>20</sup> cm<sup>-3</sup> phosphorus atoms from interstitial clusters to isolated substitutional sites.

There is still debate in the scientific community about whether  $P_4V$  clusters are necessary to obtain the experimentally measured strain in HDSiP. Experiments such as outlined in section 6.2.3 will be necessary for understanding the role of  $P_4V$  when it comes to strain. As it stands, strain loss can only be observed for annealing conditions where diffusion of the layer is evident

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regardless of activation level. This correlation alone suggests that strain loss may be related to phosphorus concentration by itself irrespective of bonding environment. Should it prove that  $P_4V$ clusters are responsible for strain in the layer and are thus stable throughout the thermal processes used in this work, then the interstitials released during activation must exclusively form into self-interstitial clusters instead of filling in  $P_4V$  complexes.

Phosphorus is an interesting dopant as it diffuses almost exclusively through interstitialcy means. Until recently, doping with phosphorus always incorporated an oversaturation of interstitials. Being able to introduce a dopant species concurrently with a substantial concentration of vacancies in addition to interstitials creates this unique opportunity for PV clusters to form. This same ability is what allows P incorporation well above previously established chemical solubility limits in silicon.

#### 6.2 Avenues for further investigation

Despite the important conclusions which have been obtained during this work, there are always more avenues for obtaining further understanding of a material. Given more time, resources, and funding these avenues could have been explored in more depth. Often times the experiments that get conducted are the ones that demonstrate the highest likelihood for success as well as the greatest knowledge return on investment. That being said some of these proposed methods for future investigation could be very difficult, time consuming, complex, or expensive. But as they offer potential for a future student to make breakthroughs in the characterization of HDSiP, they shall be discussed in the following sections.

## 6.2.1 Solid State NMR Analysis of Local Bonding Arrangements in HDSiP

For organic synthesis, local bonding environment of hydrogen can be easily determined through use of <sup>1</sup>H nuclear magnetic resonance spectroscopy. This type of analysis is also able to determine the number of unique bonding environments of hydrogen as well as quantify the ratio of hydrogen atoms in each of these bonding environments. For use in characterization of the bonding environment of phosphorus in HDSiP, <sup>31</sup>P solid state NMR (SSNMR) can be used to yield this same type of data. As HDSiP can only be grown into thin films on silicon before defects occur, the difficulty with this method is obtaining a sufficient quantity of HDSiP for SSNMR analysis. The benefit of conducting 31P SSNMR is that phosphorus exists exclusively as a 31P stable isotope. Despite this, methods such as growing on silicon-on-insulator (SOI) or growing strain relaxed buffer layers (SRB) may be needed to allow for the creation of a sufficiently high amount of material to warrant acceptable signal to noise ratios.

## 6.2.2 Nanosecond Pulsed Laser Activation Study of HDSiP

Different varieties of vacancy and interstitial clusters with different numbers of constituent phosphorus atoms have been proposed within this work. It may be possible to understand the relative concentrations of these clusters through an activation study with repeated pulse non-melt nanosecond laser annealing. Over several orders of magnitude of total anneal time, a material with different types of activating clusters will exhibit discrete activation steps using a nanosecond laser. There is a characteristic time associated with the dissolution of each varieties of cluster breaking up. By understanding the changes in activation with respect to increasing anneal time, further knowledge of the cluster dissolution process can be obtained.

## 6.2.3 Melt Laser Annealing Study

Melt laser annealing is essentially useless from a transistor process flow perspective but it can lend insight into material properties. Melt laser annealing has demonstrated the ability to achieve 100% activation of a  $2.3 \times 10^{21}$  cm<sup>-3</sup> P HDSiP film. Analysis of melt laser annealed HDSiP films and high phosphorus concentration ion implant samples has the potential for lending further insight into the phosphorus-silicon material system. By incorporating higher and higher concentrations of phosphorus into HDSiP films and undergoing melt recrystallization with a laser, the physical limitations to the hydrogenic nature of a dopant can be understood.

From a strain perspective, it is likely that the melt regrowth of HDSiP would essentially remove the majority of grown-in point defect species. Without the contributions of vacancy clusters on strain, high concentration of substitutional phosphorus films could be grown and analyzed with HR-XRD. Using this process, the lattice parameter contraction for phosphorus doped silicon could be determined for high phosphorus doping concentrations.

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## **BIOGRAPHICAL SKETCH**

Zachary Weinrich is a hobbyist mechanic, weightlifter, music enthusiast and reader who also has a passion for science. Born in Columbus Ohio, he attended Thomas Worthington High School where the path towards engineering started to materialize. The following years at Case Western Reserve University would further define the trend of his career towards graduate school. Due to the help of Dr. David Schiraldi, Zach was able to experience life and engineering research in Cleveland, Barcelona, Virginia and then ultimately end up in Florida. Zach came to find Dr. Kevin Jones after the professor he originally intended to work for decided to move to a different university after a few short months of arriving at the University of Florida. This change of advisor continued the path of focus from polymers to organic electronics to inorganic semiconductors. The future for Zach is to further continue this trend of exploring the various subsets of materials science as a process engineer in the front-end metals group at Intel in Portland, Oregon. In this next step he will be continuing to explore materials, explore more about the world and to finally explore what life is like after being done with 21 years of school.