

# Lateral Ge Diffusion During Oxidation of Si/SiGe Fins

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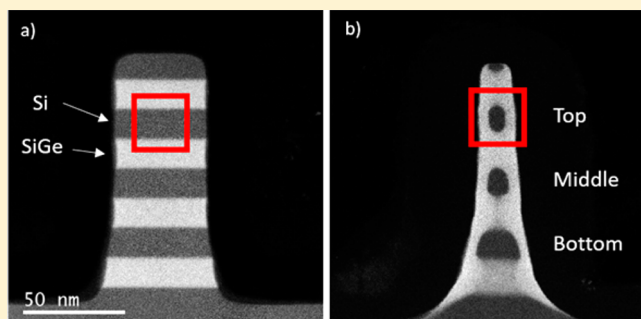
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## S Supporting Information

**ABSTRACT:** This Letter reports on the unusual diffusion behavior of Ge during oxidation of a multilayer Si/SiGe fin. It is observed that oxidation surprisingly results in the formation of vertically stacked Si nanowires encapsulated in defect free epitaxial strained  $\text{Si}_x\text{Ge}_{1-x}$ . High angle annular dark field scanning transmission electron microscopy (HAADF-STEM) shows that extremely enhanced diffusion of Ge occurs along the vertical Si/SiO<sub>2</sub> oxidizing interface and is responsible for the encapsulation process. Further oxidation fully encapsulates the Si layers in defect free single crystal  $\text{Si}_x\text{Ge}_{1-x}$  ( $x$  up to 0.53), which results in Si nanowires with up to  $-2\%$  strain. Atom probe tomography reconstructions demonstrate that the resultant nanowires run the length of the fin. We found that the oxidation temperature plays a significant role in the formation of the Si nanowires. In the process range of 800–900 °C, pure strained and rounded Si nanowires down to 2 nm in diameter can be fabricated. At lower temperatures, the Ge diffusion along the oxidizing Si/SiO<sub>2</sub> interface is slow, and rounding of the nanowire does not occur, while at higher temperatures, the diffusivity of Ge into Si is sufficient to result in dilution of the pure Si nanowire with Ge. The use of highly selective etchants to remove the SiGe could provide a new pathway for the creation of highly controlled vertically stacked nanowires for gate all around transistors.

**KEYWORDS:** SiGe oxidation, Ge condensation, silicon nanowire, gate all around transistor (GAA), interfacial diffusion, lateral diffusion



In microelectronics, there has been an increasing interest in nonplanar 3-D structures to maintain transistor scaling. The development of these devices has been motivated by the need to combat short channel effects stemming from the reduction in gate length.<sup>1,2</sup> Device architectures such as finFETs,<sup>3</sup> omega-gate,<sup>4</sup> and gate all around (GAA) transistors<sup>5</sup> have been shown to suppress these short channel effects. In particular, GAA transistors can provide superior electrostatic control over the channel region<sup>6</sup> and are currently of great interest to continue scaling down to the 5 nm node.<sup>7</sup> As the cross-sectional area of nanowires is small relative to that of a fin, multiple nanowires are generally fabricated in a stack to increase the overall drive current.<sup>8–10</sup> With improved scaling, several studies have investigated the potential of these GAA transistors for a variety of applications beyond logic and memory including solar cells<sup>11,12</sup> and sensors.<sup>13,14</sup>

Improvements to charge carrier mobility in devices can be obtained by straining the channel region.<sup>15</sup> This can be achieved in planar devices by depositing Si onto a SiGe buffer layer on a Si substrate. More recently, coherently strained Si–Si<sub>x</sub>Ge<sub>1–x</sub> core–shell nanowires have been fabricated vertically using vapor–liquid–solid growth and chemical vapor deposition techniques.<sup>16</sup> While such work shows the potential for

strained nanowires in transistors, issues with integration into current device technologies are present. If a process was developed to strain stacked horizontal nanowires down to 2 nm, improvements to device performance and scaling to smaller technology nodes would be more feasible.

When a SiGe alloy is oxidized, the oxidation potential of Si is sufficiently greater than that of Ge such that Si is preferentially oxidized and Ge is rejected, which results in a pileup of epitaxial, single crystal SiGe at the SiO<sub>2</sub>/SiGe substrate interface.<sup>17–19</sup> During this process, a Ge rich layer is formed, which continues to increase in concentration up to a value of 36–64%, which is governed by the oxidation temperature.<sup>20</sup> Once this concentration is reached, the Ge rich layer will maintain its thickness and continue to be rejected by the advancing oxide front provided there is Si below it to be oxidized<sup>21</sup> and the temperature is sufficient for the Ge to diffuse into the Si. This process has been widely investigated for use in the fabrication of Ge-on-insulator (GeOI) substrates for CMOS applications.<sup>22–27</sup>

**Received:** October 20, 2016

**Revised:** February 17, 2017

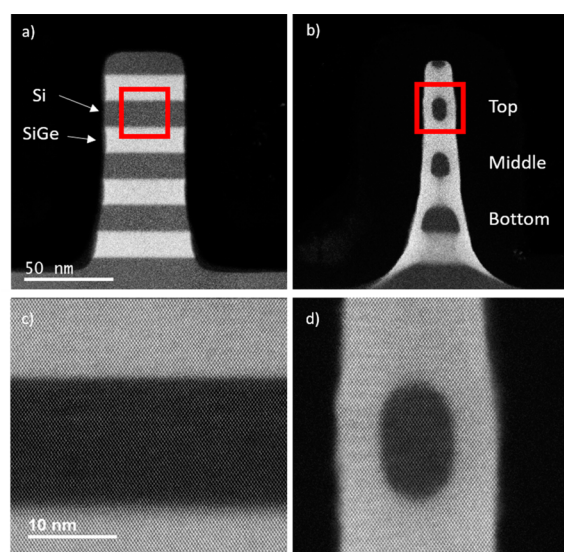
**Published:** March 1, 2017



Although previous studies on Ge condensation focused on blanket SiGe layers, no investigations on the oxidation of an interface consisting of adjacent SiGe and Si layers have been performed. Oxidation experiments have been conducted on superlattice fin structures of alternating Si and SiGe layers, offering such an interface, but did not incorporate temperature regimes in which Ge pileup would occur and instead fully oxidized the SiGe layers.<sup>28,29</sup> In this Letter, a truly unexpected observation is reported. During the oxidation of a superlattice Si/SiGe fin, enhanced Ge diffusion along the adjacent Si/SiO<sub>2</sub> interfaces was observed for the first time. Subsequently, the Si layers were effectively encapsulated in SiGe forming strained nanowires with a rounded cross-section and controllable diameters down to 2 nm. We found that a temperature process window exists in which the Si layers are encapsulated by this new interfacial Ge diffusion process without substantial interdiffusion of Ge into the Si nanowires. This process enables the fabrication of nanowires well below current lithographic limits and offers new design and optimization options for strained nanowire channels in future CMOS devices.

The initial fin structures were fabricated on commercially available 300 mm (100) Si wafers. Alternating layers of 15 nm thick Si and Si<sub>1-x</sub>Ge<sub>x</sub>, where  $x = 0.3$ , were deposited for a total of four layers each resulting in a stack height of 120 nm. Fin patterns 45 nm wide were formed in the <110> direction using photolithography and a deep reactive ion etch. Samples were analyzed with cross-sectional high angle annular dark field scanning transmission electron microscopy (HAADF-STEM) and high resolution TEM using a probe aberration-corrected JEM-ARM200CF instrument with a STEM resolution of 0.78 Å. Images were collected with a probe convergence semiangle of 22 mrad and an inner collection angle of 76 mrad. Cross-sections were prepared using a focused ion beam (FIB) system and taken orthogonal to the fin direction. A HAADF-STEM image of the Si/SiGe superlattice fin is shown in Figure 1a where the brighter areas correspond to SiGe and the darker areas to the Si layers due to the higher atomic number of Ge. A larger magnification of the alternating layers is shown in Figure 1c demonstrating that the epitaxial structure is defect free. To prevent the oxidation fronts of neighboring fins from meeting and halting further oxidation, a fin spacing of 360 nm was used. Fin oxidations were carried out in a conventional tube furnace at temperatures between 650 and 1000 °C in a flowing dry O<sub>2</sub> ambient. Prior to being placed in the furnace, samples were dipped in 6:1 buffered oxide etch (BOE) for 30 s to remove the native oxide. The grown thermal oxide was left intact for TEM analysis.

Atom probe tomography (APT) samples were prepared using an in situ FIB lift-out procedure.<sup>30,31</sup> Prior to lift out, the thermally grown oxide was removed using a 6:1 BOE solution, and a 300 nm amorphous Si layer was deposited over the fins using a PECVD process. Removal of the oxide was necessary as it has a larger evaporation field than the surrounding Si and Ge. The difference in evaporation fields could lead to artifacts in the APT reconstruction such as local magnification, out of sequence evaporation, and increased background level. Large differences can even cause fracture of the tip. To protect the fins from damage during the milling process, a strip of Pt was deposited orthogonal to the fin direction. Finally, lift-out and annular milling of the APT tips was performed. Initial milling was performed using a 30 kV beam; the final milling was done at 2 kV to limit the amount of ion beam induced damage to the specimen. These lift-out specimens were mounted to



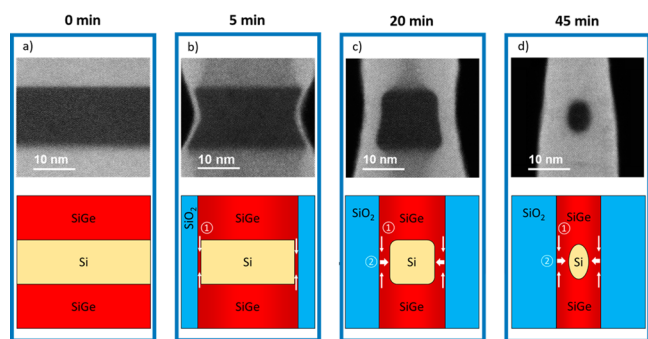
**Figure 1.** Cross-sectional HAADF-STEM images of the SiGe/Si superlattice fin structure (a) before oxidation and (b) after 40 min at 900 °C in O<sub>2</sub>. Brighter areas correspond to SiGe layers, and darker areas correspond to Si layers. The black region surrounding the fin is SiO<sub>2</sub> and protective carbon. For ease of discussion, the Si nanowires are labeled top, middle, and bottom excluding the top layer of Si as it is partially consumed by oxidation. Higher magnifications (c) before oxidation and (d) after 40 min at 900 °C in O<sub>2</sub> show no defects in the crystal structure and a rounding of the newly formed nanowires.

presharpened copper posts that were created by slicing a TEM grid in half. The holder for the grid is compatible with the FIB, TEM, and APT instrumentation.<sup>32</sup> This allowed for TEM imaging of the specimens in a Philips CM200 microscope before and after APT analysis. This aided in both the targeting of the fins and the generation of accurate APT reconstructions.

The APT analysis was performed using a local electrode atom probe (LEAP) 4000X Si from Cameca utilizing a 355 nm wavelength laser. During the run, the specimen temperature was set to 50 K, and the base pressure was 5.12e–11 Torr. To reduce the number of background counts and improve the sample yield, a detection rate (number of ions detected per laser pulse) of 0.5% was targeted and a laser energy of 40 pJ was used. APT data sets were reconstructed using Cameca's IVAS 3.6.8 program. To ensure fin dimensions in the APT reconstructions were accurate, high magnification TEM images of each tip were captured. These images were then used to create a tip profile during the 3D reconstruction process.

Cross-sectional HAADF-STEM images of an oxidized fin are shown in Figure 1b and d after oxidizing for 40 min at 900 °C. When compared to the starting fin structure in Figure 1a, the Si layers have reduced in width, and Ge has diffused around them encapsulating the newly formed Si nanowires in SiGe while remaining single crystal. This type of Ge diffusion along a Si/SiO<sub>2</sub> interface, which we will refer to as lateral diffusion, has never been reported and is critical to forming a defect free encapsulated Si nanowire.

To better study the lateral Ge diffusion around the Si layers and the formation of encapsulated Si nanowires, a time series study was performed, oxidizing the fins for 5, 10, 20, 30, 40, and 45 min at 900 °C with a dry oxygen ambient. Figure 2a–d shows the formation evolution of the Si nanowire from the starting fin structure. After 5 min (Figure 2b), Ge is present on the sides of the Si layers diffusing a distance of 7.5 nm (from

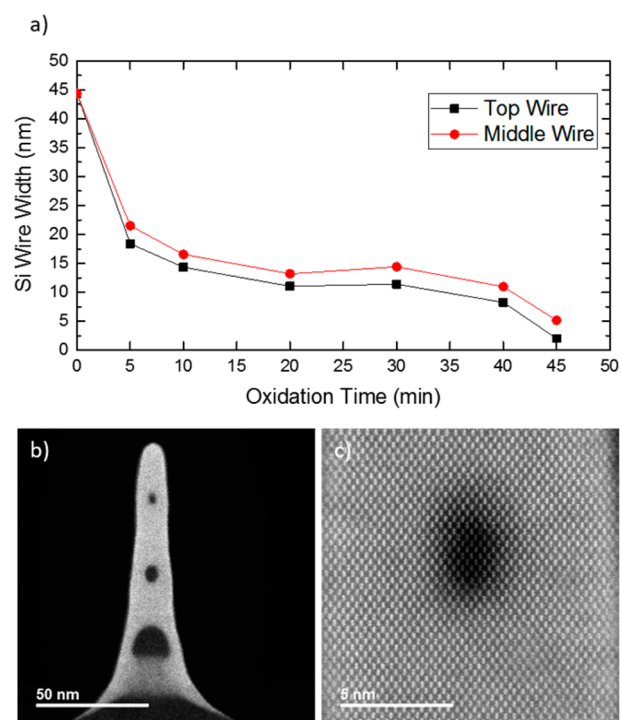


**Figure 2.** HAADF-STEM images and schematics of the middle Si layer (a) before oxidation and after oxidation at 900 °C for (b) 5 min, (c) 20 min, and (d) 45 min. The lateral diffusion of Ge along the Si/SiO<sub>2</sub> interface is indicated in the schematic by the vertical arrows labeled 1. This process initially encapsulates the Si layers illustrated in the 5 min oxidation images. As Ge continues to laterally diffuse, it is rejected by the advancing oxide front indicated by the horizontal arrows labeled 2.

each layer) with a uniform thickness of approximately 1 nm. This diffusion is at least two orders of magnitude faster than Ge diffusing a similar distance through bulk Si, which would take approximately 12.8 h (Supplementary Eqs 1 and 2). Further oxidation of the fin structure results in further shrinking of the Si layer width, and an increase in thickness of the SiGe on either side of the Si fin as Ge is rejected from the oxidizing interface (Figure 2c). As the process continues, the Si layers begin to round (Figure 2d). Schematics shown in Figure 2 illustrate these Ge diffusion processes.

The change in width of the Si nanowires with oxidation time is shown in Figure 3a where both the top and middle wire widths are presented. Initially, the nanowire width decreases in a fashion comparable to a complementary error function indicating the loss of Si exhibits Fickian behavior. Between oxidation times of 25 and 30 min, the nanowire width remains mostly unchanged. This regime marks where the nanowires begin to become rounded (Supplementary Figure 1). After 30 min, the wire thickness continues to decrease until sharply falling near the 45 min mark. This trend is analogous to spherical dissolution<sup>33</sup> and could be considered a form of cylindrical dissolution.<sup>34</sup> A minimum nanowire width of 2 nm was achieved at the top wire position after a 45 min oxidation (Figure 3b,c). Thus, size control of these nanowires is possible by tuning the oxidation time and fin geometry.

A 3D APT reconstruction of the top nanowire after a 40 min oxidation process is shown in Figure 4a. The rounded Si nanowire can clearly be observed at the center of the reconstruction with Ge present on either side (Supplementary Video 1). Figure 4b displays a 1D concentration profile through the center of the nanowire in the  $x$  direction. Peak Ge concentrations of 45% are observed in the center of the laterally diffused Ge layers, increased from effectively 0% before oxidation. These concentration values correlate well with the results of Long et al.<sup>20</sup> for SiGe oxidations at 900 °C. The decay length (defined as the distance required for a change in concentration by one order of magnitude) of Ge into the nanowire was calculated to be 1.2 nm/dec, which indicated a fairly abrupt interface between the nanowire and surrounding SiGe. Variations between the measured fin dimensions in TEM and the dimensions obtained from APT data are attributed to distortions in the reconstruction. These distortions are a result of the limitations in the reconstruction algorithm in

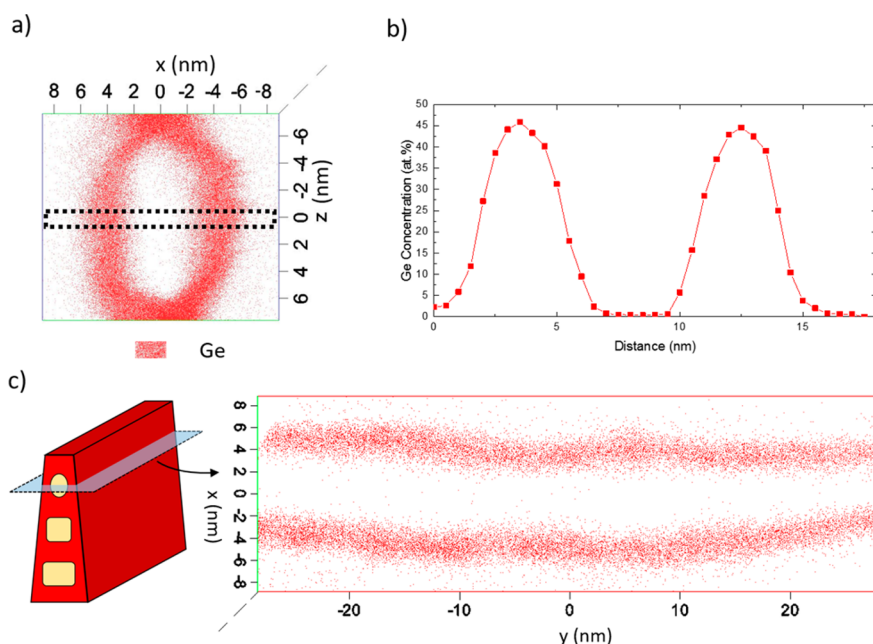


**Figure 3.** (a) Si nanowire widths plotted as a function of oxidation time for both the middle and top wire positions. Samples were oxidized at 900 °C. (b) HAADF-STEM image of a Si/SiGe superlattice fin oxidized for 45 min at 900 °C in a dry O<sub>2</sub> environment. (c) A nanowire with a diameter of 2 nm was achieved at the top wire position.

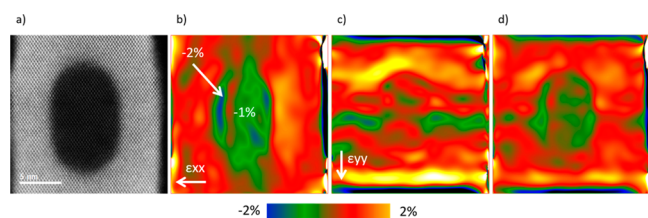
accommodating the local changes radius of the tip at SiGe layers.<sup>35</sup> However, these distortions primarily affect the dimensions of the reconstructions, not the concentrations of the species. A reconstruction cross-section down the length of the encapsulated Si nanowire (Figure 4c) demonstrates it runs the length of the fin. This further illustrates the feasibility of forming nanowires by utilizing the oxidation and lateral diffusion process.

Because of the lattice mismatch between SiGe and Si, the deposited SiGe layers are in a state of compressive strain. As Ge diffused around the Si layers during oxidation, the strain state of the newly formed Si nanowires changed. Geometric phase analysis (GPA) of atomic resolution HAADF-STEM images was utilized to quantify the strain in the oxidized samples.<sup>36</sup> The SiGe lattice below the Si wires was used as a reference for the strain calculations. Figure 5 shows strain mapping of the top wire from the 40 min oxidized sample. A maximum of  $-2\%$  strain in the  $x$  direction ( $\epsilon_{xx}$  Figure 5b) was found on the sides of the Si wire with the center showing closer to  $-1\%$  strain. Strain in the  $y$  direction ( $\epsilon_{yy}$  Figure 5c) shows some fluctuation, but the profile within the Si wire shows very little variation from the SiGe layer. A dilation of the  $\epsilon_{xx}$  and  $\epsilon_{yy}$  maps (Figure 5d) shows the Si wire is in a net tensile strain state with approximately  $-1\%$  strain. Larger  $\epsilon_{xx}$  tensile strains were observed for samples oxidized for 20 min up to  $-3\%$  (Supplementary Figure 2). Because of the shorter oxidation time, the Ge concentration on the sides of the wire was larger than the concentration above or below leading to a larger lattice mismatch in the  $x$  direction. This can be observed in Figure 2c where the Ge rich regions on either side of the Si wire have a brighter intensity than the regions above or below. (Further





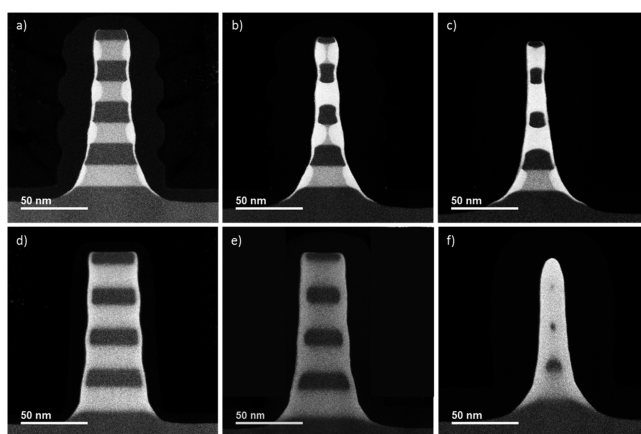
**Figure 4.** (a) Atom probe tomographic reconstruction of the top wire region from a sample oxidized for 40 min at 900 °C in a dry O<sub>2</sub> environment. Only Ge atoms are presented and are shown in red. (b) 1D Ge concentration profile taken along the dotted region in panel a. (c) A reconstructed cross-section taken down the length of the top wire shows the nanowire is continuous through the oxidized fin. Narrowing of the wire on the right side of the image is attributed to distortions in the reconstruction.



**Figure 5.** (a) Strain measurements were performed on a HAADF-STEM image using GPA software in Gatan DigitalMicrograph. Strain maps for the 40 min oxidation at 900 °C were created in the (b)  $x$  direction ( $\epsilon_{xx}$ ) and (c)  $y$  direction ( $\epsilon_{yy}$ ). A maximum  $\epsilon_{xx}$  of  $-2\%$  was calculated on the sides of the wire. (d) A dilatation, or  $D_{xy}$ , of the  $\epsilon_{xx}$  and  $\epsilon_{yy}$  shows the overall strain profile.

discussion on the strain calculations can be found in the [Supporting Information](#).)

Oxidation experiments were also carried out at 800 and 1000 °C to investigate the effect of temperature on nanowire formation. To ensure the experiments were comparable to those performed at 900 °C, equivalent oxidation times were targeted such that the thickness of the SiO<sub>2</sub> layer grown for each temperature were comparable ([Supplementary Figure 3](#)). [Figure 6](#) shows the formation of Si nanowires at 800 and 1000 °C for oxidation times comparable to 5, 20, and 40 min at 900 °C. At 800 °C, some Ge diffuses down the Si/SiO<sub>2</sub> interface encapsulating the Si layers much like the original experiments. However, continued oxidation does not increase the thickness of these Ge rich layer as the width of the fin decreases. Additionally, the Si layers no longer form into rounded wires, but into more boxlike wires similar to what was observed in previous publications.<sup>28,29</sup> Increasing the oxidation temperature to 1000 °C resulted in an increased rate of interfacial Ge diffusion relative to that of the oxidation front. This can be observed in [Figure 6e](#) where the amount of Ge diffused around the Si layer is comparable to that at 900 °C for



**Figure 6.** HAADF-STEM images of cross sections of fin samples oxidized at 800 °C for (a) 45 min, (b) 160 min, and (c) 300 min and 1000 °C for (d) 2 min, (e) 3 min 35 s, and (f) 7 min 30 s. Minimal lateral Ge diffusion around the Si layers is observed at 800 °C with no change in thickness of the Ge-rich layer after continued oxidation. After being oxidized at 1000 °C for 7 min and 30 s, the interdiffusion of Ge into the Si wires becomes apparent.

20 min but the fin width is larger for the 1000 °C sample. More importantly, because of its higher activation energy, the rate of diffusion of Ge into the Si wire increases more than the oxidation rate and leads to interdiffusion at the Si/SiGe nanowire interface. This interdiffusion is apparent in [Figure 6f](#) and would result in a roughening of the Si wire postetch and potentially limit electron mobility.<sup>37</sup>

These temperature studies indicate there are competing activation energies of several diffusion processes during the Ge encapsulation process. At low temperatures, the oxidation of Si and SiGe is dominant over the lateral diffusion of Ge along the oxidizing Si interface as well as the interdiffusion of Ge into Si, leading to limited encapsulation of the Si layers. Segregation of

Ge clusters into the growing oxide was even observed during oxidation experiments at 650 °C (Supplementary Figure 4). However, at higher temperatures, while the rate of lateral Ge diffusion increases, Ge interdiffusion into Si also increases, which results in poorly defined Si nanowires. This leads to a process window in which the combination of thermal oxidation, Ge segregation, and lateral Ge diffusion along the interface can occur without Ge interdiffusion, leading to controllable fabrication of Si nanowires of variable dimensions.

As previously stated, the estimated rate of this lateral Ge diffusion is at least two orders of magnitude faster than bulk diffusion of Ge through crystalline Si. This high diffusivity suggests an alternative diffusion mechanism to traditional interstitial and substitutional diffusion of Ge in Si. It is suggested that the diffusion process may depend on a redox enhanced diffusion (RED) reaction at the interface. It is possible Ge atoms are initially oxidized at the oxidizing interface forming GeO bonds and then reduced by Si in the lattice. As there is a larger net concentration of Si in the Si rich layers than in the SiGe layers, reduction of GeO by Si in the Si layers would result in apparent lateral diffusion. This process would repeat until the Si layer was effectively encapsulated in a thin SiGe layer. Such an oxidation and reduction process has been observed in Ge nanocrystals<sup>38</sup> and modeled for blanket oxidation.<sup>39</sup> Further oxidation and inert ambient experiments will need to be performed to determine if a RED mechanism can explain the observed diffusion.

We have shown a novel method to fabricate horizontally stacked strained Si nanowires via the oxidation of Si/SiGe superlattice fin structures. During this process, it was found that Ge diffused along the Si/SiO<sub>2</sub> interface and was subsequently rejected by the advancing oxide front. Such a process has never been reported. Further oxidation of the structure consumed the Si layers during Ge pileup forming rounded Si nanowires. Size control of these nanowires, even down to 2 nm, was achieved by tuning the oxidation time. Because of the lattice mismatch between the Si and surrounding SiGe, the resulting encapsulated Si nanowires also showed biaxial strain up to −2%. Furthermore, we have concluded that there is a temperature process window in which significant lateral Ge diffusion occurs without the interdiffusion of Ge into the Si nanowires. These nanowires have the potential to be implemented in strained CMOS devices or in more conventional nanowire transistors where the SiGe is selectively etched away. While this lateral Ge diffusion process was observed during the formation of strained Si nanowires, we believe its applications are more far reaching than what has been presented. Such a process that forms defect free epitaxial heterostructures can be applied to the fabrication of devices that would otherwise be difficult to obtain using conventional methods. This includes extremely small Hall sensor arrays formed by crossed nanowires, strained Si quantum dots, and air gap transistors.

## ■ ASSOCIATED CONTENT

### ● Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acs.nanolett.6b04407.

Diffusion time calculations, additional HAADF-STEM images, strain maps, bright field images for temperature studies (PDF)

3D atom probe tomography reconstruction video (AVI)

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### Author Contributions

W.M.B. performed mid and high temp oxidations and prepared samples for TEM and APT analysis. V.Q.T. performed low temp oxidations. C.H. provided the materials for this work. Y.X. provided the HAADF-STEM images and performed the strain calculations. D.D. and W.M.B. performed the APT analysis. W.M.B. and K.S.J. cowrote the manuscript. All authors discussed the results and commented on the manuscript.

### Notes

The authors declare the following competing financial interest(s): This work is funded through a research grant by Applied Materials. Authors W. M. Brewer, V. Q. Truong, and K. S. Jones have received research grants from Applied Materials, Inc., and K. S. Jones has consulted for Applied Materials. C. Hatem is an employee of Applied Materials.

## ■ ACKNOWLEDGMENTS

This work is funded through a research grant by Applied Materials. The authors thank the Major Analytical Instrumentation Center at the University of Florida for use of the focused ion beam and transmission electron microscope facilities and thank the Atom Probe Tomography Laboratory at Colorado School of Mines for use of the local electrode atom probe. The transmission electron microscope facility at Florida State University is funded and supported by the FSU Research Foundation, and the National High Magnetic Field Laboratory, supported by the National Science Foundation Cooperative Agreement DMR-1157490, and the State of Florida.

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