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CHARACTERIZATION OF THE PHOSPHOR LAYER MICROSTRUCTURE AND ITS EFFECTS ON THE ELECTROLUMINESCENT PROPERTIES OF THIN-FILM ELECTROLUMINESCENT DEVICES

By

ANANTH NAMAN

A DISSERTATION PRESENTED TO THE GRADUATE SCHOOL
OF THE UNIVERSITY OF FLORIDA IN PARTIAL FULFILLMENT
OF THE REQUIREMENTS FOR THE DEGREE OF
DOCTOR OF PHILOSOPHY

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1997

To My Parents,
whose love and encouragement can never be measured
and who forever will be my heroes

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I would like to take this space to express my sincere thanks to the individuals who have assisted me during my stay at the University of Florida. Without their guidance and encouragement, my experiences would have been hollow.

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"... in all kinds of weather, we will all stick together for F L O R I D A."

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CHARACTERIZATION OF THE PHOSPHOR LAYER MICROSTRUCTURE AND ITS EFFECTS ON THE ELECTROLUMINESCENT PROPERTIES OF THIN-FILM ELECTROLUMINESCENT DEVICES

By

Ananth Naman

December, 1997

Chairman: Kevin S. Jones
Cochairman: Paul H. Holloway
Major Department: Materials Science and Engineering

The objective of this study was to investigate the effect of post deposition annealing and of gallium and excess sulfur additions on the microstructural properties of SrS:Ce electroluminescent (EL) thin films and relate these effects to the electroluminescent properties of the thin film electroluminescent (TFEL) device.

SrS:Ce films were prepared by rf-magnetron sputtering of SrS:Ce (0.12 mol.%) targets at substrate temperatures between 200 and 450°C. The deposited films were annealed at temperatures between 650°C and 810°C in a nitrogen atmosphere. Post deposition annealing of as-deposited SrS:Ce phosphor thin films resulted in improved TFEL device properties, namely decreases in threshold voltage accompanied by increases in brightness, at forty volts above the threshold voltage, and luminous efficiency.

Microstructural characterization revealed an increased SrS:Ce grain size and decreased x-ray peak full width half maximum. These two results in combination suggest an overall improvement in crystal quality with increasing annealing temperatures. Characterization via electron paramagnetic resonance and photoluminescent spectroscopy indicated that post deposition annealing led to a better Ce^{3+} crystal field which in turn resulted in better luminescent properties.

Gallium and excess sulfur were added to the SrS:Ce films in hopes of improving the EL properties. Post deposition annealing at 810°C of the TFEL devices containing SrS:Ce phosphor films with gallium and excess sulfur resulted in enhanced EL performance compared with the SrS:Ce films annealed at 810°C: five-fold increase in brightness and six-fold increase in luminous efficiency. Microstructural characterization showed that as deposited microstructure was the same as that on the SrS:Ce films. However, annealing at 810°C resulted in a transformation to a equiaxed grain morphology with a mean grain size of 5000Å. The dramatic increase in the grain size was attributed to liquid phase assisted grain growth. The significant increase in the EL properties was attributed to a combination of increased scattering of the generated light, a decreased number of non-radiative decay traps and less self absorption by defects.

CHAPTER 1
INTRODUCTION

Background and Motivation

Revolutionary advances in solid state electronics have helped usher in the information age we live in today. The advances have led not only to faster, smaller and more powerful microprocessors but have also spurred the development of complimentary technologies. One such area is displays, which are the windows to this information age. The continuous push towards the miniaturization of solid state electronics, coupled with the need for instant information, has contributed to the soaring demand for flat panel displays (FPDs), with total sales doubling from $50 billion in 1995 to $100 billion in 1997 and projected to be $210 billion by the year 2000 [Wer97].

The flat panel display industry manufactures displays utilizing various technologies for innumerable applications. Technologies include liquid crystal displays (LCDs), light emitting diodes (LEDs), plasma displays, field-emission displays (FEDs) and electroluminescent displays (ELDs). Applications range from alarm clocks to wrist watches, from virtual reality avionics to dashboard mounted screens for automobile navigation systems, from electronic clipboards to the virtual reality display products used in the entertainment industry. For market acceptance, displays used for large information content applications (computer monitors, televisions, etc.) must meet the basic performance standards of traditional cathode ray tube displays in the areas of brightness,

contrast, resolution, and color gamut. Additionally, FPDs must offer the added benefits of space efficiency, low weight, and low power consumption. In 1997, the expected market FPDs used for large content applications is estimated to be $15 billion dollars, up 300% from 1995 [Wer97].

From an operational point of view, FPDs can generally be divided into two categories: non-emissive and emissive displays. Non-emissive displays utilize a back light and use an array of filters and shutters to define a pixel. The most common non-emissive devices are liquid crystal displays (LCDs). In these devices, organic molecules known as liquid crystals act as the shutters. The shutters are opened and closed via application of an electric field, which results in the alignment of the liquid crystals. LCDs are the dominant flat panel display technology accounting for approximately 90% of the market. However, due to their organic composition, LCDs suffer from many inherent disadvantages: poor brightness in daylight conditions, limited viewing angle and limited operational temperature regime.

Emissive displays include field emission displays, plasma displays and electroluminescent displays. Electroluminescent displays are currently the most prevalent emissive displays. Generally, the individual pixels in an emissive display emit light when stimulated rather than transmitting and filtering light as occurs in the case of a non-emissive display. Due to the solid-state design, ELDs are extremely rugged and can withstand a broader operational temperature range compared with LCDs. While there is significant market acceptance of ELDs ($720 million/yr.), further growth of ELD market share is limited by two factors: insufficient color gamut and high manufacture cost. Development in display phosphor technology is critical in overcoming both limitations.

Phosphors are materials that convert energy into light. In the case of electroluminescence, the energy source is an electric field. While phosphor technology has developed efficient red (ZnS:Mn) [Tue91] and green (ZnS:Tb) [Ohn85] phosphors, the focus of the current research is on the development of an efficient blue phosphor, which is essential in the production of a full color display. Currently, the state of thin film electroluminescent (TFEL) technology is lacking a suitable high-brightness blue phosphor. Without improvements in this area, an acceptable color gamut can not be achieved. Additionally, optimization of thin film phosphors requires annealing at temperatures exceeding 800°C. These processing temperatures require the use of expensive glass-ceramic substrates to avoid warping. The substrate can account for as much as 40% of the total manufacturing cost of a TFEL display.

Research Objective

A wide range of materials, including strontium sulfide with cerium doping (SrS:Ce), have been investigated as possible blue EL phosphors with limited success [Bar84],[Tan85],[Oka93]. Past research in SrS:Ce and other phosphors has shown a possible correlation between phosphor thin film microstructure and the optical/electrical properties of the TFEL device. The addition of gallium and excess sulfur has been found to significantly improve the electroluminescent properties of SrS:Ce TFEL displays, but the reasons for this improvement were not determined [Sun96]. Preliminary results indicated that this system provided an opportunity to study the effects of the phosphor layer microstructure on TFEL device performance. The objective of this research was

twofold: 1) investigate the effect of Ga_2S_3 additions on the microstructure of SrS:Ce, and 2) determine any correlations between changes in phosphor layer microstructure and improvements in the electroluminescent properties in the SrS:Ce containing Ga_2S_3 TFEL devices.

Dissertation Outline

A review of the concepts and terms germain to this study is provided in chapter two. This review includes the milestones in the development of EL device technology as well as the fundamentals of the TFEL device physics. The important EL properties used to evaluate device performance are also reviewed. The desired property requirements of the phosphor layer are presented followed by a review of the results from previous research conducted on the SrS:Ce TFEL phosphor system. Finally, a brief section is presented focussing on sputter deposition of thin films and thin film microstructural development. The experimental plan and the methods and materials used in this study are given in chapter three.

The results of the effect of post deposition annealing on the device properties of SrS:Ce TFEL devices are presented in chapter four. Electrical and optical characterization of the TFEL device as well as microstructural characterization of the phosphor layer were performed. These experiments were designed to help better understand the microstructural evolution of the SrS host matrix as a function of annealing temperature and were used to determine the effect of phosphor layer microstructure on the TFEL device properties.

Chapter five reports the effects of adding gallium and excess sulfur to the SrS:Ce phosphor layer. TFEL device properties and phosphor layer microstructure as a function of post deposition annealing temperature were studied. The results of electrical and optical characterization of the TFEL device as well as microstructural characterization of the phosphor layer are given. The changes in microstructure, as a result of the addition of gallium and excess sulfur to the phosphor layer, are explained. The improved TFEL device performance is correlated to the observed changes in the microstructure of the phosphor layer. The conclusions from this study as well as suggestions for future work are presented in chapter six.

CHAPTER 2
LITERATURE REVIEW

Introduction

Development of a bright blue phosphor is the main challenge facing electroluminescent display manufacturers [Rac96]. Crucial to achieving this goal is a better understanding of how the phosphor layer microstructure affects its electroluminescent properties. This chapter will provide an overview of some of the important concepts pertaining to TFEL devices, TFEL phosphors and microstructural evolution in thin films. The chapter begins with a brief review of the history of electroluminescent technology and is followed by a discussion of device properties, specifically, device architecture, device physics and the critical parameters used to evaluate TFEL device performance. Next, some important property requirements of the candidate phosphor layer materials will be presented followed by a presentation of past work on SrS:Ce phosphors. Microstructural development, more specifically, grain growth in thin films will be discussed. Finally, a brief review of the past work performed on the thiogallate phosphor system will be presented.

History of Electroluminescent Devices

Electroluminescence is a phenomena in which electrical energy is converted to luminous energy without the generation of thermal energy. Milestones in electroluminescence phenomena date back to the 1920s. Important but often overlooked experiments by Gudden and Pohl first demonstrated the effect of an electric field in the photoluminescent decay of a ZnS:Cu phosphor [Gud29]. Georges Destriau's observation of light emission from a suspension consisting of ZnS:Cu and oil in 1936 is often cited as the first published report concerning the phenomena of electroluminescence [Des36]. Further research in the field was not reported until the early 1950's when the GTE Sylvania laboratories received a patent for an electroluminescent (EL) powder lamp [Tana85].

Early research in ELDs, which concentrated on a powder phosphor as the light generation material, was driven by the need to develop brighter, longer-lifetime lighting sources having minimal power requirements. This research was soon abandoned when it was determined that the phosphors being investigated were unable to provide adequate sustained brightness over commercially acceptable lifetimes (500 hours). The next decade saw a revival of EL research, this time focusing on display technologies. One of the first AC thin film dot matrix displays was unveiled in 1965 by Sigmatron. This was followed by a sunlight readable numeric display in 1968 [Cas92]. However, this venture did not result in a commercially viable product. Vecht demonstrated in 1968 the first DC-driven EL panel [Vec68]. During a time of heightened interest in thin film processes, Soxman

and Ketchpel reported the fabrication of devices having acceptable brightness, lifetimes and the ability to be multiplexed. However, these devices failed to demonstrate acceptable reliability [Sox72].

Research in EL reached a milestone when Inoguchi et al. (Sharp Corporation) introduced an AC thin film electroluminescent (ACTFEL) device structure in 1974 [Ino74]. The key to the investigators approach was the concept put forward by Russ and Kennedy [Rus67] describing a three layer sandwich design (insulator/phosphor/insulator). The team of researchers at Sharp fabricated a device modeled after a capacitor using manganese activated zinc sulfide (ZnS:Mn) as the phosphor and yttrium oxide (Y_2O_3) as the surrounding insulators. Inoguchi et al. were the first to demonstrate a high brightness long-lifetime device. The results demonstrated the viability of the thin film electroluminescence (TFEL) approach as compared with the traditional powder EL approach. Sharp Corp. succeeded in the development of TFEL technology and introduced a monochrome television display in 1978, which employed TFEL technology. Soon after, multi-colored displays were reported by Coovert et al. [Coo82] at Planar Systems and by 1993, Planar Systems had introduced a color TFEL device [Bar93].

TFEL Device Related Issues

This section begins with a description of TFEL device architecture and the constituent materials and will be followed by a summary of the device physics. Lastly, the important electrical and optical properties that are used to evaluate TFEL devices will be discussed.

Device Architecture

Typical TFEL devices consist of a phosphor layer sandwiched between two dielectric layers which in turn are sandwiched between two conductive layers [Kin96]. This structure, shown in Figure 2-1, is referred to as a MISIM structure (Metal-Insulator-Semiconductor-Insulator-Metal). In the conventional device, the MISIM structure is grown on a transparent substrate, but some devices employ an inverted structure which allows for the MISIM sandwich to be grown on a non-transparent material (e.g. alumina, silicon). The most common material used for the bottom transparent electrode is In_2O_3:SnO_2 (ITO). The thickness of this layer ranges from 0.2 to 0.3 μm.

The dielectric layers must meet the requirement of having a high dielectric constant and electric field breakdown strength in order to allow for the high electric fields required for the ballistic acceleration of the electrons, which tunnel through the dielectric layer and into the phosphor layer [Mac91]. In the conventional device, the bottom dielectric and electrode layers must be transparent to the generated light since the light generated in the phosphor layer is transmitted through both the layers.

Lastly, some phosphors require the need for a high temperature deposition or post depositions anneal in order to optimize the phosphor properties. This requires that the substrate material, the bottom electrode layer and the bottom dielectric layer have to be stable at the high processing temperatures (>700 °C).

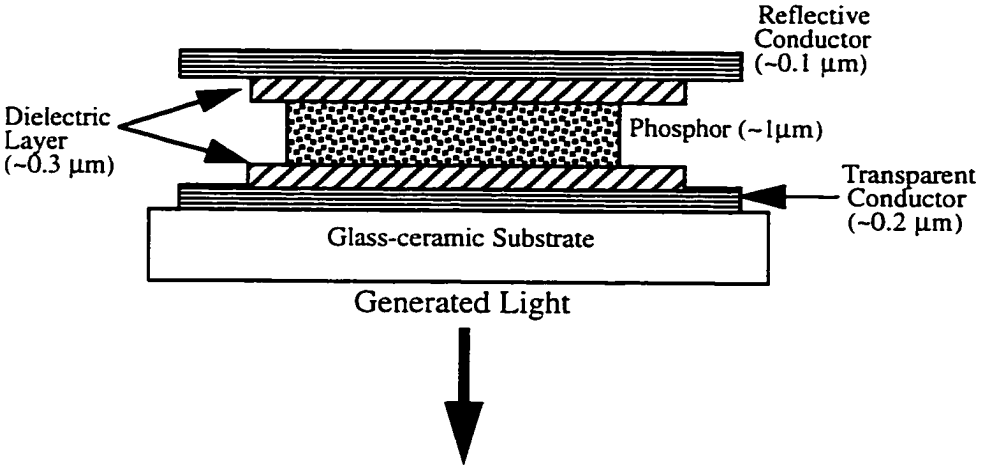


Figure 2-1. Schematic of a standard TFEL device

The phosphor layer thickness varies from 0.5 to 1.5 μm. Depending on the deposition technique and phosphor system, a high temperature anneal may follow in order to optimize the crystal quality of the phosphor layer.

The top dielectric can be of a different composition than the bottom dielectric, since it does not need to meet the high temperature requirements. Typically, the top electrode is aluminum due to its low resistivity.

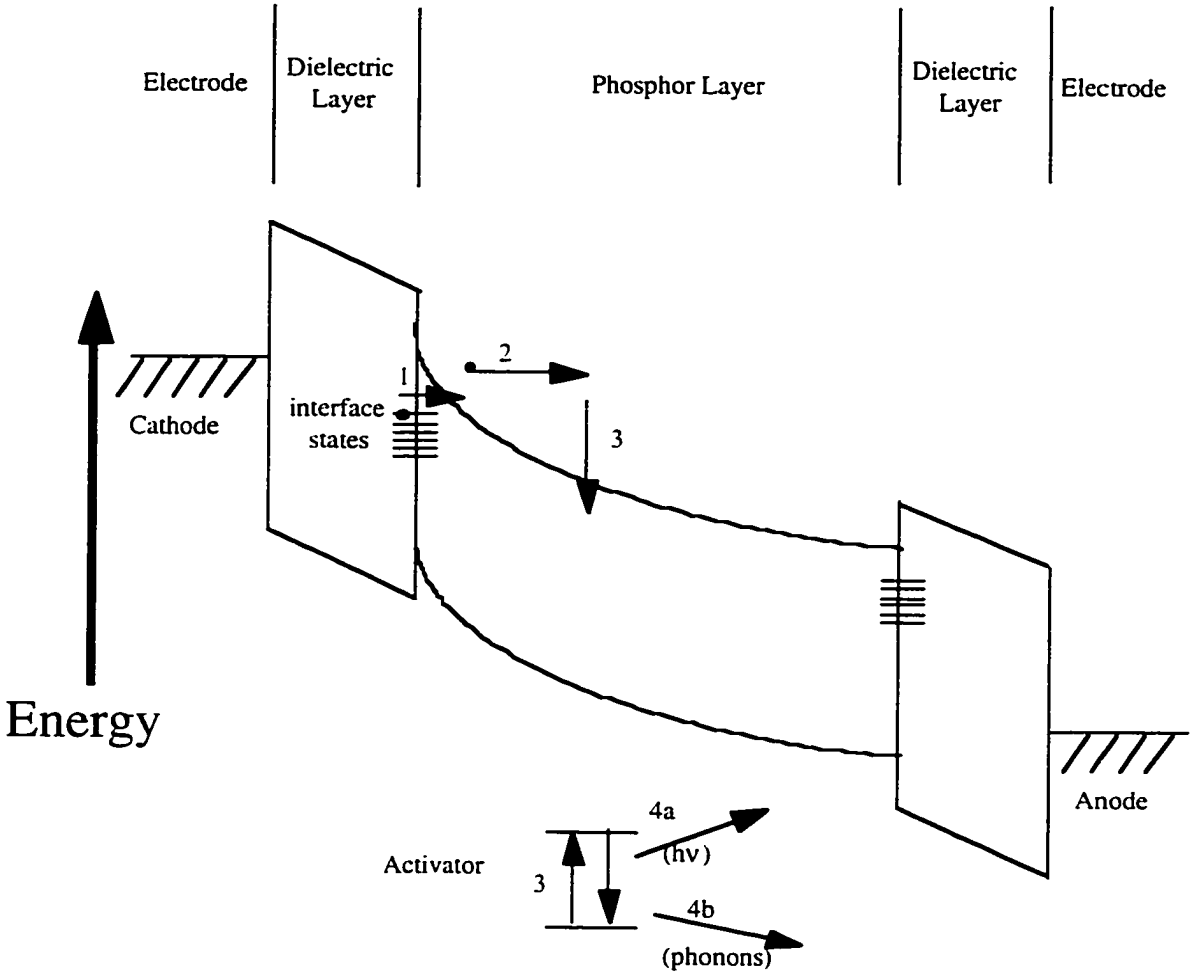
A survey of the most common materials that are used in the fabrication of commercially manufactured TFEL devices is given by Rack [Rac97]. Many deposition techniques are utilized to deposit the layers that constitute a TFEL display including evaporation, rf-sputtering and chemical vapor deposition. The critical requirement of any technique is the production of films with excellent stoichiometry and optimized crystallinity. For further information, an excellent review of electroluminescence is provided by Ono in the Encyclopedia of Applied Physics, Vol.5 [Ono92].

Device Physics

The mechanism for light generation in TFEL devices occurs in four steps [Mac91]: 1) tunnel emission of electrons from the interface states between the phosphor and dielectric layers at a threshold voltage, 2) ballistic acceleration of electrons through the phosphor layer, 3) impact ionization or excitation of the luminescent centers located in the phosphor layer and 4) de-excitation of the excited electrons of the luminescent center via radiative or non-radiative relaxation. A schematic of the model proposed by Mach et al. is illustrated in Figure 2-2.

Tunneling from interface states is primarily responsible for the injection of electrons into the phosphor layer [Mac82]. The same applied electric field (2 MV/cm) responsible for the tunneling is responsible for the ballistic acceleration of the electrons within the phosphor layer. Once the electrons have reached sufficient velocities, an interaction between the luminescent center ions located in the phosphor layer and the electron can result in either impact ionization or impact excitation.

In the case of impact ionization, the accelerated electron ionizes the ground state electron of the luminescent center into the conduction band of the phosphor material. Under high fields, these electrons are driven towards the electrodes resulting in extremely low probabilities for electron-hole recombination and subsequent light emission. Depending on the phosphor system, impact excitation is a more efficient light generating mechanism in high field devices (SrS:Ce) [Hut95]. Impact excitation causes the ground state electron of the luminescent center to be excited to a higher electronic state. Relaxation from this higher energy level can result in the generation of light.



1- Injection of electrons from interface states into phosphor layer via tunneling
2- Ballistic acceleration under high electric fields (1MV/cm)
3- Impact excitation of luminescent center resulting in transition to excited states
4- Relaxation from excited state resulting in either:
   a) Light generation (radiative emission)
   b) heat (non-radiative emission)

Figure 2-2. Schematic energy band diagram of the TFEL device and EL emission mechanism

The de-excitation process can occur either non-radiatively or radiatively. The non-radiative process involves the generation of phonons to account for the electron energy level drop from the excited state to the ground state. The radiative decay process results in the generation of a photon having a wavelength corresponding to the energy difference between the excited and ground states.

The equivalent circuit of this device is shown in Figure 2-3 [Alt84]. The capacitance of the dielectric layers are represented by C_i^1 and C_i^2 and the phosphor layer capacitance is represented by C_p. The phosphor capacitance is shunted by two back to back Zener diodes which are used to account for conduction and field clamping in the phosphor layer [Kin96]. Below the threshold voltage, both the insulators and the phosphor can be treated as pure capacitors. Above threshold, a current passes through the phosphor layer.

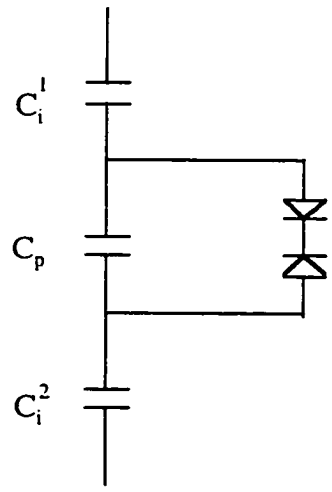


Figure 2-3. Equivalent circuit diagram for a TFEL device

The luminance and voltage characteristics as a function of time of a typical TFEL device are shown in Figure 2-4. The steep voltage versus time behavior results in virtually instant light generation when the threshold voltage is applied. This results in the corresponding luminance behavior. The lack of long turn-on time in combination with a short luminescent decay time allow for rapid addressing of the device, otherwise known as high multiplexing ratios [Kin95].

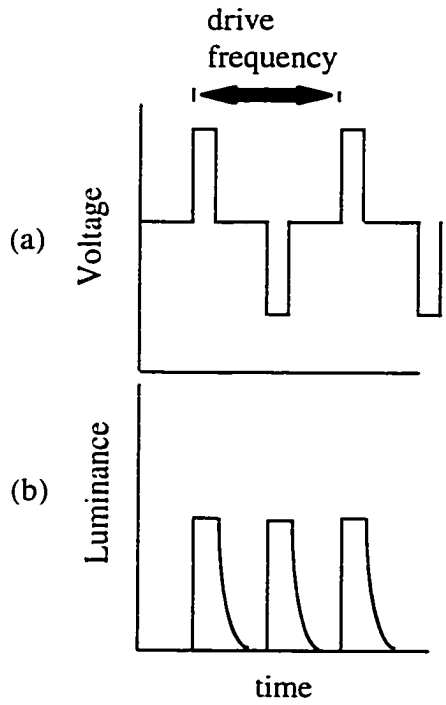


Figure 2-4. The luminance (a) and voltage (b) characteristics as a function of time for a TFEL device [Kin95]

TFEL Device Properties

Electrical and optical characterization are critical in order to effectively evaluate the performance of a TFEL device. The following section briefly describes four important measurable electrical and optical properties of TFEL devices: threshold voltage, brightness, electrical and optical efficiencies and chromaticity.

Threshold Voltage

The applied voltage is divided across the individual phosphor layers according to equation 2.1 [Rac96]. The threshold voltage is defined to be the minimum applied voltage at which the generated electric field results in the onset of Zener breakdown of the phosphor layer. A consequence of Zener breakdown is the generation of light. This leads to one definition for the threshold voltage, namely, the voltage at which the brightness of the device reaches a level of 1 cd/m^2. It should be noted that another definition for the threshold voltage is discussed in the next section. While this brightness level hardly constitutes an acceptable level for commercially viable devices, it does serve as a starting point for evaluating TFEL phosphors. From a practical perspective, it is desirable to minimize the value of the threshold voltage. Among other advantages, this allows for less complex drive circuitry and lower total power consumption.

$$V = E_1 d_t + E_2 d_b + E_3 d_p \qquad (2.1)$$

V = applied voltage

E_1 = electric field in the top dielectric — E_2 = electric field in the bottom dielectric

E_3 = electric field in the phosphor layer — d_t = thickness of top dielectric layer

d_b = thickness of bottom dielectric layer — d_p = thickness of phosphor layer

Brightness

The brightness, or luminance, of a TFEL device can be approximated by equation 2.2 [Alt84]. For any particular device the efficiency (η_p) and capacitance (C) and threshold voltage are inherent device properties. Therefore, from equation 2.2, the brightness of a particular device can only be increased by increasing the voltage or the drive frequency.

$$B(V) = 2f\,\eta_p \times \left(\frac{C_i^2}{(C_i + C_s)}\right) \times V_{th} \qquad (2.2)$$

B(V) = voltage dependent brightness

f = drive frequency — η_p = photometric efficiency

C_i = capacitance of the dielectric layer — C_s = capacitance of phosphor layer

V_{th} = threshold voltage — V = applied voltage

This becomes important when comparing brightness values of other candidate TFEL phosphors, since it will be necessary to ensure that the devices being compared are operated at equivalent conditions. The luminance at 40 volts above threshold (L_{40}) is the most common way to characterize the brightness of a TFEL device. As seen in Figure 2-

5, the luminance versus voltage characteristic is non-linear at applied voltages below the V_{th}. At applied voltages well above the V_{th}, the brightness is seen to saturate. Equation 2.2 describes the brightness in the linear portion of the brightness-voltage curve shown in Figure 2-5. As seen in Figure 2-5, the extrapolation of the line describing the linear behavior between brightness and voltage to the voltage axis is another way of defining the threshold voltage.

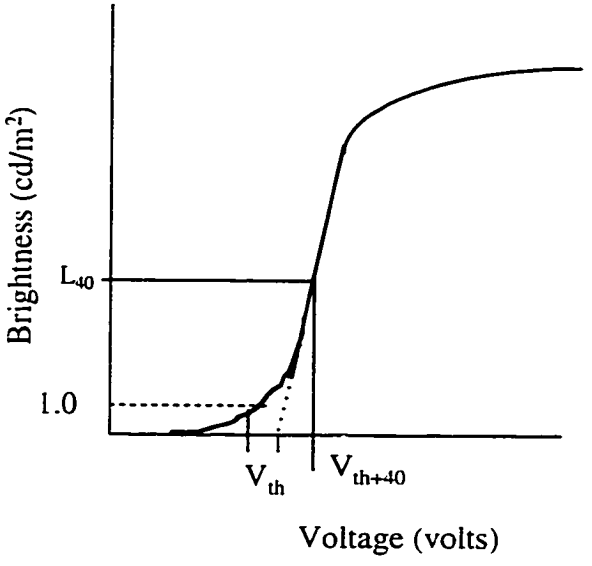


Figure 2-5. Brightness as a function of voltage for a TFEL device.

Efficiencies

From a device physics perspective, the energy efficiency (η_e) is defined as the number of photons generated per electron transferred over a unit thickness of phosphor. Using this definition for the energy efficiency, the electroluminescence efficiency (η), can be defined as the following [Mac91]:

$$\eta = \frac{\eta_e e F}{E_{phot}} \qquad (2.3)$$

η = electroluminescence efficiency

η_e = energy efficiency

E_{phot} = photon energy

e = charge of an electron

F = clamped field in the phosphor layer

The electroluminescence efficiency is composed of external (η_{out}) and internal efficiencies ($\eta_{internal}$). In other words, not all of the generated light is transmitted through the bottom glass substrate. However, unless an integrating sphere is used, only the light that is transmitted through the bottom glass substrate is measured in typical brightness measurements. Since the index of refraction of the phosphor is typically larger than that of the dielectric layers, a significant portion of the light generated is wave guided to the sides of the device rather than transmitted out through the glass substrate. The outcoupling efficiency is defined as the amount of light penetrating through the bottom surface divided by the total amount of light generated in the phosphor layer. For ZnS:Mn devices the outcoupling efficiency is calculated to be only 10% [Mac91].

The internal efficiency of a TFEL device is described by equation 2.4 [Mac91]. In this equation, the fraction of tunneled electrons hot enough to cause impact excitation is a complicated function of many scattering processes and is highly dependent on the energy band properties of the host material [Rac97]. As stated earlier, light emission in these devices originates from the radiative decay of luminescent centers.

$$\eta_{internal} = \eta_{not} \times \eta_{exc} \times \eta_{lum} \qquad (2.4)$$

$\eta_{internal}$ = internal electroluminescence efficiency

η_{hot} = fraction of tunneled electrons hot enough to cause impact excitation

η_{exc} = fraction of centers that undergo impact excitation

η_{lum} = fraction of electrons excited to a higher energy level undergoing radiative decay

The excitation efficiency is defined as the fraction of centers which undergo impact excitation. It is dependent on the crystal quality surrounding the luminescent center. Enhanced crystal quality of the host is critical to optimize excitation efficiencies.

De-excitation of a luminescent center does not necessarily result in radiative emission. As stated earlier, the excited electron can return to its ground state via one of two general processes: radiative or non-radiative decay. One of the most detrimental factors affecting the luminescent efficiency is temperature. Increased temperatures can promote the non-radiative transition to the ground state via excess phonon generation commonly referred to as thermal quenching. Another factor that influences the luminous efficiency is the luminescent center concentration. It is possible that high luminescent center concentrations will result in interactions among the centers themselves, a process referred to as concentration quenching. In this scenario, energy from the excited state of one center may be transferred to a neighboring center where it can radiatively or non-radiatively decay. The chances of non-radiative decay are greater in this scenario. The neighboring center is said to have quenched the decay: this quenching is only possible when the two centers are close enough to allow energy transfer between them, a condition that is satisfied when luminescent center concentrations are high. Lastly, radiative decay can result from the absorption of the emitted photon by defects within the phosphor

layer [Paw90]. These defects can result in unoccupied states within the bandgap of the host resulting in absorption.

As described above, the overall efficiency of a TFEL device is a complex property dependent on the product of many probabilities. For this study, the luminous efficiency is measured. The luminous efficiency is a ratio of the power out and the power in. The power out is measured by the brightness in lumens and the power in is the electrical power supplied to the device.

Chromaticity

The chromaticity, i.e. color, of the emission from a TFEL device is one of the most critical properties from a design perspective. Emission from a device is characterized on a chromaticity chart introduced by the Commission Internationale de l'Eclairage in 1931 and shown in Figure 2-6. Using this chart, any color seen by the average human eye can be specified by a pair of x and y coordinates [Kel96]. The determination of the coordinates for a particular emission are based on three sets of tristimulus functions (X,Y,Z). These values constitute spectral sensitivity curves that simulate the sensitivity of the average human eye receptors to red, green and blue light (Figure 2-7). The x and y coordinates are determined by equations 2.5 and 2.6. The color gamut is defined as all the colors that can be achieved by the three primary colors of a particular set of phosphors. The color gamut is determined by plotting the coordinates (x,y) of the three primary colors on the chromaticity chart [Kel96].

$$x = X/X+Y+Z \quad (2.5)$$

$$y = Y/X+Y+Z \quad (2.6)$$

x = value of x-axis coordinate on the 1931 CIE chromaticity chart

y = value of x-axis coordinate on the 1931 CIE chromaticity chart

X,Y,Z = tristimulus function values for a particular emission wavelength

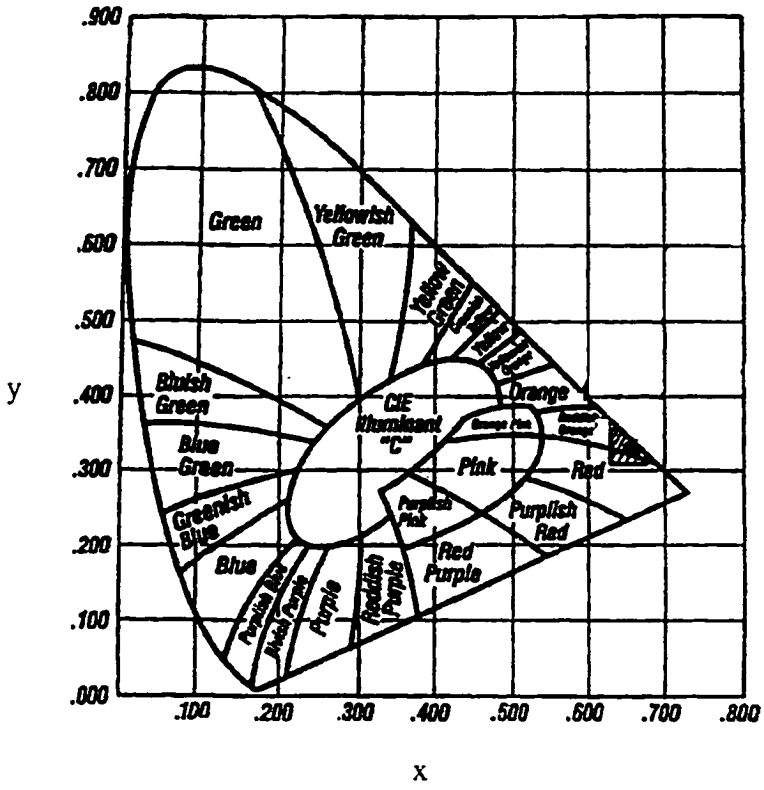


Figure 2-6. The 1931 CIE chromaticity chart

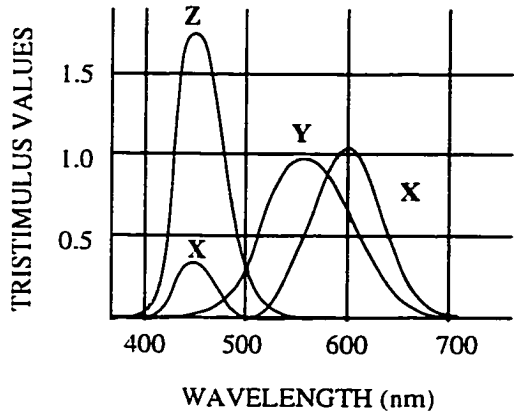


Figure 2-7. Spectral response of the tristimulus functions

In summary, the performance of TFEL devices is evaluated on its electrical and optical properties. It is clear that the ideal device should have a low threshold voltage, with maximized brightness and the desired chromaticity. The next section will address materials issues related to the phosphor layer.

Phosphor Layer Properties

The properties of the phosphor layer ultimately dictate device performance. Phosphor materials consist of a host material doped with luminescent centers. The dopant levels range from 0.1-1.0 mol%. The host material controls the electrical properties, primarily the threshold voltage of the phosphor, while the luminescent center is responsible for the emission wavelength. The host-luminescent center complex is generally thought to control the brightness and luminous efficiency [Ono92].

Host

The host material provides the lattice to which the luminescent material is added. Host materials must exhibit certain electrical and physical properties. The critical requirement of the host material is that it have an energy band gap large enough to allow visible light transmission without significant absorption. For blue phosphors, which have emission wavelengths ranging from 400 to 470 nm (3.09-2.64 eV), this requirement eliminates all materials with a bandgap below 2.6 eV. Additionally, due to the need for ballistic acceleration, the host material must have a high dielectric breakdown strength. Host materials must also allow for efficient transport of high energy electrons (> 2 eV) [Mac82]. It has been shown that materials having band gaps greater than 4.5 eV do not have the capability to transport significant current densities of hot electrons [Kin96]. The combination of the need for low light absorption and high electron transport efficiency results in limiting the bandgap range to between 2.6 and 4.5 eV for candidate host materials. Host materials should also exhibit both chemical and electrical stability. From the previous discussion on efficiencies, it is clear that it would be desirable for the host material microstructure to be defect free, in other words, only a low number of defects with minimum size such as dislocations, voids, non-crystalline regions or any structure which would reduce the internal efficiency can be tolerated. This would suggest that a single crystal material would be the ideal host; however the problem of wave guiding due to the index of refraction difference between the phosphor host material and the surrounding insulators prohibits its use. A polycrystalline material that promotes light scattering is a more suitable host material candidate.

Luminescent Center

The second component of the electroluminescent phosphor complex is the luminescent center. The luminescent center is an ion which undergoes an electronic transition upon excitation. The electronic transitions associated with the center upon impact ionization/excitation gives rise to the emission wavelength. An important prerequisite is that the candidate center material have inner shell transitions. To have efficient emission, the center must have a large capture cross-section for impact ionization and/or excitation and moderate solubility in the host matrix to take advantage of the hot electrons [Kin96]. Due to the high field operational conditions, these centers must also be stable. Specifically, the center must contain deep levels so that tunneling is not possible and also ideally should be isovalent or neutral with respect to the host lattice. Lastly, and most important for display applications, the emission associated with the center must be in the visible wavelength range.

SrS:Ce Phosphor System

Strontium sulfide belongs to the family of alkaline earth sulfides. Some of the important physical properties of SrS are listed in Table 2-1. Strontium sulfide is an ionic crystal with a rock salt crystal structure as shown in Figure 2-8 [Cul78]. As mentioned earlier, in order for SrS to be an electroluminescent phosphor, a luminescent center must be added. The emission wavelength of the doped SrS is determined by the type of dopant used. Studies have shown that a range of emission wavelengths are possible depending on the dopant used (Table 2-2).

The emission spectrum of a SrS:Ce TFEL device is shown in Figure 2-9. In a typical SrS:Ce TFEL device, emission is in the greenish-blue region (475-500 nm). Ligand field effects as well as the local crystal field results in an emission spectra rather than a line emission [Bla94]. Since, cerium is most commonly incorporated into the lattice as Ce^{3+}, the electron configuration is as follows: (krypton core) $4d^{10}4f^{1}$. The 4f orbital is an inner core shell which is sheltered from the surrounding crystal lattice atoms by the outer filled $5s^2$, $5p^6$ and $6s^2$ orbitals. The host lattice crystal field splits the excited configuration of the ground state into two components ($^2F_{5/2}$ and $^2F_{7/2}$) which are separated by some 2000 cm^{-1} due to spin-orbit coupling (Figure 2-10). Upon excitation, electrons from either of the ground state levels are excited into the unoccupied 5d level. Relaxation from the 5d into the ground state 4f levels results in the emission spectrum [Rac97].

Table 2-1. Physical properties of SrS.

Property	SrS
Crystal Structure	Rock Salt
Lattice Constant (Å)	6.019
Coordination Number	6
Ionic Radii of cations (Å)	1.13
Ionic Character (%)	≥ 78.5
Energy Band Gap (eV)	4.30 (indirect)

Table 2-2. Emission wavelengths as a function of dopant in SrS.

Luminescent Center	Peak Emission Wavelength (nm)
Cerium	480
Europium	600
Praesodenium	490;660
Samarium	570
Copper	470

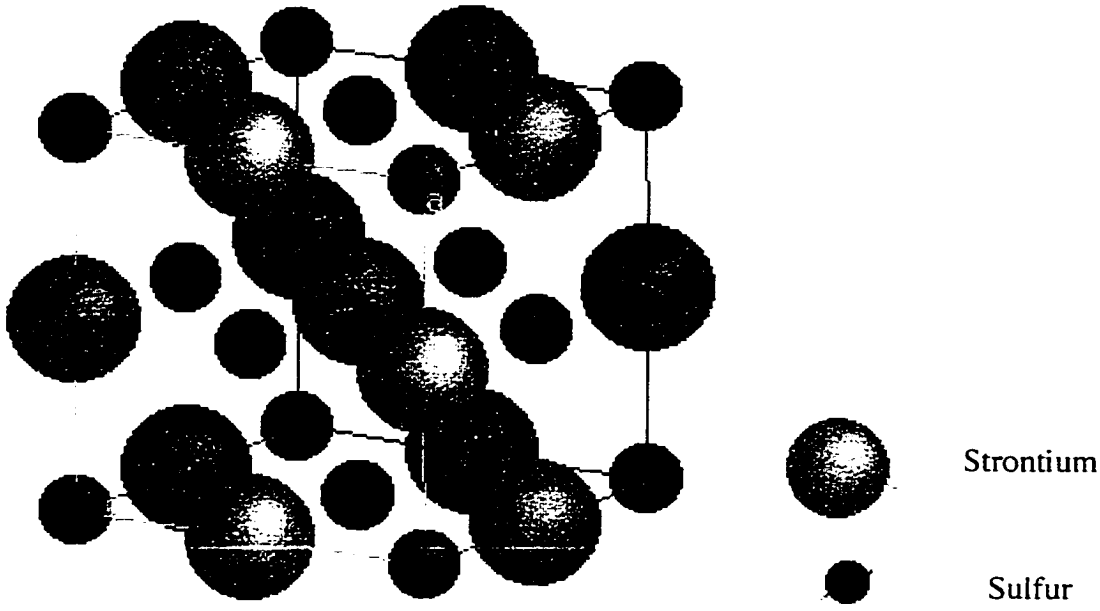


Figure 2-8. Crystal structure of strontium sulfide

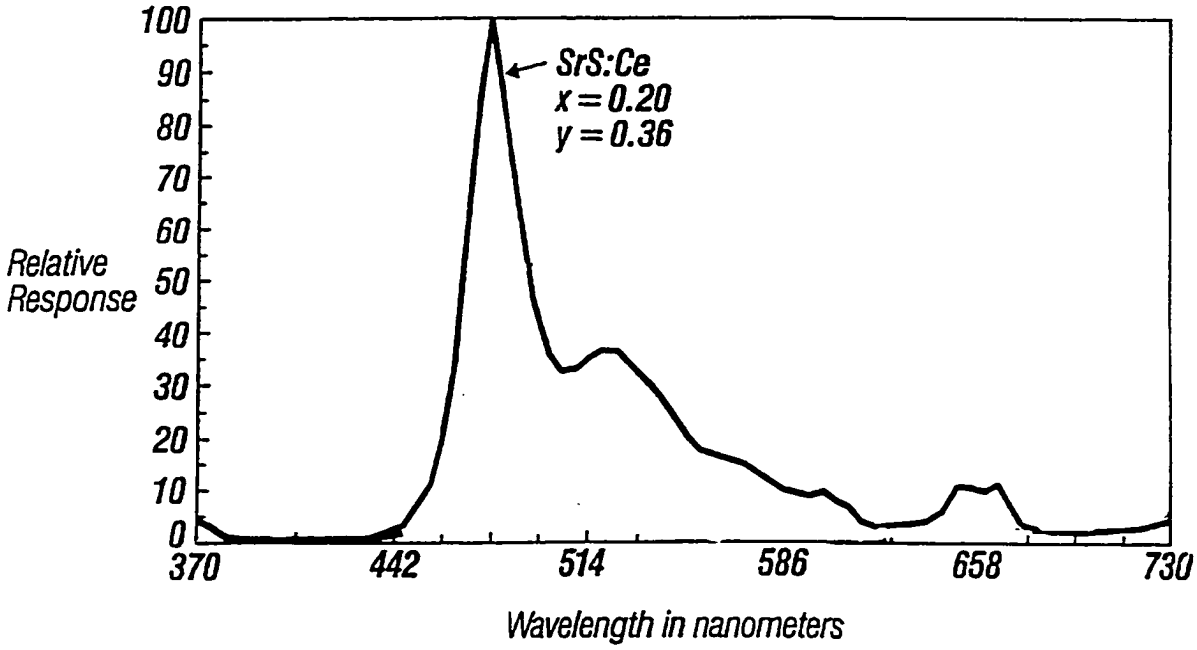


Figure 2-9. Electroluminescent spectrum from a SrS:Ce phosphor TFEL device

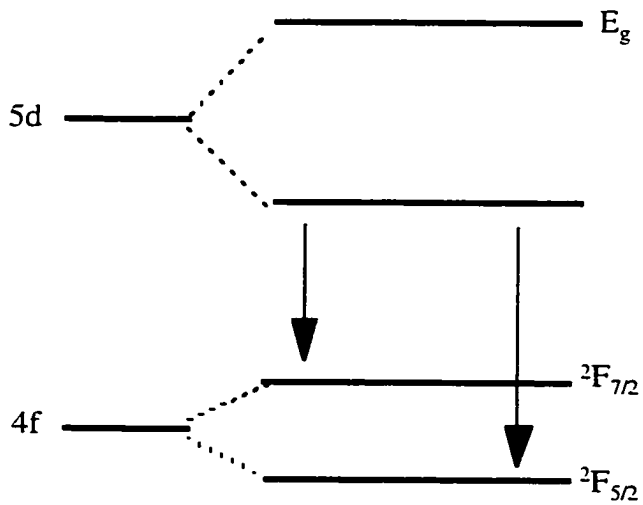


Figure 2-10. Possible radiative relaxation electron transitions in the Ce^{3+} ion in the SrS:Ce phosphor system

While the SrS:Ce system provides the best combination of brightness and blue emission of any phosphor system studied to date, this materials system still presents many opportunities for further development. The emission from these phosphors is blue-green and needs to be further shifted into the blue. Processing of SrS:Ce requires high temperatures and SrS is extremely hydroscopic resulting in chemical instability when exposed to moisture. The following section summarizes some of the work done on characterizing SrS:Ce TFEL devices as well as optimizing processing conditions.

SrS:Ce TFEL Devices

The first report of greenish-blue emission from SrS:Ce TFEL devices was by Barrow et al. [Bar93]. The authors reported significant improvement in brightness compared to the highest brightness blue/green phosphor at that time, ZnS:Tb. Intensive investigation was undertaken to improve the electrical and optical properties of SrS:Ce TFEL devices.

Onisawa et al. reported that sulfur addition during growth improved the luminance by three orders of magnitude [Oni88]. The authors proposed that the SrS:Ce films were sulfur deficient and that sulfur overpressures were needed to reach stoichiometric levels. The authors suggested that the incorporation of sulfur resulted in the reduction of oxygen in the film. Improved luminance was attributed to lower oxygen content, increased film density and improved crystallinity of the SrS:Ce layers.

Tamura et al. demonstrated improved crystallinity using sulfur co-evaporation followed by a post deposition anneal [Tam86]. The investigators also noted that the

improved crystalline quality of the SrS:Ce directly correlated with improved crystalline quality of the ZnS underlayer.

Tanaka et al. confirmed Onisawa's earlier work and demonstrated crystallinity improvement with increased substrate temperature and reduction in oxygen contamination with the addition of sulfur co-evaporation [Tan90]. The authors reported difficulty in preparing SrS:Ce TFEL devices. Stoichiometric deviation and poor crystallinity were attributed to the chemical instability and hydroscopic nature of SrS. X-Ray diffraction (XRD) analysis of the SrS:Ce layer showed that the full width at half maximum (FWHM) of the highest intensity reflection (200) decreased with increased substrate temperature used during deposition. Columnar grains of 0.1 to 0.2 μm diameter and 1 μm length were measured using a scanning electron microscope. The authors noted that the grain size must be increased in order to reach the electroluminescent efficiencies of the ZnS:Mn materials system.

Tohda et al. confirmed the increase in the intensity of the (200) XRD peak as a function of the substrate temperature [Toh91]. Confirming earlier works, the investigators reported a strong dependence of crystalline orientation on the hydrogen sulfide (H_2S) pressure. The improved luminance is attributed to improved crystallinity and stoichiometry in the SrS:Ce films. The authors pointed out two factors that should be considered with respect to the phosphor layer microstructure and its effects on the luminance. Primarily, the authors noted that the thickness of the grain boundary should be minimized. Secondly, the crystalline direction along which hot electrons flow in the SrS host matrix should be considered. The investigators postulated that in the SrS crystal,

the <100> directions may have higher impact excitation rates than other crystallographic directions.

The reoccurring observation of the deleterious effect of oxygen prompted Onisawa et al. to study the effects of oxygen on SrS powder and TFEL device performance [Oni91]. Since SrS is formed via sulphurization of $SrCO_3$, incomplete reaction can result in strontium existing in the form of SrS and $SrSO_3$ and $Sr(OH)_2$. Heat treatment of the impure SrS powder in a reducing atmosphere (H_2S) resulted in oxygen free powders. Films grown from the evaporation of the reduced powder resulted in narrower FWHM of the (200) peak than films grown from the un-reduced powders. The films grown from the reduced powder also exhibited a five fold increase in brightness at 60 volts above threshold (L_{60}). The authors hypothesized that the heat treatment reduced the amount of sulfur vacancies which are a major source of defects in the film. The authors cited previous work in ZnS:Mn films which showed a decrease in the threshold voltage and an increase in electrical conductivity with the reduction of sulfur vacancies.

Okamoto et al. reported the improvement in TFEL device performance after a post deposition annealing treatment [Oko93]. The annealed samples exhibited a ten fold increase in brightness. Luminance reached a maximum at an annealing temperature of 720°C with a decrease in luminance for higher annealing temperatures. This decrease was attributed to the degradation of the dielectric layers due to ion diffusion. Improved luminance was attributed to improved crystallinity which reduced electron scattering and resulted in greater acceleration of the electrons in the field. The authors also attributed enhanced luminescent center formation to the annealing procedure.

Ohmi et al. studied the effect of post deposition annealing of SrS:Ce TFEL devices in an argon-sulfur (Ar-S) atmosphere [Ohm95]. Annealing was performed at 630°C for 30 minutes. Luminance improved two fold as a result of annealing. The authors reported the presence of a "dead layer" comprising of small, uniform size polycrystalline grains near the dielectric surface of the as-deposited structure. The authors attributed the poor device characteristics of the as-deposited structure, in part, to the dead layer. The authors suggested that during annealing, recrystallization took place between the SrS grains. In the as-grown films, strontium atoms are not completely bound to sulfur atoms at grain boundaries and the dead layer. The recrystallization between the SrS grains is thought to be promoted through the reaction of the unstable strontium atoms with the supplied sulfur vapor. XRD results showed a twenty fold increase in the intensity of the (200) reflection. The intensity increase of the (200) plane was explained as being a result of improvement in the orientation as well as further crystallization of the SrS. Photoluminescent (PL) characterization of the annealed devices suggested that the crystal field around the Ce^{3+} luminescent centers did not change as a result of the annealing. In other words, the Ce^{3+} substituted for the Sr^{2+} sites of the SrS host lattice in both the as-deposited and annealed films. However, the increase in the photoluminescent (PL) intensity after annealing suggested that the defect density in the SrS host was reduced as a result.

The role of sulfur in the annealing atmosphere was found to be critical. Annealing in vacuum or in pure argon atmosphere was found to have no improvements in either EL or PL measurements. Sulfur vacancies were thought to be shallow electron traps and cause charge generation in the SrS:Ce layer. Crystallinity of the SrS:Ce thin films,

especially with regard to the previously mentioned dead layer, was found to improve with annealing in the Ar-S atmosphere. The improvement in crystallinity was thought to suppress charge generation and thus increase the electric field in the phosphor layer. This led to an increase in the excitation efficiency of the Ce^{3+} luminescent centers.

Yang et al. studied the effect of different dielectric underlayers on the EL properties of SrS:Ce TFEL device [Yan95]. The investigators proposed the phosphor layer crystallinity was a function of substrate temperature, deposition rate, and underlayer composition. The investigators studied two amorphous layers, Ta_2O_5 and SiO_2/Si_3N_4. While both dielectric materials are amorphous in structure, the XRD (200) peak intensity was found to be an order of magnitude greater for the Ta_2O_5 than the SiO_2/Si_3N_4. The increase in luminance was attributed to the measured increase in (200) peak intensity. The authors concluded that any increase in luminance could only result from the improvement in the crystallinity of the phosphor film.

Table 2-2 summarizes the results from the reviewed work. This table clearly shows that high brightness devices are possible, but at a cost. For example, Onisawa et al. reported a brightness of 1000 cd/m^2. However, in order to attain such a value the device must be driven at 350 volts at a frequency of 5 kHz. As previously discussed in equation 2.2, the brightness is directly dependent on drive voltage and frequency. The need for inexpensive and space efficient drive electronics require that devices should operate at 60 Hz and not the 1kHz that is most commonly reported in the literature. Additionally, drive voltages used in the literature typically exceed the 150 volts desired for commercially viable TFEL devices.

Table 2-2. Brightness and threshold voltages as a function of drive conditions for SrS:Ce TFEL devices.

Author/Year	Drive Voltage (volts)	Drive Frequency (hz)	Threshold Voltage (volts)	Brightness (cd/m^2)
Onisawa/1988	350	5000	200	1000
Tanaka/1990	220	1000	180	325
Onisawa/1991	260	1000	200	280
Tohda/1991	200	1000	120	600
Chubachi/1992 [Chu92]	200	1000	95	300
Okamoto/1993	150	1000	90	320
Ohmi/1995	280	1000	200	800
Yang/1995	225	1000	180	80

The preceding survey identified that improvements in the crystalline quality of the phosphor layer directly led to optimized device performance. Based on the past work, the critical parameters which control the overall crystalline quality of SrS based thin films were found to be: 1) sulfur content, 2) annealing temperature, 3) crystalline quality of underlayer and 4) film deposition rate. The objective of the previously reviewed work was to establish the baseline electrical and optical properties of SrS:Ce TFEL devices, such as threshold voltage and emission wavelength, and identify optimized growth methods. The various devices were evaluated only on performance. Inferences were made to a relationship between crystalline quality and TFEL device properties, but none of the studies focused on the microstructure of the phosphor layer. The next section summarizes articles which directly investigated the phosphor layer microstructure and its role on the TFEL device properties.

Phosphor Layer Microstructure

Thies et al. studied the cross-sectional structure of TFEL devices fabricated by various deposition methods using a transmission electron microscope (TEM) [The83]. Two different phosphor layer materials were studied: ZnS and ZnSe. The deposition methods used were e-beam evaporation, atomic layer epitaxy (ALE), and sputter deposition. Evaporated ZnS films showed a strong tendency to form columnar structures. Increased substrate temperatures led to increased grain diameters with the largest mean grain diameter of 80 nm for the films grown on a substrate at 250°C. Voids were detected between the columnar grains. The samples containing voids exhibited much higher brightness but poor reliability. The ZnSe evaporated films had much higher grain sizes which resulted in an increase in brightness. The larger equiaxed grains that result from annealing were thought to reduce the number of shunt paths for electron flow which resulted in enhanced luminescence efficiency. ALE grown ZnS films exhibited very pronounced columnar grain morphology. Sputter deposited ZnS samples were not stoichiometric. The S/Zn ratio was found to change as a function of film depth. The total grain boundary surface area in the initial fine grained growth region was found to decrease with increasing S/Zn ratio i.e., grain size increased from the dielectric layer to the top of the film. The authors summarized that the strongly disordered fine grained structure is responsible for higher threshold fields. The long thin grains associated with both evaporated and ALE deposition methods lead to relatively low efficiencies and brightness. There was a direct correlation between large grained material and higher brightness films.

Hua et al. studied the role of microstructure on the photoluminescent properties of SrS:Eu^{2+}, Sm^{3+} TFEL devices [Hua94]. In this system, the host is doped with two

centers, giving rise to emission peaks attributable to Eu^{2+} and Sm^{3+}. The microstructure was altered by changing the substrate temperature and/or deposition rate during e-beam evaporation. Microstructures were analyzed using transmission electron microscopy (TEM) and XRD. The motivation for the study was the significantly higher PL emission intensity of bulk material compared with thin film samples. The poor crystallinity of the films was blamed for the poor PL intensity of the Sm^{3+} emission. Growth rates were found to have an even greater effect on the PL intensity. While the Eu^{2+} emission PL intensity was slightly higher with higher growth rates, the emission PL intensity of Sm^{3+} was significantly increased. TEM analysis showed that the films grown at higher growth rates contained columnar grains that were wider and longer (100nm) than those grown at lower growth rates . The authors noted that the smaller grained material contained greater grain surface area. The authors cited earlier work which noted that samarium can exist in both a divalent and trivalent state depending on whether its in the bulk or at the surface. The divalent form is optically inactive and found in higher concentrations at the surface. The authors suggested that the lower PL intensity for the fine grained films was a result of a greater number of Sm ions existing in the optically inactive divalent state due to the larger grain surface area.

Hsieh et al. studied the use of SrS:Eu,Sm as an infrared stimulable phosphor to be used in a photonic data storage disk [Hsi95]. In order to maximize the brightness, the authors optimized the following process parameters: deposition method, substrate temperature and sulfur addition. Moisture in the starting SrS powder was identified as a factor leading to poor crystallinity. Energy dispersive spectroscopy (EDS) showed that the films were sulfur deficient due to preferential re-sputtering of sulfur. The sulfur

deficiency is thought to have led to the formation of micro-cracks. Co-evaporation of sulfur during film deposition led to two-fold increase in the brightness of evaporated films. TEM analysis revealed a columnar grain morphology with a mean grain diameter of 400 nm. Voids were reported between the columnar grains. The authors suggested that the thermal expansion mismatch between the film and the substrate resulted to a tensile stress state being imparted on the film upon cooling from the elevated deposition temperature. The formation of the tensile stress state is the cause of micro-cracking. There was some evidence that the co-evaporation of sulfur resulted in the reduction of void concentration as well as micro-cracking. RF-sputter deposited films had lower void densities than their evaporated counterparts. However, the brightness of these films was an order of magnitude lower than their evaporated counterparts. The authors suggested that sulfur deficiency, oxygen contamination and crystalline defects all contributed to the poor brightness.

The past three studies clearly identified a relationship between the thin film microstructure and the electroluminescent properties. The microstructural characterization revealed that the phosphor layer microstructure was far from ideal for optimized electroluminescence. The presence of small diameter columnar grains and large grain boundary volume combined with crystalline defects such as voids led to reduced EL performance. These studies show that for optimized EL performance the microstructure should exhibit the following: 1) crystalline structure, 2) large equiaxed grains, 3) reduced grain boundary volumes, 4) good stoichiometry.

Microstructural Evolution

Most materials of practical importance are polycrystalline and the size, shape and orientation of the constituent grains and the corresponding grain boundaries strongly influence the physical properties of the material. Understanding the mechanisms which determine the final grain size and orientation in order to produce the desired final properties is one of primary goals of this study.

The previous section highlighted the importance of the phosphor layer microstructure on the TFEL device performance. This section will identify the factors which control the microstructure of sputter deposited thin films. A review of thin film deposition via the sputter deposition process as well as the process variables which control the as-deposited thin film microstructure is presented. Next, since the films in this study are subjected to a post deposition anneal, the fundamentals of thermally assisted grain growth will also be reviewed.

Sputter Deposition

Sputter deposition is one of the most widely used thin film deposition methods used in industry. Sputtering is a process in which energetic particles strike the surface of a target material and eject particles from the target's surface by a momentum exchange process [Ohr92]. The resultant flux deposits onto a substrate (Figure 2-11). An inert gas such as argon is backfilled into a vacuum chamber and due to a potential difference between the anode and cathode in the sputter system, argon ions (Ar^+) are generated. A conducting target material can be biased using a DC potential, where the target can also be

used as the cathode material. The bias condition results in the acceleration of the Ar^+ to the cathode and this bombardment results in the sputtering of the target material. A non-conducting target material requires the use of a RF potential and the target is usually attached to a conducting cathode electrode [Tho84] . The sputtered flux consist primarily of low energy atoms, although energetic neutral molecules as well as low and high energy positive and negative ions can also be generated. One of the primary reasons that sputtering is so widely used in industry is that, in general, the composition of sputter deposited films equals that of the multi-component target [Ohr92]. The efficiency of the sputtering process of a particular target material is measured by the sputter yield. The sputter yield is defined as the number of atoms or molecules ejected from a target per incident ion [Ohr92].

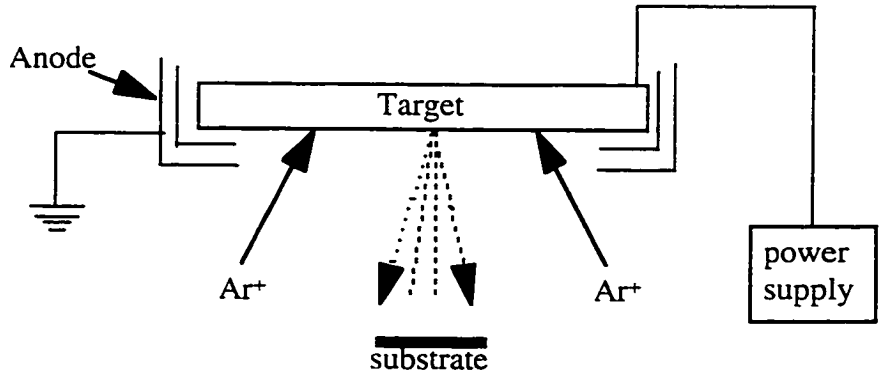


Figure 2-11. Schematic representation of a sputter deposition chamber

Altered layer formation

In a multi-component target, with a composition of AB, the sputtering process produces an altered layer at the sputter target surface [Cho85]. If the sputter yield of component A, Y_A, is twice that of component B, Y_B, the initial sputtered flux will be rich in component A resulting in the surface of the sputter target being depleted in component A. This layer in which the stoichiometry has been changed is referred to as the altered layer. While this may lead to deviations from stoichiometry initially, a steady state condition will be reached in which the surface concentration of A will become half the concentration of A in the bulk with a simultaneous rise in the surface concentration of B. The formation of the altered layer counteracts the effects of differing sputter yields. After the initial transient period, the steady state sputtered flux and the deposited thin film will have the same composition as the bulk target.

Factors leading to deviations in stoichiometry

As stated earlier the formation of the altered layer acts as a correction mechanism to counteract the differences in sputter yield of the different components in an alloy. While sputtering should theoretically result in little or no stoichiometric deviations between the film and target, there are four main mechanisms which can lead to deviations between the sputter target stoichiometry and the thin film stoichiometry: 1) migration of species to the sputter target surface, 2) angular distribution of sputtered species, 3) different sticking coefficients and 4) negative ion re-sputtering.

Migration of species to the target surface can affect the formation of the altered layer leading to stoichiometric deviations [Tho84]. Target heating can lead to the formation of mobile species which are driven by the concentration gradient between the target surface and the bulk. The migrated species can change the stoichiometry of the altered layer. Since the altered layer formation acts to counteract the differing sputter yields of individual components, changes in the altered layer stoichiometry can result in time dependent compositional differences between the deposited film and the bulk of the target.

Differences in the angular distribution of the sputtered species in a multi-component target can also lead to variations in stoichiometry [Vos78]. Preferential sputtering of the lower mass component along the target surface normal is observed with the heavier component sputtered along more oblique angles. Careful positioning of the substrate may be used to ensure a proper angle which will result in a film with same composition as the target.

Different sticking coefficients between the various constituents in a multi-component target is a major source of compositional variances between the film and target. The sticking coefficient is commonly defined as the number of atoms of a particular species adhering to a surface divided by the total number of atoms of that species that hit the substrate surface often measured per unit time in both cases [Cho85]. The volatile species in the target will commonly be deficient in the film due to low sticking coefficients. Another factor which can affect the sticking coefficient is the substrate temperature. Due to bombardment by electrons and reflected argon atoms, substrate temperatures can reach temperatures as high 200°C without intentional heating.

For large grain sizes and better crystallinity, the substrate is intentionally heated in order to improve atomic mobility. At these elevated temperatures, high vapor pressure species such as sulfur may have sticking coefficients less than one.

Negative ion re-sputtering can be a significant cause of compositional differences [Dav97]. As stated earlier, the list of species that result from the sputtering process include atoms, molecules as well as positive and negative ions. While the positively charged ions are attracted to the target due to its negative charged, negatively charged ions are attracted to the substrate. Usually, interaction with electrons in the plasma result in the formation of neutrals which are then subject to further energy draining collisions. For target to substrate distances less than or on the order of the mean free path for collisions, energetic negative ions can pass through the plasma and sputter the film on the substrate. This re-sputtering can cause deviations in film thickness as well as stoichiometry.

The above discussion has highlighted some of the problems which may arise during the sputter deposition process. Due to problems such as different sticking coefficients or different atomic masses, it is clear that sputtering of multi-component targets is challenging. Careful control of sputtering power, gas pressure, substrate distance and substrate temperature are essential in order to achieve stoichiometric films as compared with the target.

As-Deposited Thin Film Microstructure

The interaction between the sputtered species and the substrate define the as-deposited thin film microstructure. The thin film deposition can be broken up into three steps: 1) the transfer of kinetic energy from the incident sputtered species to the

substrate lattice resulting in loosely bonded adsorbed atoms or molecules (adatoms or admolecules), 2) diffusion of adatoms or admolecules on the substrate surface terminating when the adatoms become trapped at low energy lattice sites and 3) rearrangement of adatoms within the lattice via bulk diffusion processes [Tho77]. The most common classification system developed to explain the microstructure of as-deposited thin films is the Movchan-Demchishin model. The model is based on the microstructure observed for evaporated metallic films as a function of the substrate temperature divided by the melting temperature of the sputtered species (T_s/T_m). Thorton refined this model for sputtered films by including the effect of inert gas pressure [Tho77]. As seen in Figure 2-12, Thorton's model uses four distinct zones to describe the microstructural morphologies that are observed as a function of T_s/T_m and inert gas pressure.

Zone 1 is found when $T_s/T_m < 0.1$. The microstructure of zone 1 is characterized by fine columnar grains separated by voids. These grains are characterized by high dislocation densities. The observed microstructure is a result of very limited adatom diffusion which is too low to overcome the effects of substrate shadowing [Tho77].

Zone 2 is found when T_s/T_m is between 0.3 and 0.5. The microstructure in this zone is characterized by columnar grains which are separated by distinct and dense boundaries. The observed microstructure in this zone is attributable to appreciable rates of surface diffusion [Tho77].

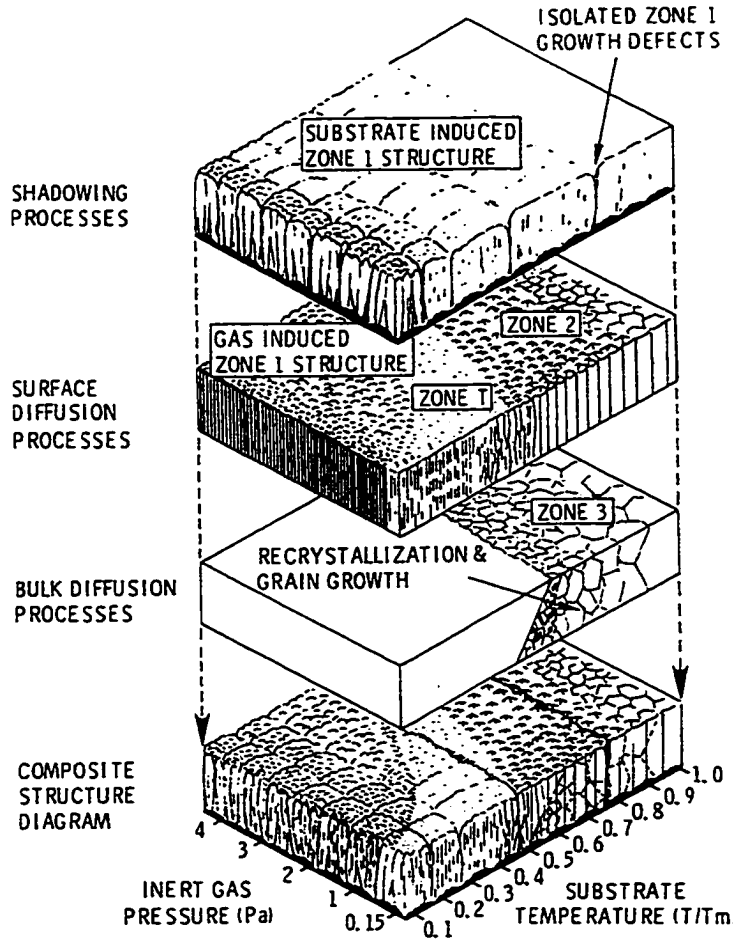


Figure 2-12. Schematic representation of the observed microstructure in as-deposited thin films as a function of T_s/T_m and inert gas pressure as proposed by Thorton [Ohr92]

Zone T or a transition zone is the name given to the microstructure found to exist between zones 1 and 2 and consists of a dense array of poorly defined columnar grains without voided boundaries. The temperature range where one would observe these microstructural features is a function of inert gas pressure and can range from $T_s/T_m = 0.1$ for inert gas pressures of 0.15 Pa to $T_s/T_m = 0.4$ for inert gas pressure of 4 Pa [Tho77].

Zone 3 is characterized by equiaxed grains and is observed when Ts/Tm is between 0.6 and 1.0. The observed microstructure is attributed to significant bulk diffusion processes due to the high temperatures [Tho77].

Thermally Assisted Grain Growth

It is clear from the earlier sections that large grain, properly textured polycrystalline material would result in improved EL performance. However, the high substrate temperatures required to achieve such an as-deposited microstructure could lead to detrimental stoichiometric deviations. Post deposition annealing is widely used to increase the grain size of as-deposited polycrystalline thin films. The following section highlights the fundamentals of thermally assisted grain growth in thin films including grain growth models, the driving force for grain growth and grain growth kinetics.

Grain Growth Models

Physical models have been proposed to describe the mechanisms for thermally assisted grain-boundary migration including: 1) the vacancy model [Hae71], 2) the step model [Li61] and 3) the dislocation model [Smi80]. The vacancy model states that atoms can only cross the boundary at vacant sites, whereas in the step model atoms dissociate from kinks on one boundary and diffuse to kinks of the other grain boundary. In the dislocation model, dislocation glide is thought to be responsible for boundary migration. All of these mechanisms are essentially governed by a similar rate limiting process, the

addition of an atom to a site such as a vacancy, step or dislocation. Hence the activation energy for the thermally assisted grain growth represents the energy barrier of the thermally activated atomic diffusion in the grain boundary area.

In single phase systems, it is assumed that the grain growth mechanism is diffusion controlled. In other words, the motion of a grain boundary is due to the movement of atoms from one side of the grain boundary to the other as illustrated in Figure 4-13. Therefore the grain growth rate is determined by the diffusion rate of atoms across the grain boundary interface. This movement is accomplished by a series of diffusion jumps of individual atoms across the boundary. In the absence of a driving force, the jumps in one direction will equal the jumps in the opposite direction resulting in no net movement of atoms. When a driving force is present, the total free energy is reduced with the net flow of atoms from one grain to another resulting in the boundary migration and thus grain growth.

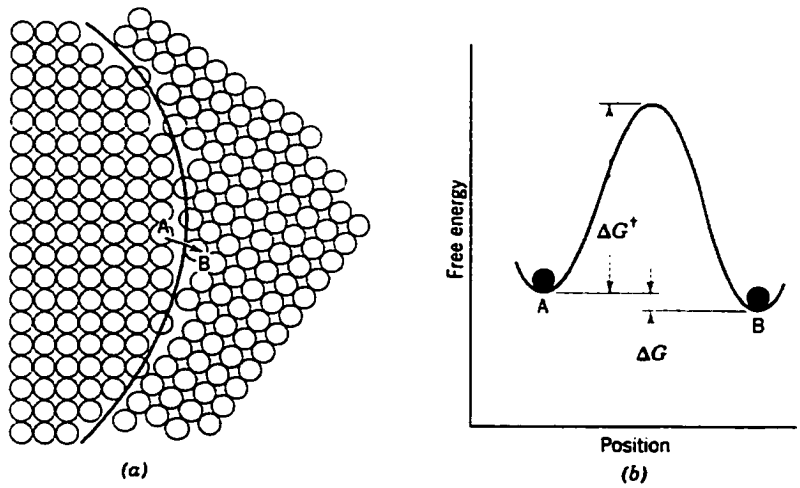


Figure 2-13. (a) Schematic of an atomic jump across a boundary associated with grain growth and (b) the free energy change associated with such a jump

Another model proposed by Dehoff suggests that grain growth is achieved not by diffusion across the grain boundary but rather by much smaller movements from lattice site of the consumed grain to lattice site of the growing grain as shown in Figure 2-14 [Deh97]. In Figure 2-14, the atomic rearrangement would result in the atoms in grain 1 migrating to the open lattice spacings which follow the registry of grain 2 resulting in the grain boundary moving by one row of atoms. This process, carried out over time, would ultimately result in the growth of grain 1 and the disappearance of grain 2. This process would involve less energy than the atomic diffusion process reviewed earlier resulting in the lower activation energy value.

Driving Force

The microstructure of polycrystalline thin films is comprised of grains and defects. Defects can include point defects such as vacancies, line defects such as dislocations and planar defects such as grain boundaries. During the annealing process, the driving force for grain growth is the reduction in interface energy of the material resulting from the grain boundaries [Sin94]. As the grains grow in size, their numbers decrease corresponding to a decrease in grain boundary area and therefore interface energy. The pressure difference that exists between one side of the grain and the other results in diffusion of atoms; the net flow occurring through the grain from the high to the low pressure side [Kin76]. In other words, the atoms diffuse from the inside to the outside of the grain.

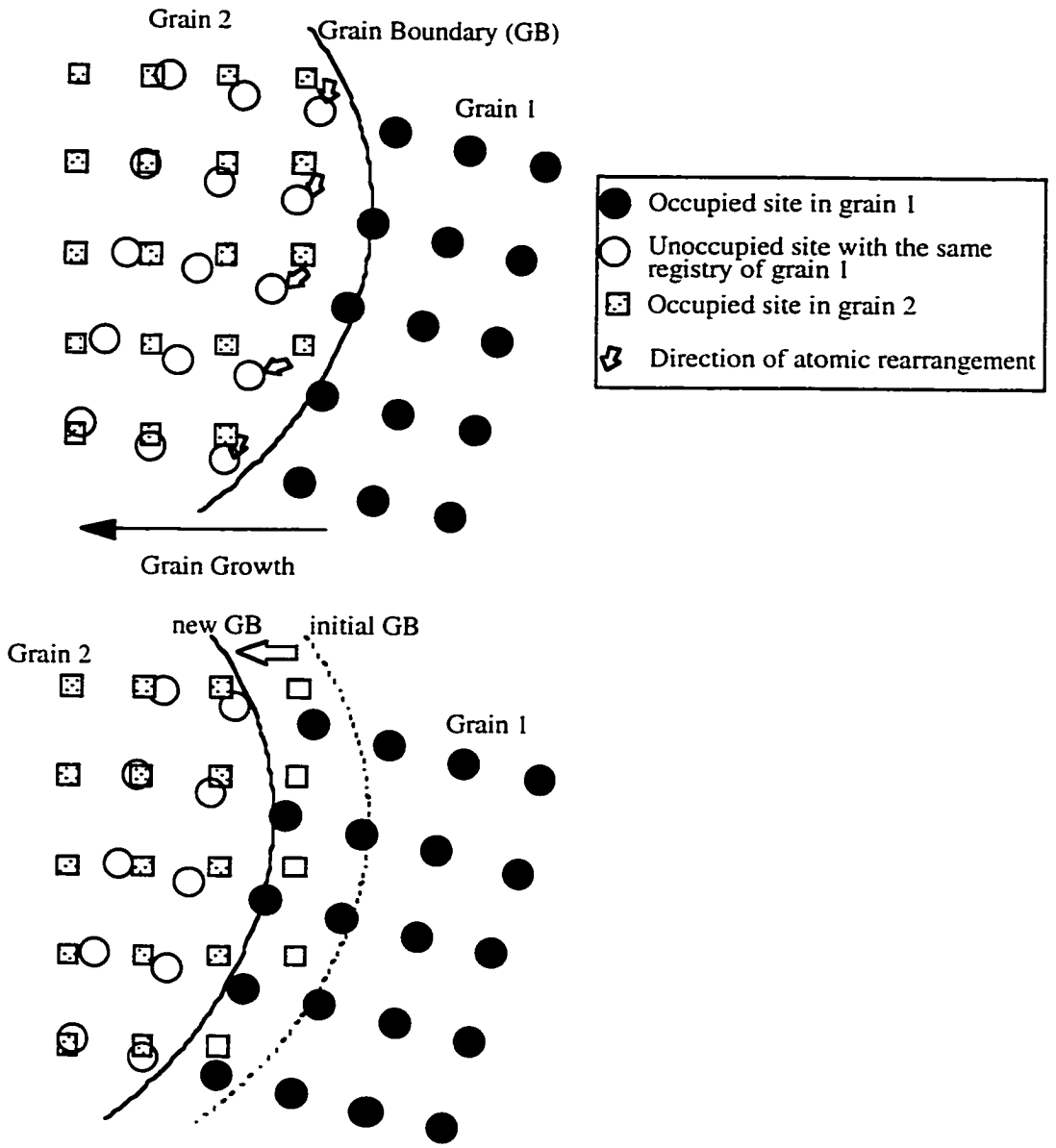


Figure 2-14. Atomic migration theory for grain growth proposed by Dehoff [Deh97]

In addition to the interfacial energy associated with the grain boundary, there is a free-energy difference across a curved grain boundary [Kin76]. The difference in the free energy of material on two sides of a grain boundary is the driving force that makes the boundary move toward its center of curvature.

Grain Growth Kinetics

In the analysis of growth kinetics, Hillert suggested that the migration velocity of a grain boundary is proportional to the pressure difference caused by the grain boundary curvature [Hil65]. In consequence, the average grain size is parabolically dependent on the time of a thermally activated process. For any one grain, the radius of curvature of a side is directly proportional to the grain diameter, so that the driving force, and therefore the rate of grain growth, is inversely proportional to the grain size (equation 2.13) [Kin76].

$$\frac{\partial d}{\partial t} = \frac{k}{d} \qquad (2.13)$$

$\frac{\partial d}{\partial t}$ = rate of change of the grain diameter with time

k = constant d = grain diameter

The grain growth law describes the relationship between the grain size and time for an isothermal annealing step (equation 2.7). From experimental results, it is found that the grain growth exponent, n, increases with increasing temperature and approaches

the value of 0.5 [Ree92]. From equation 2.8, it is clear that temperature affects the constant, k, and thus the relationship between the mean grain diameter and time.

$$D = kt^n \tag{2.7}$$

$$k = k_0 \, e^{\frac{Q}{2RT}} \tag{2.8}$$

D = mean grain diameter
t = time
k = grain growth constant
n = grain growth exponent assumed to be 0.5
k_0 = constant
Q = activation energy
R = gas constant
T = temperature (Kelvin)

Summary

The survey of the literature indicated that the microstructure of the phosphor layer plays a critical role in the properties of a TFEL device. The literature suggests that properly textured films composed of large grains lead to enhanced device performance. However, past research performed on the SrS:Ce phosphor system indicates that the microstructure consists of fine columnar grains which results in poor EL performance. Grain growth in this system has not been studied but if it obeys conventional diffusion controlled grain growth models, increased annealing temperature is the only way to increase grain size. The temperature limitation imposed by the glass substrate confines the temperature regime that can be used.

The addition of gallium sulfide (Ga_2S_3) has been found to significantly improve the electroluminescent properties of SrS:Ce TFEL displays, but the reasons for this improvement were not determined [Sun96]. Based on the literature, our hypothesis was

that the Ga_2S_3 resulted in a change in the microstructure. The objective of this study was to investigate the effects of Ga_2S_3 additions on the microstructure of SrS:Ce as a function of annealing temperature and to determine whether the microstructural changes were responsible for the enhanced EL properties.

Preliminary Work

Prior to studying the SrS:Ce TFEL phosphor system, the microstructural properties of the cerium doped thiogallate ($(Sr_{.55}Ca_{.45})Ga_2S_4$:Ce (3%)) blue phosphor system were investigated as a function of post deposition annealing temperature. Thiogallates are gallium sulfide based compounds with alkaline earth atoms (Ca and/or Sr) substituting for some of the gallium atoms. The luminescent properties of cerium doped thiogallates were first reported by Peters et al. [Pet72].

Electrical and optical characterization performed on these TFEL devices showed that deeper blue (smaller CIE y component), lower threshold voltages and higher brightness were achieved with higher annealing temperatures. The lowest threshold field of 180 volts and highest brightness levels of 2.4 cd/m^2 were measured for the devices annealed at 810°C.

Microstructural analysis revealed that the as-deposited phosphor material was amorphous in nature (Figure 2-15) and upon annealing, at temperatures above 750°C, the phosphor film crystallized (Figure 2-16). The result of the amorphous to crystalline transition was the formation of voids. The mean grain size of the thiogallate films

annealed at 810°C was 2200 ±500Å. A homogenous void distribution was observed with a void volume fraction of 10% and an average void size of 1000 ± 450Å.

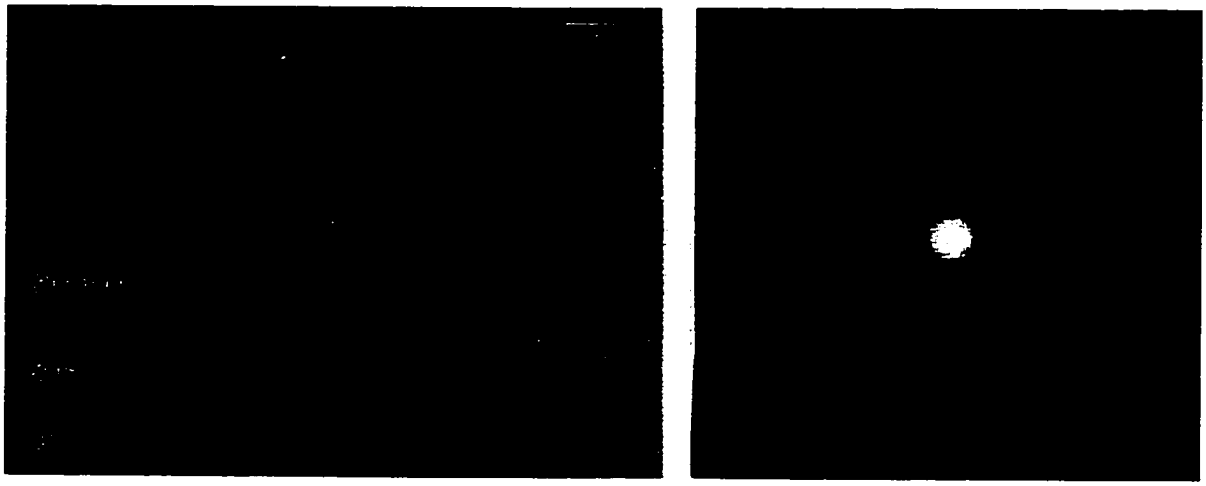


Figure 2-15. As-deposited thiogallate TEM micrograph and SADP from the thiogallate layer indicating amorphous structure

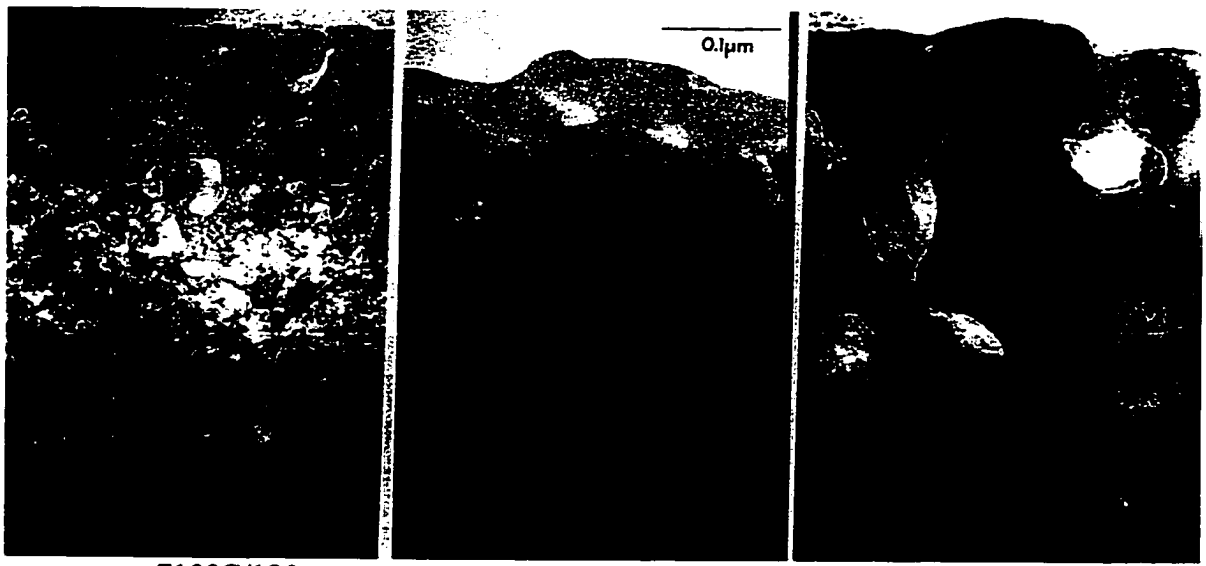


Figure 2-16. TEM micrographs of the thiogallate phosphor layer as a function of annealing temperature

Concurrent research in the SrS:Ce phosphor system indicated that even with the use of a filter to enhance the blue emission, filtered SrS:Ce was still brighter than the brightest thiogallate phosphors. Due to the low brightness levels, investigations into thiogallate containing TFEL devices was abandoned. However, the availability of the SrS:Ce phosphor system provided an opportunity to study the effect of combining the two systems on the EL properties. The rationale for this study was that the threshold field of the SrS:Ce was so low that it was thought that SrS:Ce could be added to the thiogallate phosphor system in order increase the brightness without significant impact on the threshold voltage. The result of these experiments led to the discovery that additions of Ga_2S_3 to SrS:Ce TFEL phosphors led to significant improvements to TFEL device performance. The reports of these experiments are reported in chapter five.

CHAPTER 3
MATERIALS AND METHODS

Introduction

The following chapter provides a review of the experimental details of this study. This chapter is divided into four sections: 1) review of the experimental plan, 2) the phosphor materials studied, 3) TFEL device fabrication and 4) characterization techniques.

Experimental Plan

As stated earlier, the objective of this research was twofold: 1) investigate the effect of Ga_2S_3 additions on the microstructure of SrS:Ce and 2) determine a correlation between changes in phosphor layer microstructure and improvements in the electroluminescent properties in the Ga_2S_3 containing SrS:Ce TFEL devices. Schematics of the different device compositions are listed in Figure 3-1.

In order to gain a better understanding of the SrS:Ce phosphor system, devices were fabricated using only SrS:Ce in the phosphor layer with different annealing conditions. This experiment was performed in order to understand the microstructural evolution of the SrS host matrix as a function of annealing temperature. Electrical and

optical characterization was also performed on these devices in order to correlate the microstructure with the EL properties.

Gallium and excess sulfur were introduced into the SrS host matrix via the deposition of a 400 Å capping layer of thiogallate ($(Sr_{.55}Ca_{.45})Ga_2S_4$:Ce(5%)) on the 1 μm thick SrS film. These devices are known as double layer devices. The double layer devices were annealed at three different temperatures, 650°C, 750°C and 810°C for 120 seconds. Following the annealing, the double layer devices were electrically and optically characterized. The role of post deposition annealing temperature on the phosphor layer microstructure and device properties was investigated.

The next set of devices introduced more gallium and excess sulfur via the addition of multiple layers of thiogallate. Alternating layers of thiogallate (300 Å) and SrS:Ce (1700Å) were grown resulting in a 1μm thick phosphor layer. These devices are referred to as multi-layer devices. These multi-layer devices underwent the same annealing procedures as the double layer films. Electrical and optical characterization was also performed on the multi-layer devices.

The results of the double layer and multi-layer studies led to direct addition of Ga_2S_3 (7 wt.%) into the SrS:Ce target material. Phosphor films were sputter deposited from this target and annealed. The same post deposition annealing temperatures were utilized. The gallium sulfide doped TFEL devices were electrically and optically characterized.

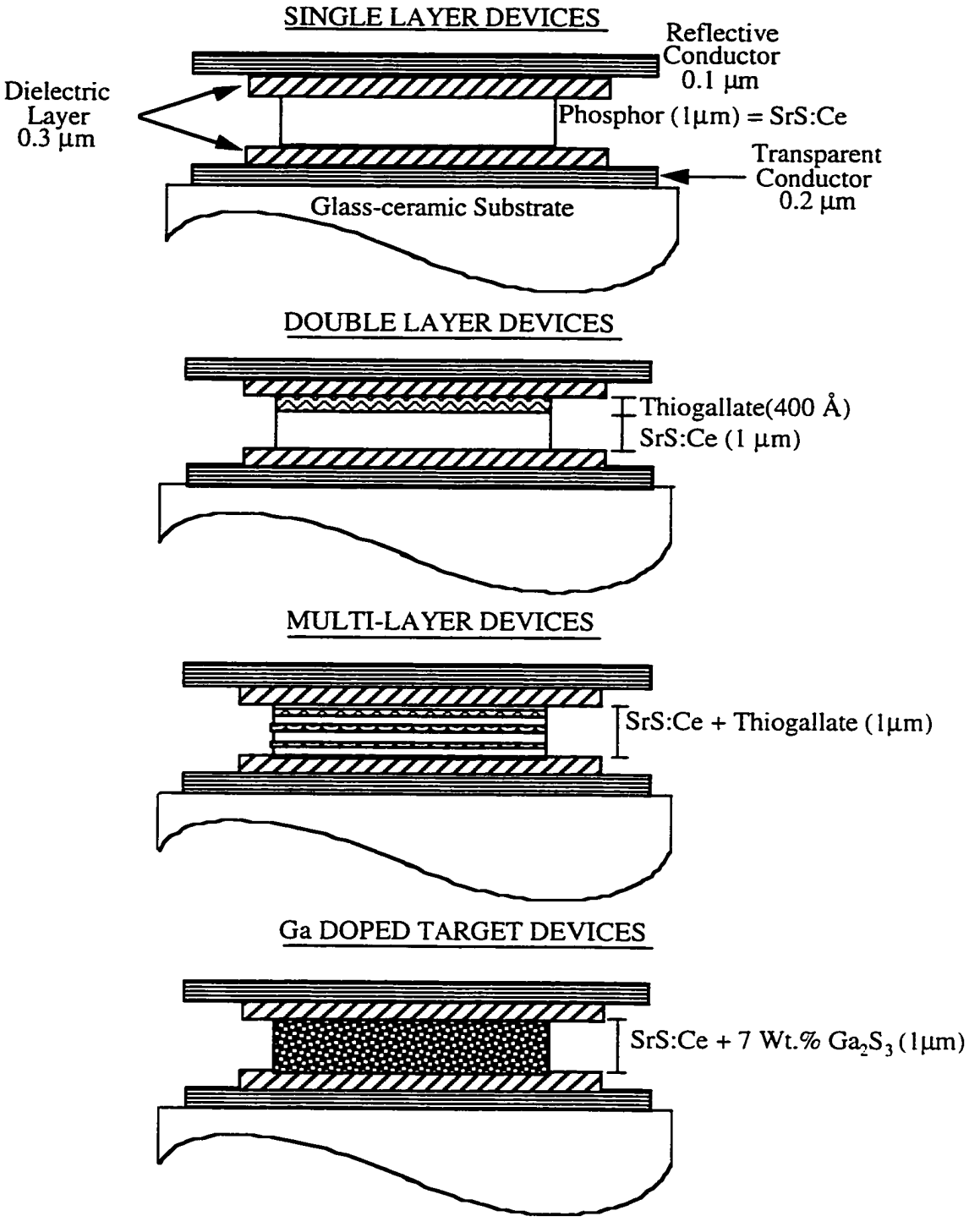


Figure 3-1. Schematic illustrating the different phosphor layer compositions investigated

Device Fabrication

The following section describes the materials and fabrication methods used to make the TFEL devices. In this section, information on the materials used for the substrate as well as the conductive, dielectric and phosphor layers will be presented, along with information on the sputter deposition conditions and the post deposition annealing process. A schematic diagram describing the TFEL device fabrication process is illustrated in Figure 3-2.

Substrate Material

As mentioned earlier, the most important property requirements for the substrate material are the need for light transmission and thermal stability. A 1.1 mm thick glass-ceramic material (Ohara Glass) was used as the substrate material. In addition to the desired optical properties, the glass-ceramic substrate had a softening temperature greater than 850°C which allowed for the high temperature post deposition annealing process.

Conductive Layer Materials

A transparent conductive layer consisting of indium tin oxide (ITO) was sputter deposited onto the glass-ceramic substrate. The ITO film thickness was 2000 Å. Due to the architecture of the device, a reflective top electrode was required. A 1000 Å thick layer of aluminum was evaporated and served as the top electrode.

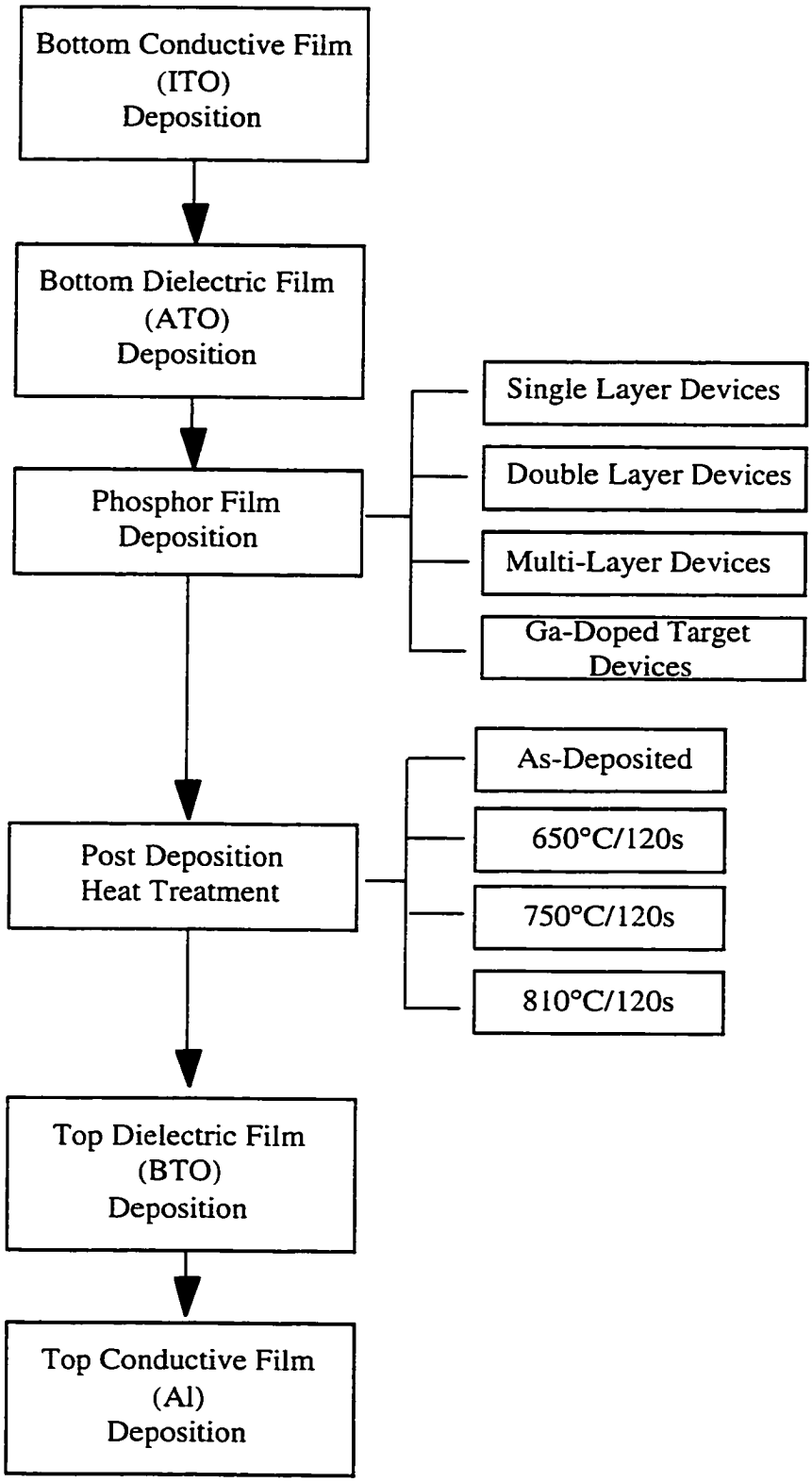


Figure 3-2. TFEL device fabrication flow diagram

Dielectric Layer Materials

A 2600 Å thick film of ATO (alternating layers of alumina (Al_2O_3) and titania (TiO_2)) was deposited on the ITO layer. The ATO film served as the bottom dielectric layer. ATO was chosen in part for its dielectric properties as well as its thermal stability. Since the TFEL devices were annealed prior to the deposition of the top dielectric layer, a dielectric material with a lower degradation temperature could be used. The top dielectric layer consisted of a 3000 Å thick film of barium tantalate (BTO, $BaTa_2O_6$).

Phosphor Layer Materials

Experimental sputter targets were made at the David Sarnoff Research Center. Strontium sulfide powder with cerium fluoride powder (0.12 mol.%) was mixed and pressed into a circular tablet (d = 6 cm; t = 0.5 cm) and sintered at 1200°C for 3 hours. Thiogallate targets were made by mixing calcium sulfide, strontium sulfide, cerium fluoride (0.12 mol.%) and gallium sulfide powders. Following thorough mixing, the resultant powder was then pressed into a circular tablet and sintered at 1200°C. Gallium doped SrS targets were made by mixing Ga_2S_3 (7 wt.%) with the SrS:Ce powder. The resultant powder was pressed into a circular tablet and sintered at 1200°C.

Phosphor Layer Deposition Conditions

Phosphor layers were sputter deposited onto glass-ceramic substrates coated with ITO and ATO at substrate temperatures of either 250 °C or 380 °C depending on the phosphor layer composition. The sputter deposition power was 100 W and an argon pressure of 35 mTorr resulting in a film growth rate of approximately 3000 Å/hr.

Annealing Conditions

Following the deposition of the phosphor layer, the devices were annealed in order to optimize performance. Due to the previously mentioned deleterious effects of oxygen, a load-lock annealing furnace was used. A schematic illustration of the annealing furnace is shown in Figure 3-3. Since the infra-red radiant energy flux of the annealing furnace is not absorbed by the phosphor material, the samples were placed on a graphite susceptor plate. The graphite susceptor plate is used to absorb the infra-red radiant energy. The heat is transferred to the glass-ceramic substrate by conduction and ultimately to the phosphor film via conduction.

Once inside the load locked chamber, samples were raised to the top level of the furnace which was held at the preset maximum temperature. Travel times for the sample averaged 30 seconds. The hold time at the top level was programmed and was set at 120 seconds. An optical pyrometer focused on the graphite substrate holder can also be used to monitor the TFEL device temperature. After completion of the annealing step, the sample was lowered to the lower level. Due to the configuration of the annealing furnace, the annealing temperatures reported were the maximum temperatures seen by the sample and the annealing times were the dwell times of the platform at the top level. All anneals took place in an nitrogen ambient where the oxygen concentration was kept below 10^{-9} ppm.

Following annealing, the top dielectric layer, BTO, and the Al electrode are deposited to complete fabrication of the TFEL device. For easier microstructural characterization, half of the device was masked off via a shadow mask. The masked off

portion of the device, referred to as a half-device structure, does not have the top dielectric and conductive layers rendering it electrically inactive.

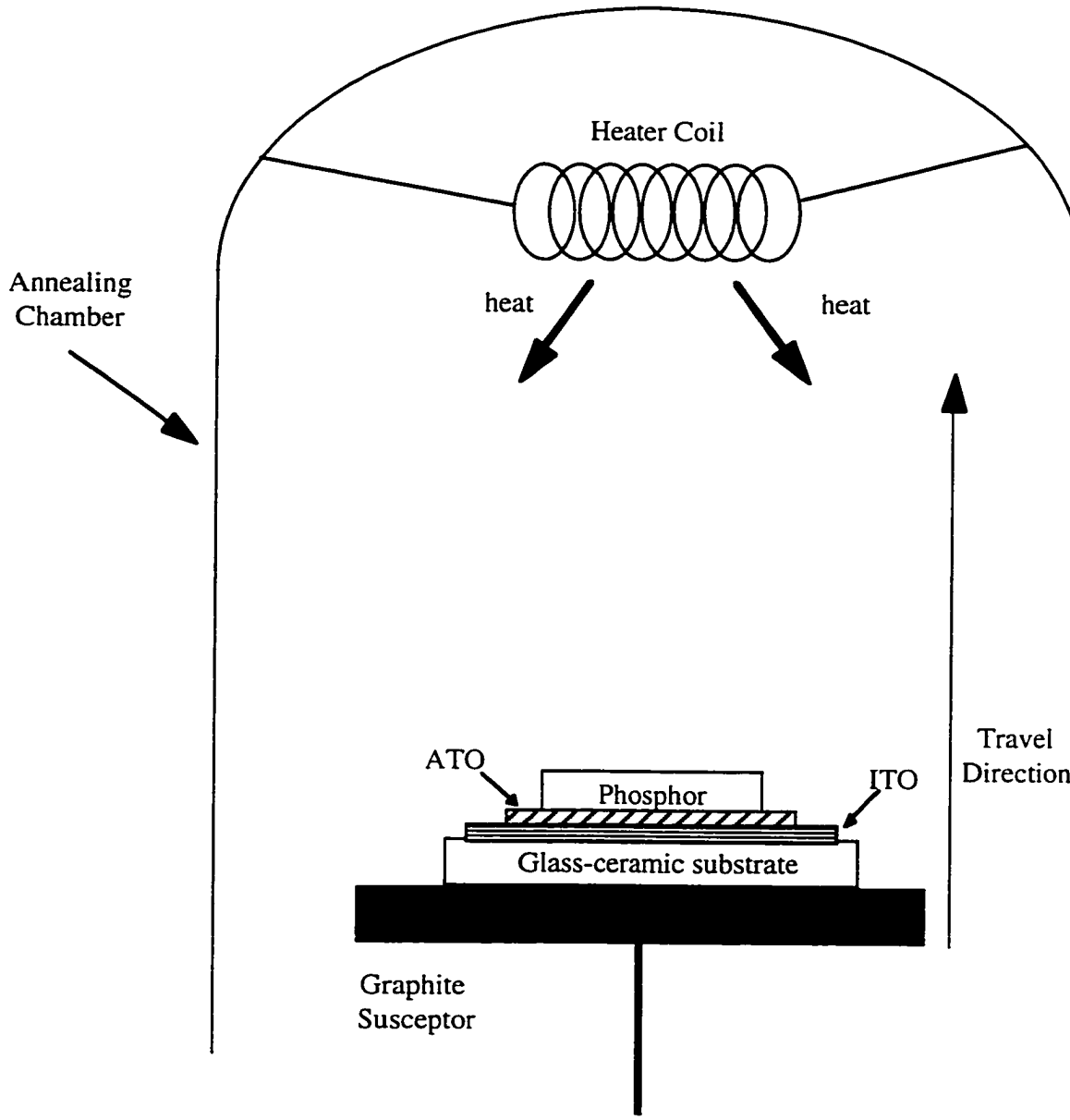


Figure 3-3. Illustration of the post deposition annealing chamber

Characterization

The following section summarizes the characterization techniques utilized in this study (Figure 3-4). Device performance was evaluated by measuring the brightness, efficiency, threshold voltage and emission spectra. The microstructure of the thin film phosphor layer was evaluated by various analytical techniques. Crystal quality was measured via x-ray diffraction [Cul78]. Chemical composition was measured via secondary ion mass spectroscopy (SIMS) and energy dispersive spectroscopy (EDS) [Bor92] [Rom92]. The film microstructure was characterized using a transmission electron microscope (TEM) [Wil96].

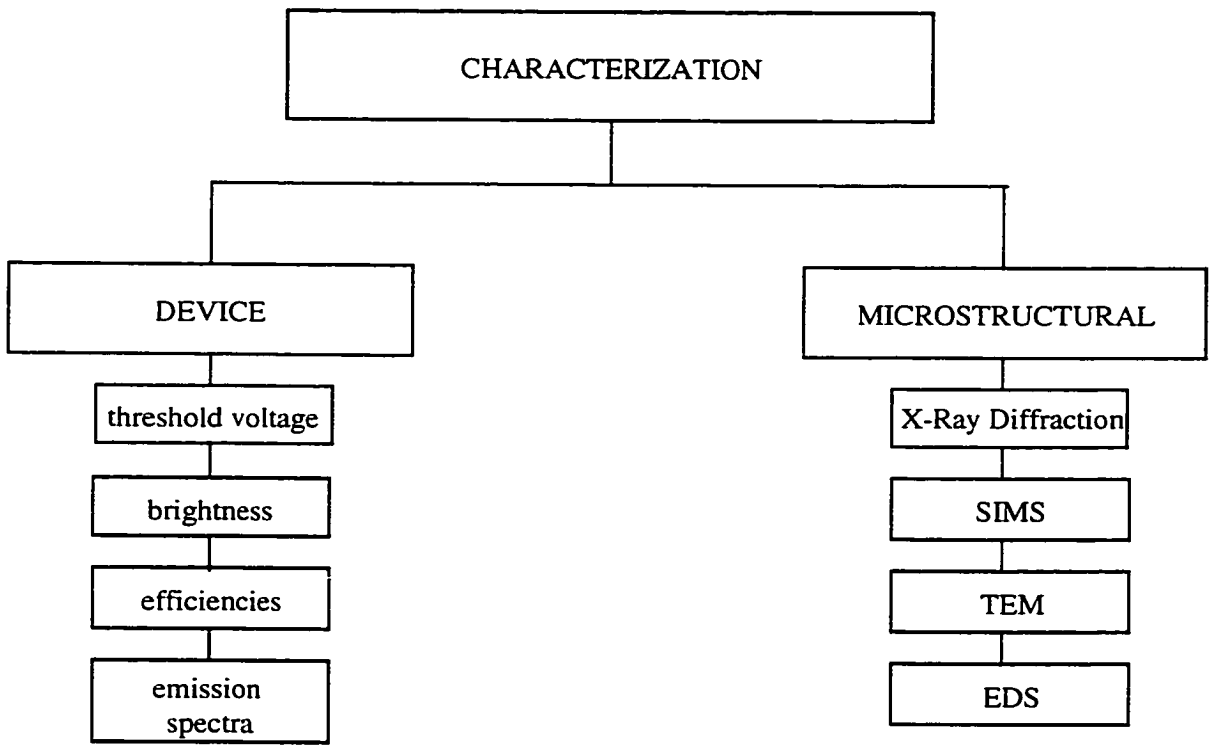


Figure 3-4. Outline of the characterization techniques used in this study

Device Characterization

Electrical and optical characterization of the TFEL device was performed at Planar America. Electrical characterization was limited to the determination of threshold voltage. Optical characterization included measurement of the brightness at forty volts above threshold (L_{40}), the luminous efficiency and the emission spectra.

Completed TFEL devices were connected to a function generator (Wavetek Model 395) which supplied excitation pulses to the device in the form of a square wave with a 30 μs peak duration and a 5.0 ms delay between pulses. Light generated from the TFEL device was converted into a brightness signal. TFEL threshold voltage was determined by calculating the intercept of the extrapolation of the steepest slope of the resulting brightness-voltage (B-V) curve with the voltage axis. The L_{40} was the brightness value at the intersection point between the B-V curve and the threshold voltage plus 40 volts (Figure 2.5). The emission spectra of a TFEL device was determined by using a spectrophotometer (Pitchard 1980B). The luminous efficiency was a ratio between the optical power generated and the electrical power required to generate the light. It is calculated by equation 3.1.

$$\eta_p = L_{40} / (2 f \{C_i^2/(C_i + C_s)\} * V_{th} (V-V_{th})) \qquad (3.1)$$

η_p = photometric efficiency (lumens/watt)
L_{40} = brightness at 40 volts above threshold (lumens)
C_i = capacitance of the dielectric layer (nanofarad/cm^2)
C_s = capacitance of phosphor layer (nanofarad/cm^2)
f = drive frequency (Hz)
V_{th} = threshold voltage (volts)
V = applied voltage (volts)

Microstructural Characterization

Characterization of the phosphor layer microstructure was essential in understanding its role in device performance. Once the electrical and optical characterization had been completed, the microstructure of the phosphor was characterized. Microstructural characterization was usually performed on the half device structure.

X-Ray diffraction

X-Ray diffraction was performed on the samples to measure the crystalline quality of the phosphor layer. As previously discussed, x-ray intensities directly correlated to device performance . In addition to providing a quick measure of crystalline quality, x-ray diffraction also yielded information on the crystalline lattice structure as well as phase identification and phosphor film texture.

Half device samples were cut into test samples (10 mm x 15 mm) and loaded into the x-ray diffractometer (Phillips APD 3720). A copper target operated at 40 KV and 20 mA was used to generate the K_α and K_β x-rays used for the analysis. Scans were taken from 10-65° at step sizes of 0.05° with a dwell time of one second.

SIMS

Initially, SIMS analysis was performed to study any possible migration of species in the double layer experiments. It proved effective not only with the double layer samples but all the samples containing gallium. SIMS analysis was performed on a Perkin

Elmer PHI 6600. Square samples approximately 3 mm x 3 mm were used. A cesium ion sputtering source was used to sputter the surface of the film at an energy of 5 kV and a current of 100 nA at a sputtering angle of 60.8°.

Transmission electron microscopy

Due to scale of the features to be studied, the primary tool used for mircostructural analysis was the TEM. Several microscopes were utilized in this study (JEOL 200, JEOL 4000, Phillips CM-12). The JEOL 200, tungsten filament TEM, was operated at an accelerating voltage of 200 KV. The JEOL 4000 TEM was used for high resolution analysis of the grains, grain boundaries and interfaces. The added feature of the EDS detector on this instrument allowed for chemical analysis of the observed region. The Phillips CM-12 was used for chemical mapping of the grain-grain boundary interface. The CM-12 is a field emission instrument which allows for much greater probe currents at smaller beam sizes, which in turn result in better signal to noise ratio for the EDS detector.

Unlike other microscopy techniques, transmission electron microscopy requires that the specimen to be analyzed be thin enough for electron transmission. While the maximum thickness for electron penetration is a function of many parameters including the atomic structure of the sample and the wavelength of penetrating electrons, samples typically had to be below 2000Å in thickness in order for analysis [Wil96]. This requires extensive sample preparation which is discussed in detail in the following section.

TEM Sample Preparation

In order to completely characterize the microstructure of the phosphor layer, two types of TEM samples based on two orientations were used, plan-view and cross-sectional. Schematics of the two orientations are shown in Figure 3-5. The plan-view orientation is analogous to looking down on the surface of the film. Plan-view samples were used to determine the in-plane grain morphologies as well as the grain size distribution. The cross-sectional orientation is analogous to looking at the sample edge on. Cross-sectional samples were used to determine the cross-sectional grain morphology, layer thickness as well as interface morphology.

Early work with the SrS:Ce phosphor system had clearly shown the deleterious effects that prolonged exposure to both acetone and water had on the samples. Therefore, care was taken to ensure that significant decomposition of the SrS:Ce phosphor layer did not occur.

The first steps in TEM sample preparation were mechanical grinding and polishing of the sample in order to thin the sample. Ideally, the thinned sample would be between 15 and 30 μm. The thinned sample was then ready for ion milling. The purpose of ion milling was to create a hole in the sample via bombardment of Ar^+ ions at low angles. The milling angle is defined as the angle at which the Ar^+ ions strike the sample surface and the plane of the sample. The guns are configured so that the milling angle can be adjusted from 12-20° and the energy and flux of the Ar^+ ions can be controlled. Due to the low angle operation, the area adjacent to the hole will be thin enough for electron transparency. All glass-ceramic substrate samples had an average milling rate of 1μm/hr while being milled from both sides at 15° at 4 KV and 1 mA.

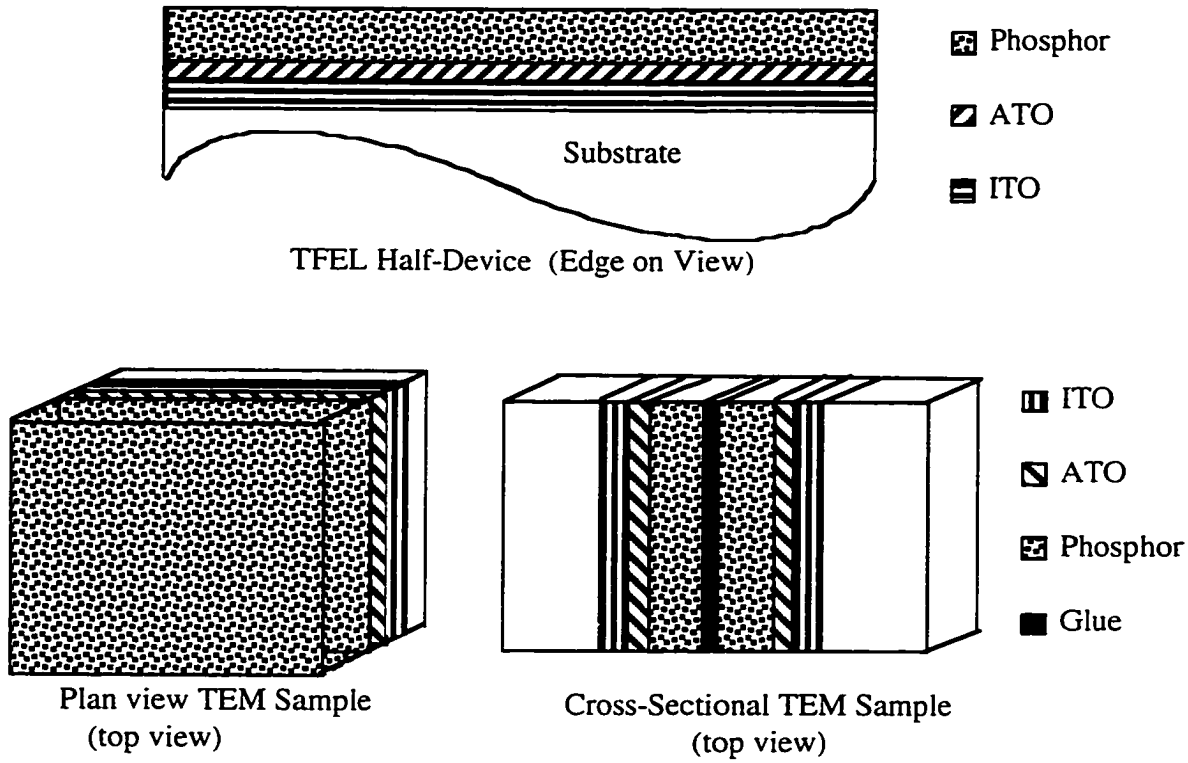


Figure 3-5. Schematic illustration of two types of TEM sample orientations used in this study

Plan-view TEM sample preparation. Since the devices were grown on a transparent glass substrate, it was essential to differentiate between the film and substrate side. The film side of a TFEL sample was identified using an ultra-violet lamp with a highest intensity emission wavelength of 254 nm (UVP Mineralight, model UVGL-25) . This procedure took advantage of the photoluminescent properties of the electroluminescent phosphor. By exposing the film side to the UV lamp, the phosphor would emit a characteristic light depending on its composition. This procedure was used repeatedly in the sample preparation process in order to ensure that the phosphor film had not been damaged or destroyed. A 10 mm x 10 mm sample from the original TFEL device was fractured using a diamond tip scribe. The sample was mounted to a steel

sample mount, film side down, using a thermoplastic adhesive (Crystalbond 509). The steel sample mount was then attached to the lapping fixture (South Bay Technologies, model 150).

An automatic grinding wheel was used to thin the sample. In the operation of the grinding wheel, care was taken to ensure that the water flow was optimized to avoid thermal failure as a result of too low a flow or hydroplaning of the lapping fixture as a result of too high a flow. The grinding procedure began with the use of 320 grit grinding/polishing paper (Buehler Microcut silicon carbide) to thin the sample from the original thickness of greater than 2000 μm to 500 μm. The thickness of each sample was measured using an optical microscope (Nikon). This thinning process could be accelerated by applying some downward force on the lapping fixture. Once the sample was approximately 500 μm, a succession of grinding papers starting with 400 grit and progressing through 600, 800 and finally 1200 grit were used to polish the sample and remove any surface imperfections.

The square sample was then removed from the steel mount and attached, film side down, on a glass slide using the Crystalbond. The slide was then placed in a sample holder specifically designed for a precision coring drill (VCR Group, model V7100). A 3.05 mm diamond coring drill bit (VCR Group) along with 3 μm polycrystalline diamond slurry (VCR Group) was used to core out several 3 mm diameter disc samples. These discs were placed on a hot plate at approximately 250 °F to aid in the removal of any slurry and adhesive residue. A small amount of acetone was used to remove any remaining Crystalbond from the sample surface. Prolonged exposure to the acetone was avoided. The cored sample discs were thinned to approximately 100 μm thickness via the

grinding/polishing procedure described above. The resulting disc measuring between 90 and 130 μm in thickness was ready for the mechanical dimpling stage. Figure 3-6 illustrates the steps described so far.

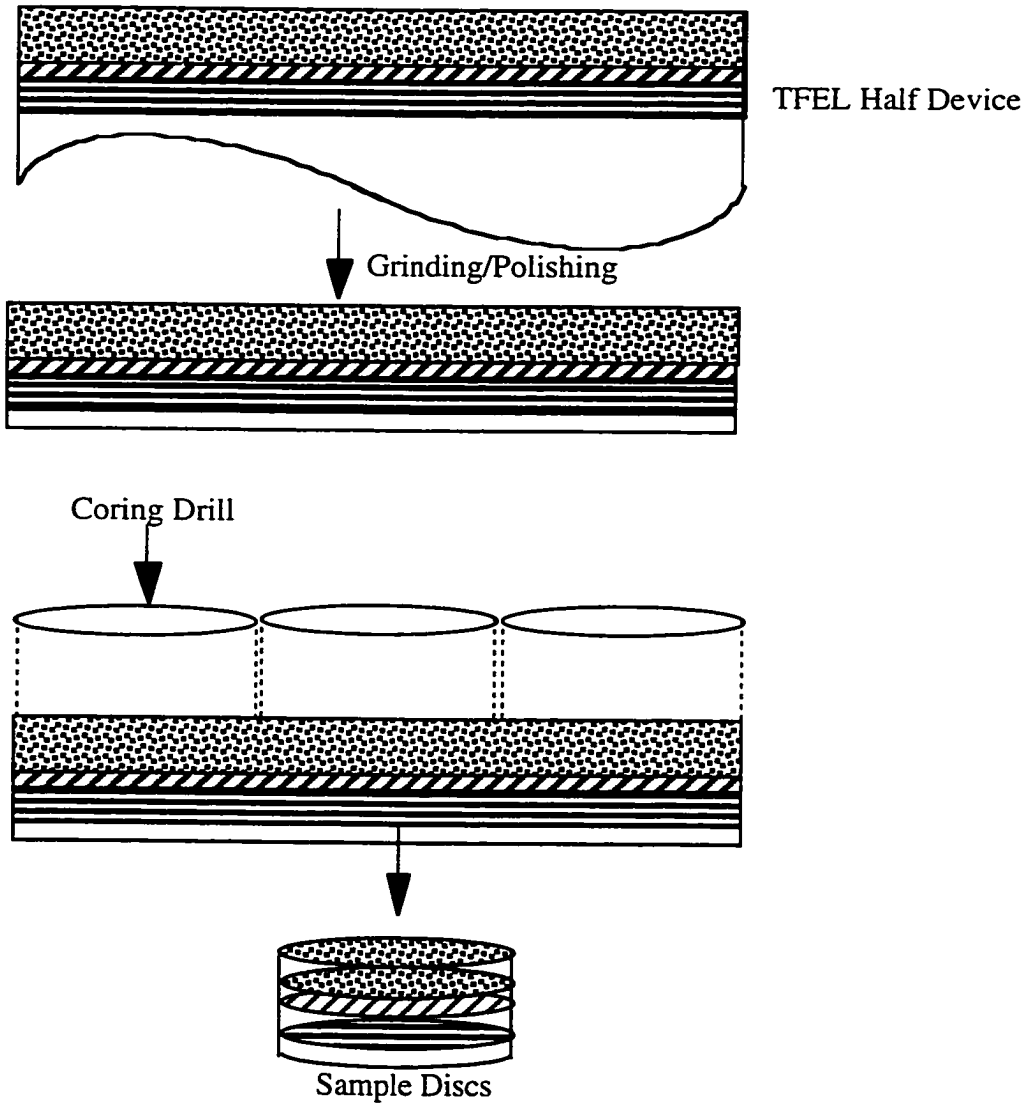


Figure 3-6. Schematic representation of the TEM sample preparation procedure

Mechanical dimpling is used to further thin the sample (Figure 3-7). A dimple approximately 0.5 mm in diameter is formed by a polishing wheel and abrasive slurry (3 μm water based polycrystalline diamond suspension). The 3 mm diameter sample disc is placed in a sample holder specifically designed for the dimpler (VCR Group model D500i). With the dimpler set at a force of 50 g and a speed of 40 rpm, the sample was dimpled to approximately 40 μm in 10 μm increments. An optical microscope was used to measure the difference between the dimple center and the outer edge. Careful monitoring of the sample was required at a thickness below 40 μm because the risk of catastrophic sample cracking. Further dimpling was performed using a 1 μm water based polycrystalline diamond suspension. The dimpled disc was then ready for the final stage of the TEM sample preparation process, ion milling.

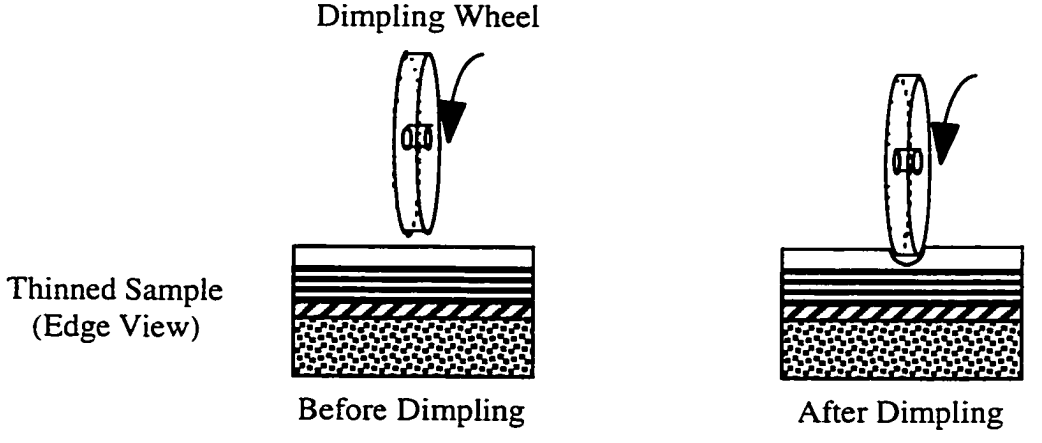


Figure 3-7. Schematic representation of the mechanical dimpling procedure

The dimpled TEM sample was placed in an ion milling specimen holder (Gatan), film side down, and placed in the ion mill (Gatan Duo-mill, model 600). The ion milling schedule that was utilized is listed in Table 3.2. Since the samples were plan view, only the substrate side of the sample was milled. Therefore, only the top gun was used to ensure milling of the substrate. In order to expedite the milling procedure, a high angle of 19° was chosen as the initial milling angle with a gun voltage of 4 KV and a gun current of 1mA. Careful monitoring of the sample was necessary in order to ensure that too steep a hole would not develop. Once a hole was detected, the milling angle was reduced to 12° and the sample was milled for an additional 30-45 minutes. Finally, in order to remove any debris that may have re-deposited during the milling process, the sample was milled from both sides at 12° for approximately 10 minutes.

Table 3.2. Milling procedure for plan-view TEM samples.

Ion guns	Milling Angle	Voltage/ Current	Time
top gun	19°	4 kV/ 1mA	3 hrs. or until hole formation
top gun	12°	4 kV/ 1mA	30-45 minutes
top and bottom guns	12°	4 kV/ 1mA	10 minutes

Cross-sectional TEM sample preparation. Cross-sectional samples were made by attaching two pieces of the TFEL device together. Half device samples measuring 10 mm x 10 mm, are glued phosphor film side to phosphor film side with G1 adhesive (Gatan). The composite is placed in a vice and annealed in an oven at 110 °C under pressure for two hours. The cured composite is then diced with a low speed saw into 1.5 mm strips.

These strips are then cored into circular samples. A similar procedure to the one described for the plan view samples is used to core the strips.

The cored disks are thinned using a succession of finer grit sand paper (400, 600, 800 and 1200). In order to avoid debonding of the individual strips, care must be taken to thin and polish along the glue line of the sample. In other words, the polishing direction must be parallel to the glue line and must remain constant. After polishing, to a thickness of approximately 200 μm , the disk is then flipped over and subjected to the same polishing procedure. The final thickness of the disk is approximately 100 μm. The disk is then dimpled using the same procedure described above. Dimpling should result in a disc with a minimum thickness ranging from 25 to 40 microns.

Dimpled cross-sectional TEM samples were affixed on an ion milling specimen holder and placed into the ion mill. The ion milling schedule utilized for the plan view TEM samples was used, however both top and bottom guns were used. In order to expedite the milling procedure, a high angle of 19° was chosen as the initial milling angle with a gun voltage of 4 kV and a gun current of 1mA. Careful monitoring of the sample was necessary in order to ensure that too steep a hole would not develop. Once a hole was detected, the milling angle was reduced to 12° and the sample was milled for an additional 30-45 minutes.

CHAPTER 4
SrS:Ce TFEL DEVICES

Introduction

Presented in this chapter are the results of the characterization experiments performed on TFEL devices which contain SrS:Ce as the phosphor layer. These results will serve as a baseline for comparing the effects of additions of gallium and excess sulfur on TFEL device performance reported in chapter five. The electrical and optical properties are first reported, followed by the microstructural properties. A discussion of the data concludes this chapter.

Results

The phosphor layer of the single layer devices studied consisted of a 1μm film of SrS:Ce. A schematic of the device architecture is shown in Figure 4-1. As stated earlier, previous studies have shown that post deposition annealing was required for optimum device performance. Three annealing temperatures (650°C, 750°C and 810°C), along with the as-deposited device, were used to study the effect of the annealing temperature on the device properties. This section reports the effect of annealing temperature on the threshold voltage, brightness, luminous efficiency and emission spectra.

SINGLE LAYER DEVICES

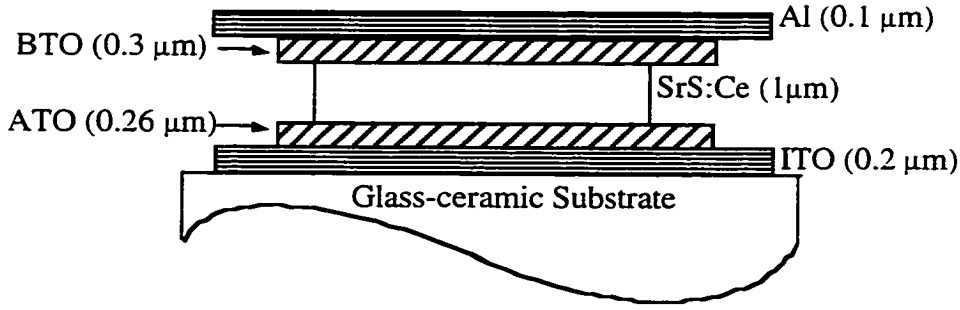


Figure 4-1. Single layer TFEL device architecture

Threshold Voltage

The threshold voltage as a function of annealing temperature is plotted in Figure 4-2. It is clear that post deposition annealing significantly reduced the threshold voltage. The 810°C anneal resulted in the lowest threshold voltage of 150 volts.

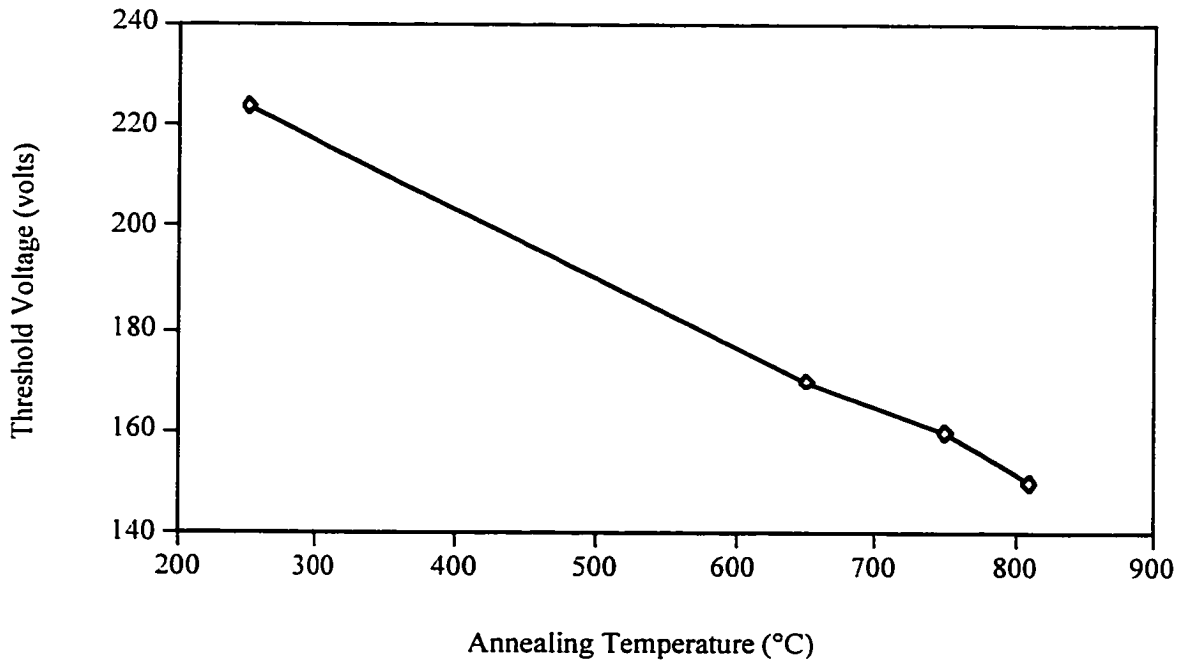


Figure 4-2. Relationship between the threshold voltage and the annealing temperature for single layer SrS:Ce TFEL devices

Brightness

The effect of annealing temperature on the brightness, as characterized by the L_{40} value, is shown in Figure 4-3. As in the case of the threshold voltage, post deposition annealing had a significant effect on the brightness. Annealing at 810°C resulted in greater than a five fold increase in the brightness, compared to the as deposited condition, with a maximum measured L_{40} of 26.2 cd/m^2.

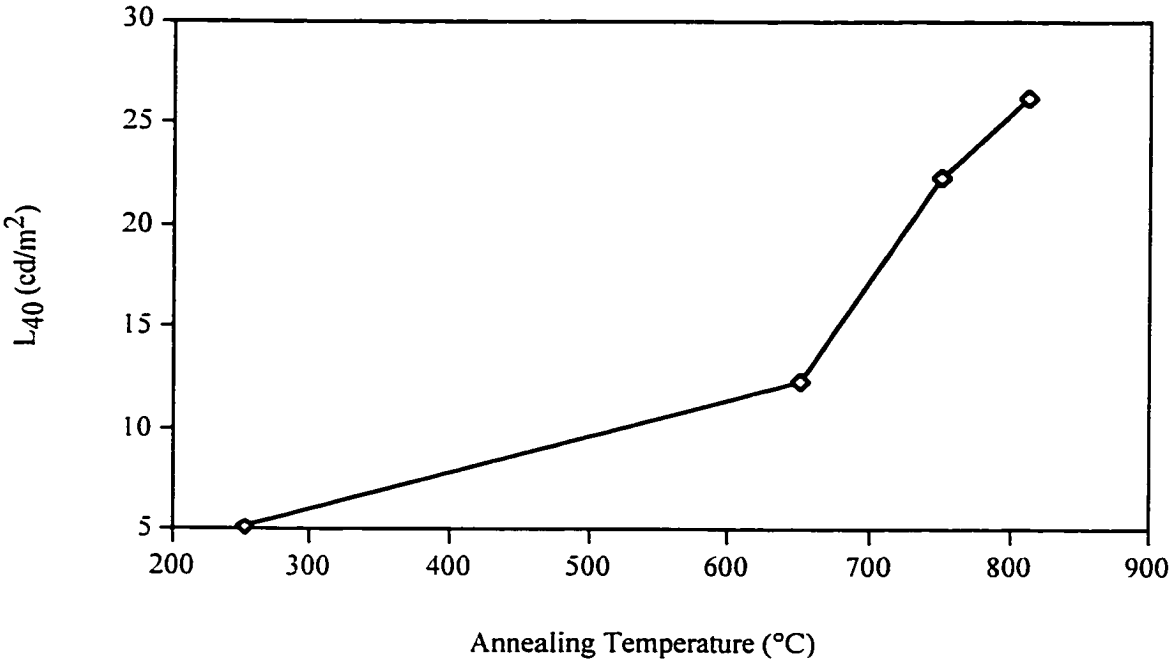


Figure 4-3. Relationship between L_{40} and the annealing temperature for single layer TFEL devices

Luminous Efficiency

As seen in Figure 4-4, post deposition annealing also resulted in significant improvement in the luminous efficiency of the single layer TFEL device. The luminous efficiency in the 810°C annealed single layer TFEL device was 0.14 lumens/watt (l/w), which was more than three times greater than the luminous efficiency of the as-deposited single layer TFEL device.

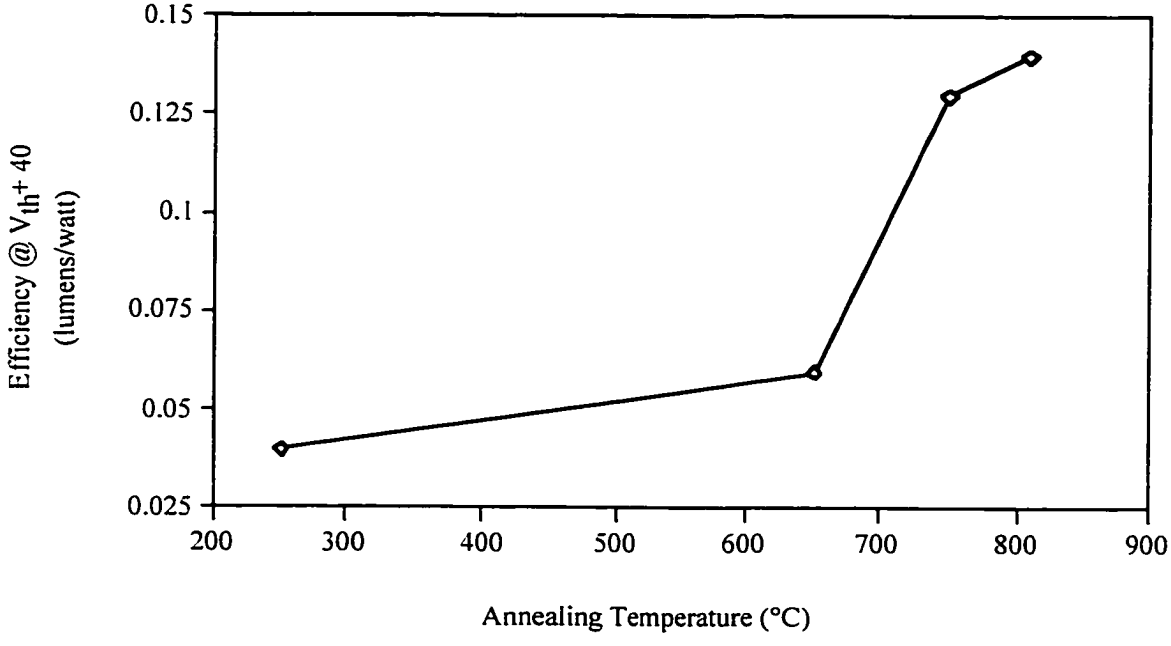


Figure 4-4. Relationship between luminous efficiency (at the threshold voltage + 40 volts) and the annealing temperature for single layer TFEL devices

Emission Spectra

The emission spectra as a function of annealing temperature is plotted in Figure 4-5. The peak emission of the as-deposited single layer TFEL device was 480 nm while the peak emission of the single layer TFEL device annealed at 810°C was 476 nm. This shift in the peak emission towards shorter wavelengths is referred to as a blue shift. The corresponding CIE coordinates for the single layer TFEL devices are listed in Table 4-1. The CIE coordinates are also plotted on a CIE diagram in Figure 4-6.

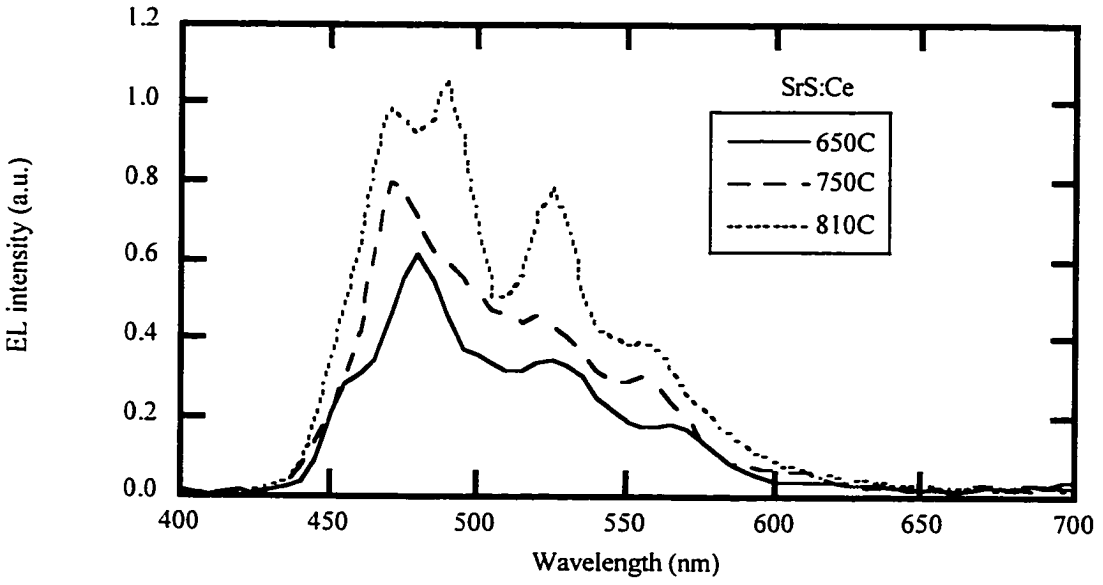


Figure 4-5. Emission spectra for single layer TFEL devices as a function of post deposition annealing temperature

Table 4-1. CIE coordinates measured for the annealed single layer TFEL devices.

Annealing Treatment	Peak Emission Wavelength (nm)	CIE Coordinates (x,y)
As-Deposited	480	(.24,.39)
650°C/120s	480	(.21,.37)
750°C/120s	478	(.20,.36)
810°C/120s	476	(.20,.36)

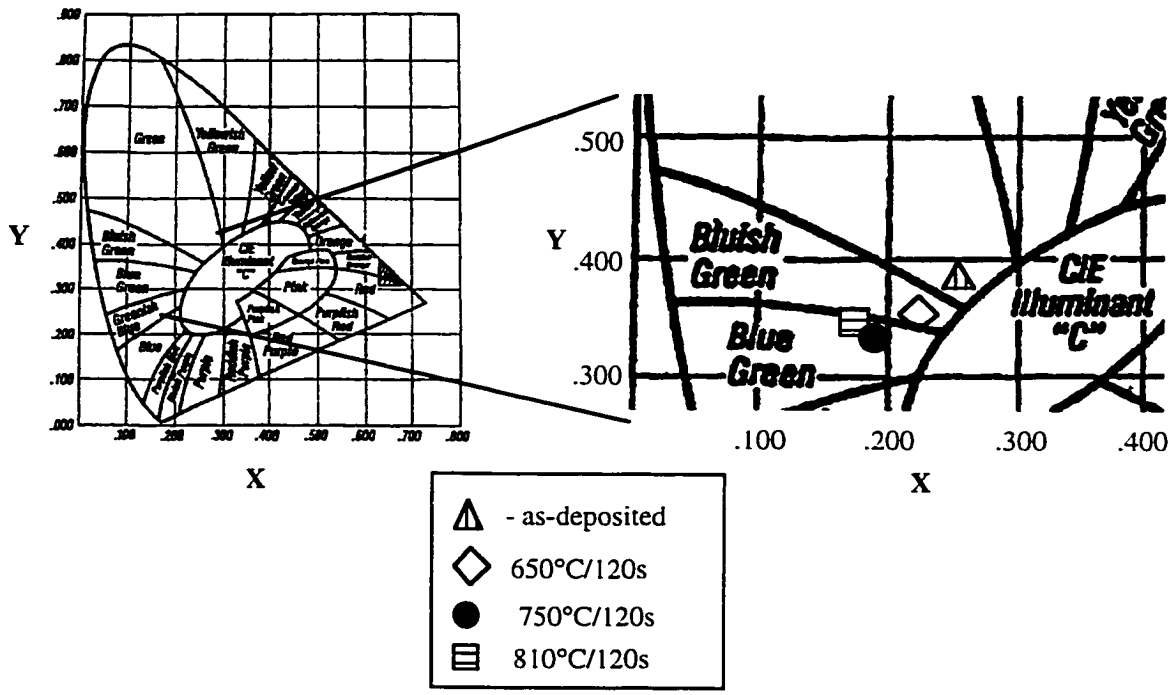


Figure 4-6. CIE Diagram with the coordinates measured for the annealed single layer devices

Microstructural Characterization

Data, from the electrical and optical characterization experiments, show that post deposition annealing led to significant improvement in TFEL device properties. In order to better understand the reasons for the improvement, the effect of the annealing on the phosphor layer microstructure was investigated. This section will present data from XRD, SIMS and TEM analysis performed on the single layer TFEL devices.

X-Ray Diffraction

The results from the XRD analysis performed on the single layer devices are listed in Tables 4-2, 4-3, 4-4 and 4-5. The SrS:Ce films, regardless of the annealing temperature, were textured with a preferred (220) crystallographic orientation. The full width at half maximum (FWHM) of the (220) peak decreased with increasing annealing temperature as seen in Figure 4-7.

Table 4-2. XRD summary table for as-deposited single layer TFEL device.

Angle	D-Spacing	Intensity	Peak
42.26	2.1368	100	SrS (220)
29.61	3.0143	35.65	SrS (200)
25.45	3.4964	27.06	SrS (111)
30.44	2.9344	19.32	ITO

Table 4-3. XRD summary table for single layer TFEL device annealed at 650°C/120s.

Angle	D-Spacing	Intensity	Peak
42.47	2.1269	100	SrS (220)
29.76	2.9999	65.37	SrS (200)
39.325	2.2893	31.70	ITO
25.63	3.4732	21.30	SrS (111)

Table 4-4. XRD summary table for single layer TFEL device annealed at 750°C/120s.

Angle	D-Spacing	Intensity	Peak
42.52	2.1245	100	SrS (220)
29.78	2.9977	42.06	SrS (200)
25.68	3.4666	33.06	SrS (111)
36.21	2.4789	24.56	ITO

Table 4-5. XRD summary table for single layer TFEL device annealed at 810°C/120s.

Angle	D-Spacing	Intensity	Peak
42.47	2.1265	100	SrS (220)
29.65	3.0108	31.17	SrS (200)
35.29	2.5411	20.19	ITO
61.64	1.5035	7.12	SrS (400)

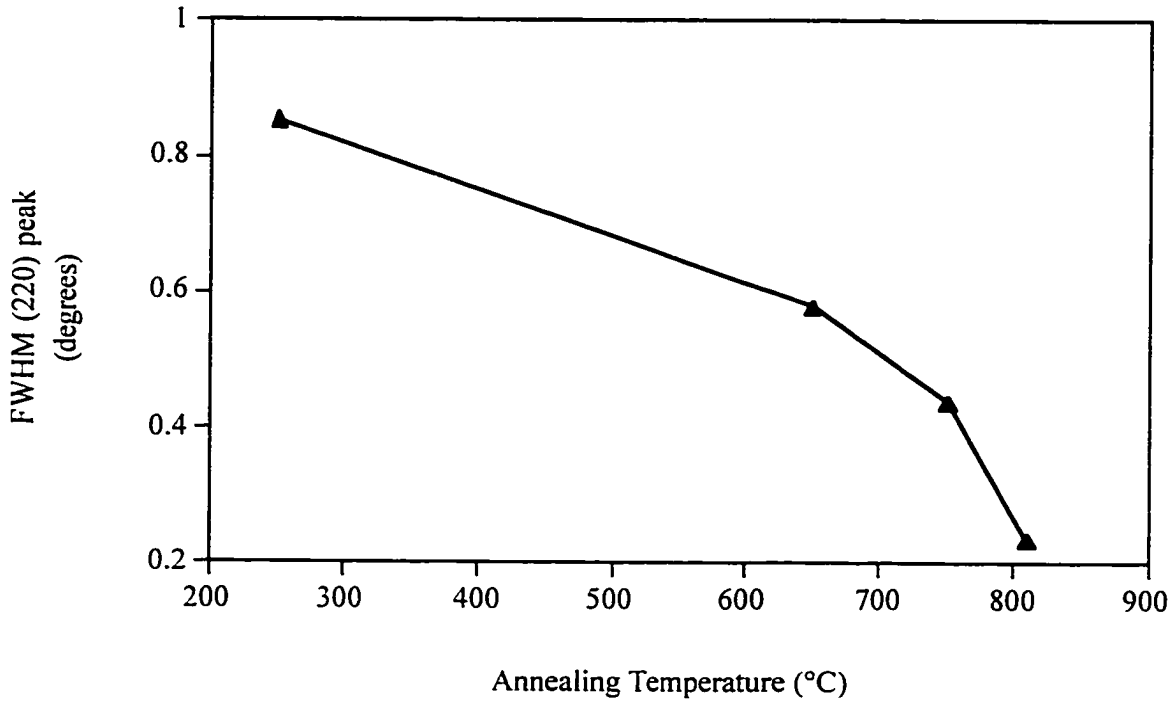


Figure 4-7 FWHM of the SrS:Ce (220) peak as a function of post deposition annealing temperature

SIMS

SIMS analysis was performed on the as-deposited and 810°C annealed films. The SIMS profiles, given in Figure 4-8, show no significant change after annealing. Both profiles show that the levels of strontium, sulfur and cerium remained constant throughout the phosphor layer.

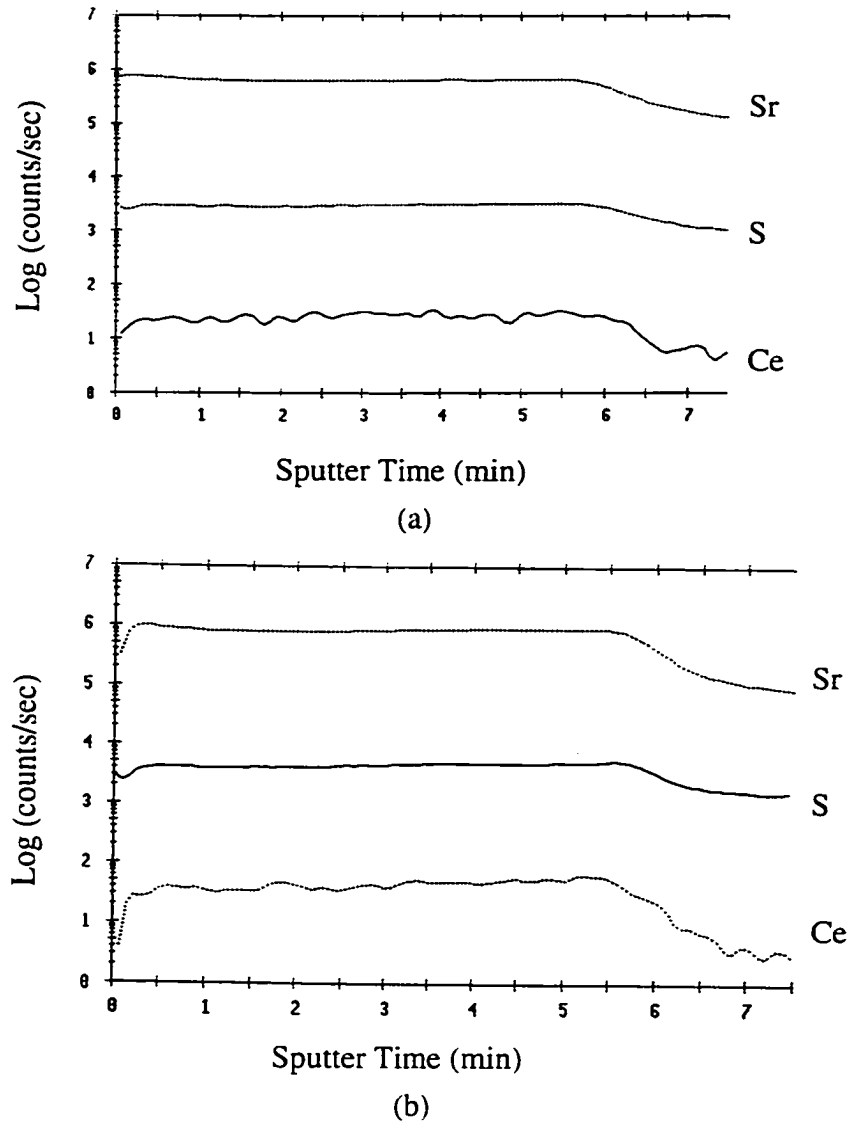


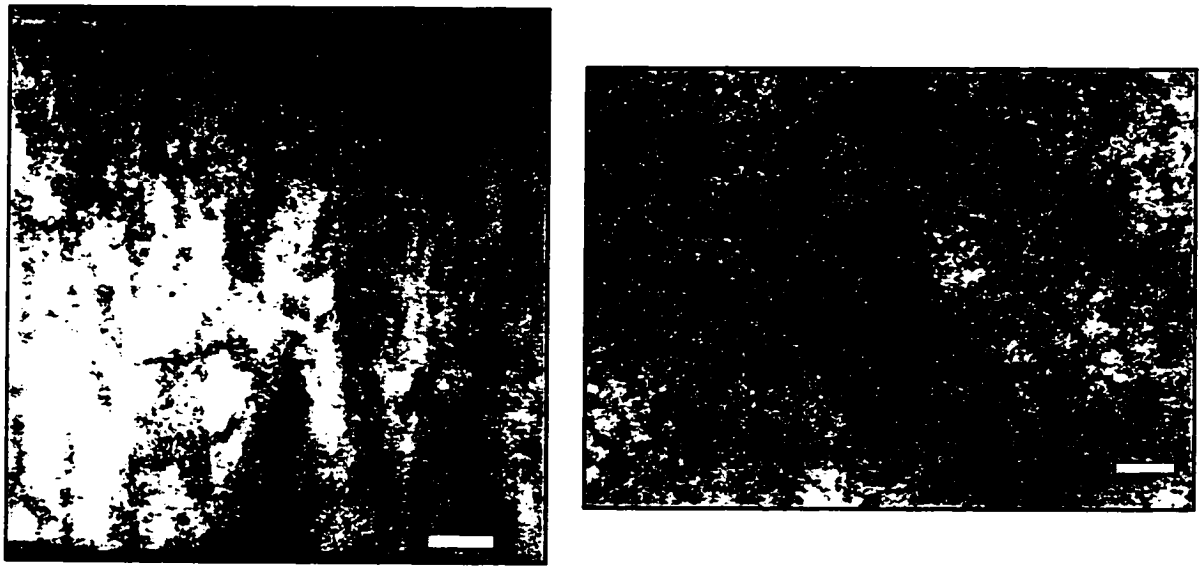
Figure 4-8. SIMS profiles of the phosphor layer in an (a) as-deposited and (b) 810°C annealed single layer TFEL device

TEM

The primary focus of the TEM analysis was the characterization of the microstructure of the SrS:Ce layer namely, the grain morphology and grain size. TEM micrographs representative of the as-deposited and 810°C annealed single layer devices are shown in Figures 4-9 and 4-10.

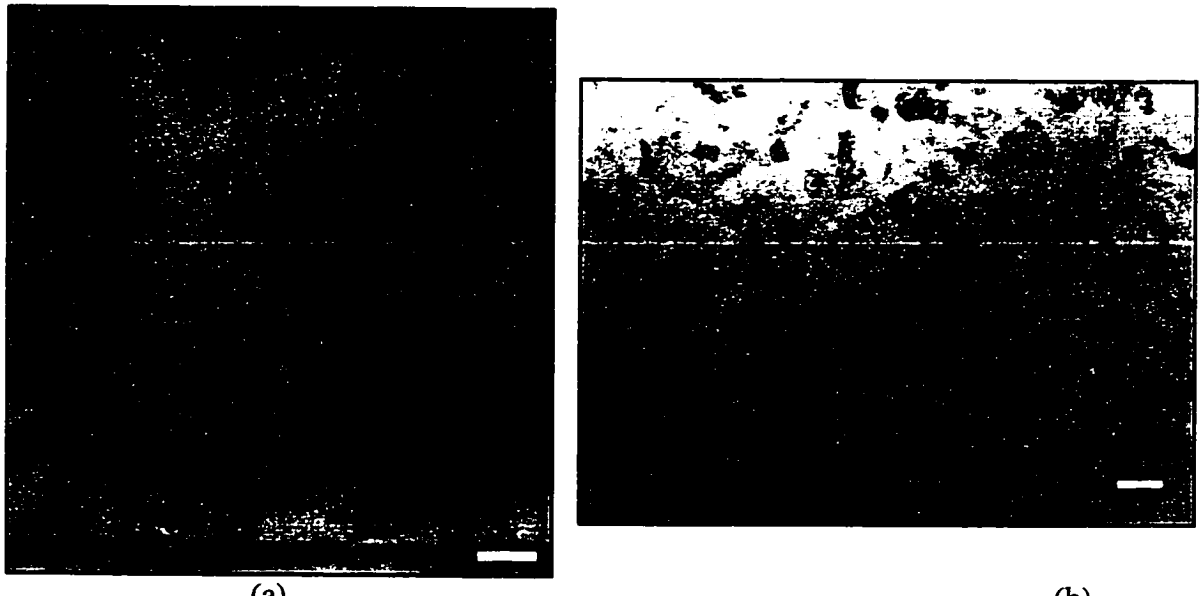
The combination of plan and cross-sectional views of the SrS:Ce layer yields information on the grain morphology. It is clear that regardless of the heat treatment, the grains maintained a columnar grain morphology. Dark field transmission electron microscopy was utilized to highlight the individual columnar grains. In this technique, a beam diffracted by a particular grain is used to image the sample whereas in bright field transmission electron microscopy, the transmitted beam is used to image the sample. A bright field micrograph and the corresponding dark field micrograph of the same region are presented in Figure 4-11 in order to highlight the columnar grain morphology.

The mean grain size was determined via measuring several grain diameters from plan-view TEM micrographs. The grain size as a function of annealing temperature is plotted in Figure 4-12. The standard deviation is plotted as the error bars. The average grain size increases from 150 ± 100 Å for the as-deposited sample to 900 ± 200 Å for the sample that was annealed at 810°C.



(a) (b)

Figure 4-9. TEM micrographs of the as-deposited phosphor layer (a) cross-section sample and (b) plan view sample



(a) (b)

Figure 4-10. TEM micrographs of the phosphor layer annealed at 810°C/120s (a) cross-section sample and (b) plan view sample

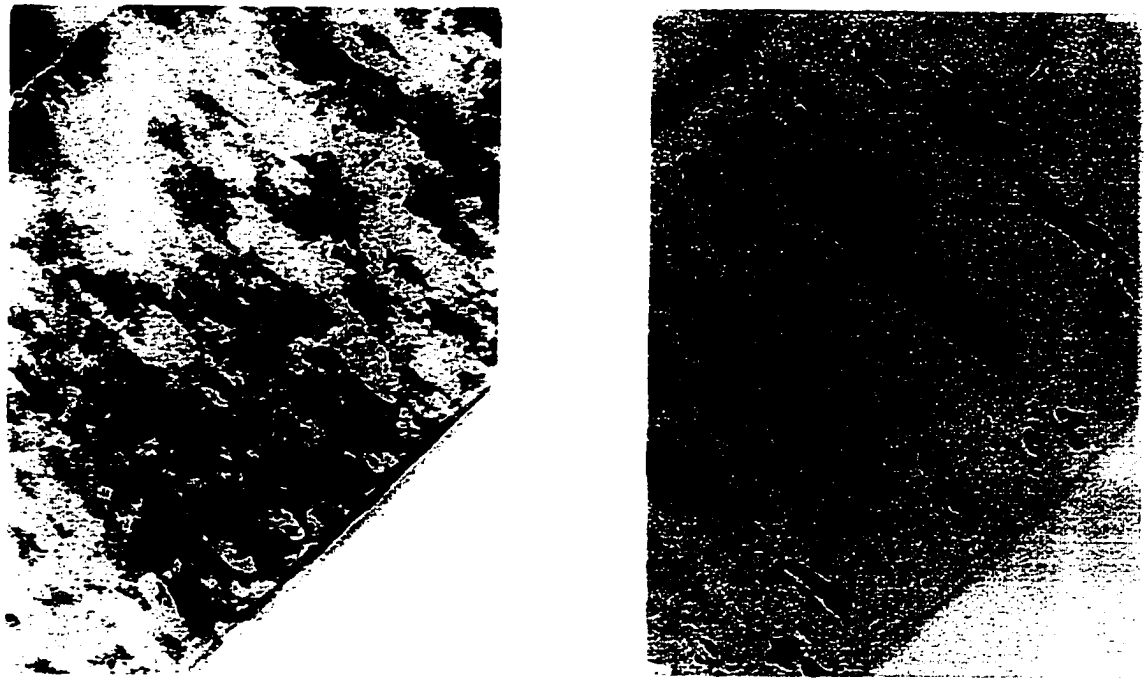


Figure 4-11. SrS:Ce layer imaged under (a) bright field and (b) dark field

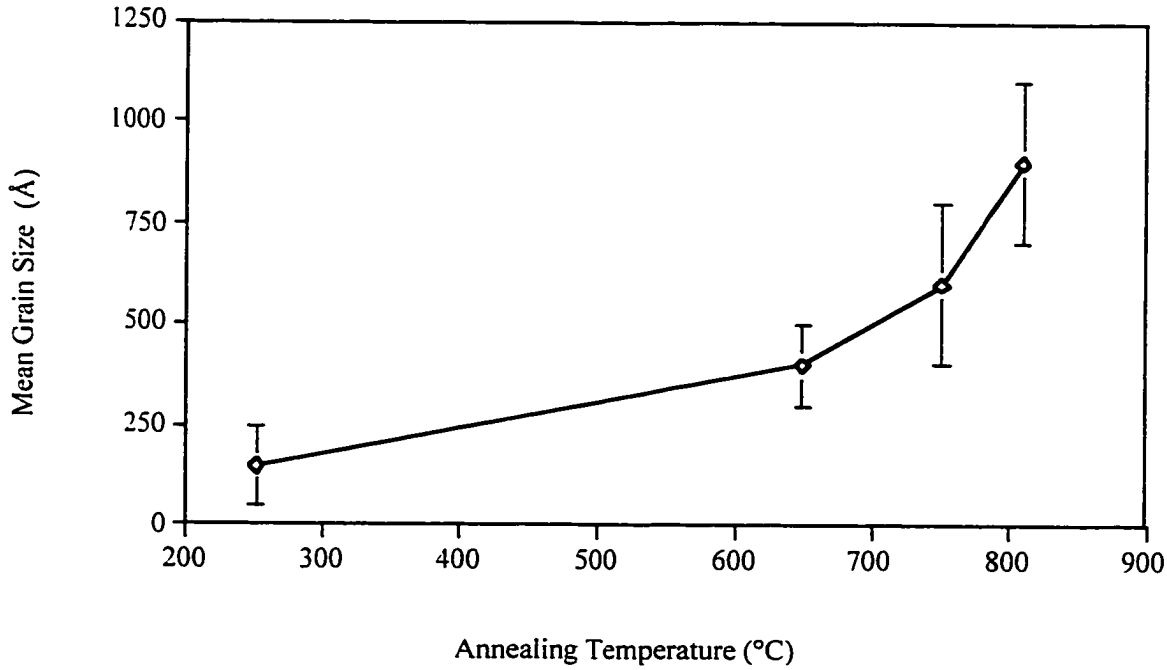


Figure 4-12. Grain size of the SrS:Ce grains as a function of annealing temperature for single layer TFEL devices

Discussion

Post deposition annealing resulted in enhanced device performance as evidenced by Figures 4-2, 4-3, and 4-4. These results agree with previous studies on SrS:Ce TFEL devices which attributed the improved device performance to the improvement in crystalline quality [Oko93], [Ohm95]. In these studies, crystalline quality was evaluated via x-ray FWHM measurements.

Electrical/Optical Properties

The reduction in threshold voltage , as a function of annealing, can be attributed to the improved crystallinity at the phosphor/dielectric layer interface [Ohm95]. Ohmi et al. attributed the reduction of the threshold field with annealing on the increased grain size at the phosphor/dielectric layer interface. The investigators had reported the presence of a thin layer of equiaxed grains (D_{mean} = 700 Å) as seen in an SEM image of the cross-section of the device. This layer was referred to as a dead layer. Upon annealing, grain boundaries between the granular grains were seen to disappear, resulting in a more columnar morphology. No dead layer was observed in our as-deposited single layer device.

Hirabayashi et al. concluded that the dominant factor affecting the threshold voltage was the phosphor layer conductivity, which was proportional to the trapping center densities [Hir89]. Increasing the phosphor layer conductivity would reduce the threshold voltage. While there was no evidence of a dead layer in our samples, we believe that very small grain sizes measured in the as-deposited SrS:Ce films have a similar effect.

We believe that decrease in threshold voltage is due to the increased conductivity in the SrS:Ce film due to the reduction in grain boundary area as a result of grain growth.

The increase in brightness coupled with the increase in luminous efficiency with annealing temperature strongly indicated that annealing had resulted in an improvement in crystal quality of the SrS:Ce phosphor layer. The increase in luminous efficiency suggests that a greater amount of the luminescent Ce^{3+} centers are undergoing radiative decay. Since crystallographic defects such as point defects, grain boundaries and dislocations are typically associated with the promotion of non-radiative decay [Ohm95], we suggest that the reported increase in crystalline quality and increase in SrS:Ce grain size are primarily responsible for the improved brightness and luminous efficiency.

The shift in emission spectra towards shorter wavelengths is not readily understood. As discussed earlier, the emission associated with any TFEL device is dependent on the activator ion used. The shift in EL emission suggests that the local Ce^{3+} environment was altered as a result of annealing. Rack et al. proposed that the observed shifts in the EL spectra are due to the removal of non-radiative centers (point defects, line defects and grain boundaries) [Rac96(2)].

Microstructure

The as-deposited structure was crystalline in nature as evidenced by both the XRD analysis as well as the TEM analysis. The narrowing of the FWHM of (220) peak with annealing temperature as shown in Figure 4-6 confirms that annealing led to an improvement in crystalline quality i.e., reduction in the inherent strain induced defect concentration in the as-deposited SrS:Ce thin film.

The use of the FWHM as a measure of crystalline quality is based on the principle that a more perfect crystal results in a narrower and sharper x-ray reflection due to less scattering of the incident x-rays. The primary source of imperfections that lead to scattering is residual stress in the sputter deposited film. The preferred orientation of the SrS:Ce layer was along the (220) crystallographic direction. This result is contrary to the work of Yoshiyama et al., who used surface energy calculations to study the growth mechanisms for ZnS, CaS and SrS evaporated films [Yos88]. The investigators concluded that the most favorable plane for evaporated SrS films was the (200) orientation, when the substrate temperature is held below 400°C, with a subsequent switch to a (220) orientation at higher substrate temperatures. The substrate temperature for our experiments was 250°C. The discrepancy in the film texture may be attributable to the fact that Yoshiyama et al., studied evaporated films in which the incident flux of material is much less energetic than the incident flux of atoms in sputter deposited films. For evaporation, the average kinetic energy of evaporant atoms is reported to be 0.1 eV while the kinetic energy associated with sputtered atoms can range from 2-30 eV [Ohr92]. This energy difference could explain the different textures since higher energies could supply enough energy for the (220) crystallographic orientation otherwise seen at only higher substrate temperatures.

Grain Growth

The as-deposited SrS:Ce columnar grain morphology agreed with the model proposed by Thorton [Ohr92]. Under the growth conditions employed in this study, Thorton's model would predict a Zone T microstructure which is defined as a dense array

of poorly defined, very narrow columnar grains with no voids present between the grains. Analyzing the plan view TEM micrographs, the as-deposited grain diameter was an average of 150 Å with no voids present between individual grains. Annealing did not result in a change in grain morphology: columnar SrS:Ce grains were still observed after the 810°C anneal. The observed columnar grain morphology is similar to the one reported by other investigators [Hua94], [Hsi95]. While Hua et al., made no mention of voids between the columnar grains, Hsieh et al., reported the presence of voids in between the columnar grains and suggested that the voids resulted from stresses due to the thermal expansion mismatch between the film and substrate. The substrate temperature (600 °C) used by Hsieh at al. may have increased the magnitude of the thermal expansion stress a

Transmission electron microscopy revealed an increase in SrS:Ce grain size as a result of post deposition annealing. The average grain size in the as-deposited structure was 150 Å. Due to the extremely small grain size, the standard deviation of the grain size measurements was relatively large (100Å). The average as-deposited grain size was an order of magnitude smaller than those reported by Hua et al. The discrepancy could be explained by the increased substrate temperature (550 °C) employed by Hua et al. versus the temperature of 250°C used in this study of SrS:Ce thin films. Annealing at 650°C for 120s resulted in grain growth with mean grain size increasing to 400 Å. Further grain growth was observed after a 750°C/120s anneal with the average grain size increasing to 600Å. The largest mean grain size of 900 Å was measured for samples annealed at 810°C for 120s with a standard deviation of 200 Å.

The increase in grain size results in a reduction in grain boundary area. The calculation begins by assuming a phosphor layer volume of 1 μm^3. The calculation of the

grain boundary area involves the calculation of the number of grains that occupy a cubic micron of phosphor layer. This is equal to dividing the phosphor layer volume by the volume of a single columnar grain. Using the measured mean grain diameters from the as deposited and 810°C annealed films, (150Å, 900Å) and a grain length of 1 μm, it was found that there are approximately 5658 SrS grains/μm^3 in an as deposited film and 157 SrS grains/μm^3 in a film annealed at 810 °C. Since the grain morphology is columnar, the grain boundary area associated with a single grain can be determined by obtaining the cylindrical surface area. This number should be divided by two since no voids were found in between the grains and thus all the grains were shared. The total grain boundary area per one cubic micron of phosphor is then obtained by multiplying the total number of grains by the grain boundary area associated with a single grain. For the as deposited phosphor film the total grain boundary area per cubic micron was calculated to be 1.33 * 10^{-6} cm^2 and 2.22 *10^{-7} cm^2. By dividing the total grain boundary volumes, it was found that annealing resulted in a six fold decrease in the grain boundary volume. In order to better understand the role of the microstructure on the TFEL properties, experiments were performed to determine the changes in the Ce^{3+} environment as a result of post deposition annealing.

An Arrhenius equation (equation 4-1) was used to determine the activation energy for the grain growth process. In order to estimate the activation energy for the grain growth process, an Arrhenius plot of the log of the SrS grain size as a function of 1/T was plotted in Figure 4-13.

$$D = k_0 \exp(-Q/2kT) \qquad (4\text{-}1)$$

D = temperature dependent grain size k_0 = constant

Q = activation energy for grain growth T = temperature (°K)

k = Boltzmann constant ($8.617 * 10^{-5}$ eV/°K)

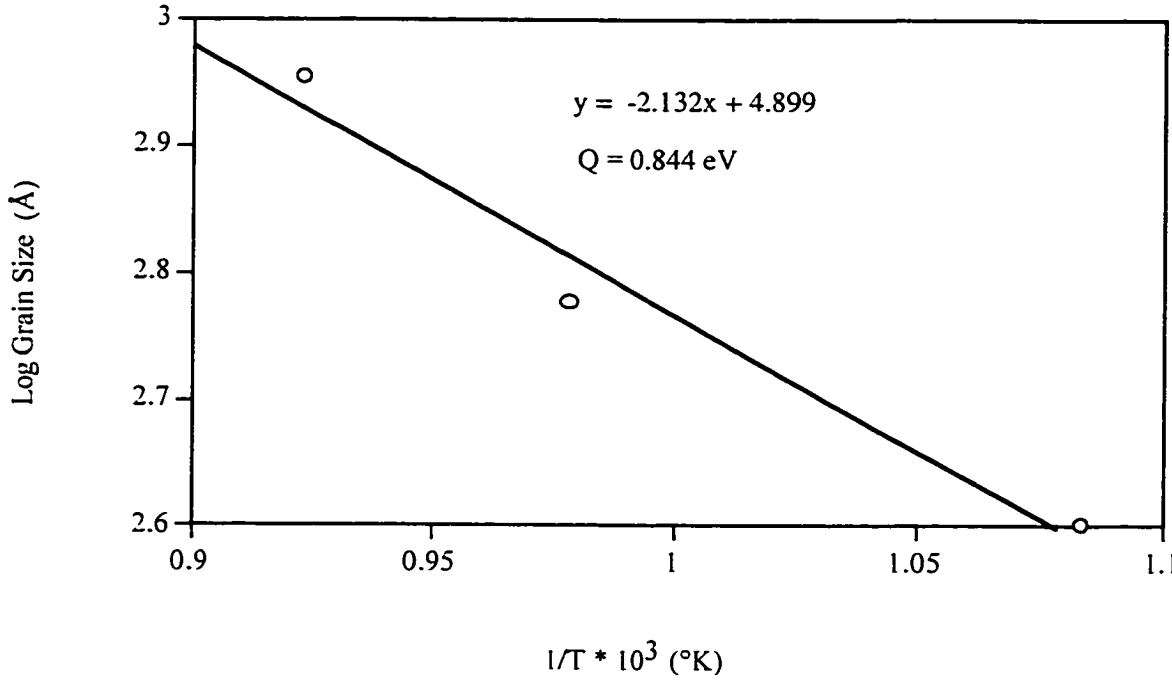


Figure 4-13. Arrhenius plots of the log of the grain size versus the inverse annealing temperature for SrS

The effective activation energy for grain growth in SrS was calculated to be 0.88 eV. No activation energies have been reported for SrS in the literature. A list of grain growth activation energies for other systems is presented in Table 4-6. The value for the effective activation energy derived for SrS is within the range of values shown in this table.

Table 4-6. Grain growth activation energies for various materials.

Material	Activation Energy (eV)	Reference
CdTe	2.5	[Qi96]
ZnO	2.32	[Sen90]
CdO	1.29	[Shi88]
$YBa_2Cu_3O_7$	1.29	[Shin91]
SrS	**0.88**	**this work**
$MoSi_2$	0.66	[Mag84]
As doped poly-silicon	0.42	[Kal88]

Role of Microstructure on Ce^{3+} Environment

Post deposition annealing has been shown to improve the EL efficiency. This suggests that the annealing led to the removal of defects in the SrS:Ce layer. This was confirmed by a narrower FWHM of the x-ray diffraction peak and larger grain sizes associated with the 810°C annealed phosphor layer. These defects, created by the non-equilibrium film growth associated with the sputtering process, can act as non-radiative traps which act to reduce EL efficiency [Hut95]. Electron paramagnetic resonance (EPR) analysis and photoluminescent (PL) studies were performed on the SrS:Ce TFEL devices, in order to correlate the changes in the phosphor layer microstructure to the local Ce^{3+} crystallographic environment.

Warren et al. used EPR to study the local symmetry, oxidation state and atomic site to site fluctuations in the crystal field of the Ce^{3+} ion in the SrS lattice [War97]. The study reported an appreciable increase in the nearly cubic Ce^{3+} concentration and a decrease in the line width of the Ce^{3+} ion resonance with increased annealing temperature (Figure 4-14). The narrowing of the Ce^{3+} EPR line width indicated a more uniform crystal field surrounding the Ce^{3+} ion. The nearly cubic Ce^{3+} density increased from $0.6*10^{19}$

ions/cc for the as-deposited film to $1.6*10^{19}$ ions/cc for the film annealed at 810 °C. It can be concluded, from the EPR results, that the improved SrS:Ce film crystal quality led to a more uniform crystal field environment around the cubic Ce^{3+} site. We believe that the improved crystal field is thought to contribute to the improved luminous efficiencies.

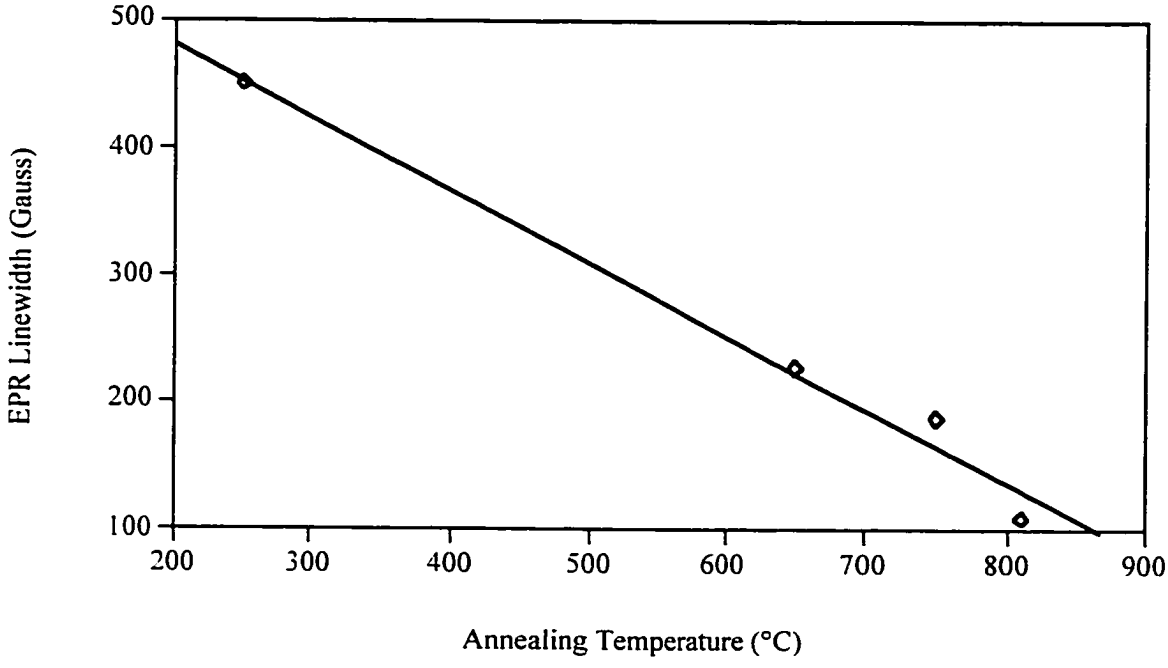


Figure 4-14. Ce^{3+} EPR line width as a function of annealing temperature [War97]

Dennis et al. used PL spectroscopy to investigate the mechanisms responsible for the improved EL properties as a function of annealing [Den96]. The investigators used time resolved laser spectroscopy to determine the fluorescence decay times of SrS:Ce films. By exciting at a specific wavelength corresponding to the Ce^{3+} transition (440 nm), the investigators were able to study the decay time of the luminescence yielding information on the presence of non radiative and radiative traps which quench the

luminescence. Shorter decay times are associated with higher probability of traps capturing the energy from the Ce^{3+} and de-exciting non-radiatively. The fluorescent transients of annealed and as-deposited SrS:Ce phosphor films are plotted in Figure 4-15. The Xe lamp line is plotted to represent the detection systems response for a zero decay time signal; note that the fluorescent transients from the SrS:Ce will not be affected by the system response time. It should be also noted that the PL intensityie plotted have been normalized i.e., the PL intensity for the annealed films were higher. The fluorescent transients showed an increase in decay time from 15 ns to 20 ns as a result of annealing at 810°C. This strongly supports the hypothesis that post deposition annealing led to a reduction in the relative concewntration of luminescent traps in SrS:Ce.

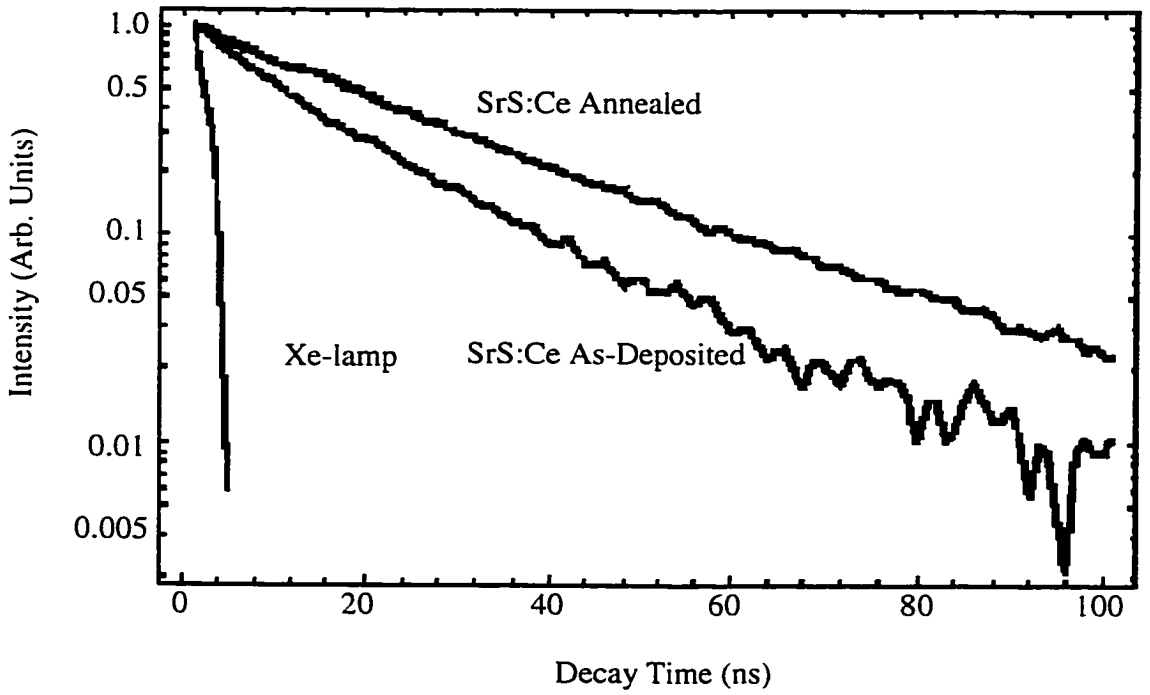


Figure 4-15. Fluorescent transients of annealed and as deposited SrS:Ce phosphor films

Summary

Post deposition annealing of as-deposited SrS:Ce phosphor thin films resulted in improved TFEL device properties, namely decreases in threshold voltage accompanied by increases in brightness (L_{40}) and luminous efficiency. Microstructural characterization revealed an improvement in crystal quality with increasing annealing temperatures. The narrowing of FWHM of the (220) x-ray diffraction peak as well as the increased grain size showed evidence that annealing led to the elimination of strain induced defects associated with non-equilibrium deposition and grain boundary area as a result of grain growth. EPR characterization indicated a significant increase in the nearly cubic Ce^{3+} concentration which supported the earlier contention that annealing led to a better Ce^{3+} crystal field. PL studies indicated that annealing led to a significant increase in the luminescent decay time suggesting that traps leading to a quenching were reduced. We conclude from this experiment, that improvement in TFEL device properties can be achieved with larger grain sizes and further elimination of crystalline defects. Since the substrate limits the annealing temperature that can be used, novel methods must be utilized to promote grain growth in the SrS:Ce film at lower temperatures.

CHAPTER 5
SrS:Ce TFEL DEVICES CONTAINING GALLIUM AND EXCESS SULFUR

Introduction

The previous chapter reported on the EL performance of SrS:Ce TFEL devices as a function of post deposition annealing temperature. It was found that annealing at 810°C for 120s resulted in significantly improved EL device performance. Annealing also resulted in the improvement in the SrS:Ce crystal quality as well as in an increase in the SrS:Ce grain size. EPR and PL characterization of Ce^{3+} activator ions suggested that the improvement in crystal quality led to an increase in the nearly cubic Ce^{3+} density which resulted in increased luminous efficiencies.

Significant improvement in EL properties was observed when small amounts of thiogallate were added to the SrS:Ce system. The addition of thiogallate essentially equated to the addition of gallium and excess sulfur to the SrS:Ce phosphor layer. Presented in this chapter are the results of these experiments performed on the SrS:Ce TFEL devices containing excess gallium and sulfur. The electrical and optical properties are reported for each of the three different devices, followed by the results of the microstructural characterization performed on the phosphor layers. A discussion of the data concludes this chapter.

Results

Excess gallium and sulfur were introduced into the SrS:Ce phosphor layer via three different methods: 1) a thiogallate capping layer (double layer device) , 2) alternating layers of thiogallate and SrS:Ce (multi-layer device) and 3) incorporation of Ga_2S_3(7 wt.%) in the SrS:Ce sputter target (Ga_2S_3 doped target device). The electrical, optical and microstructural characterization results for each device is presented below.

Double Layer Devices

The double layer devices studied consisted of the basic TFEL device architecture discussed earlier but with a phosphor layer consisting of a 1 μm thick layer of SrS:Ce with a 400 Å capping layer of thiogallate. A schematic of the device architecture is shown in Figure 5-1.

DOUBLE LAYER DEVICES

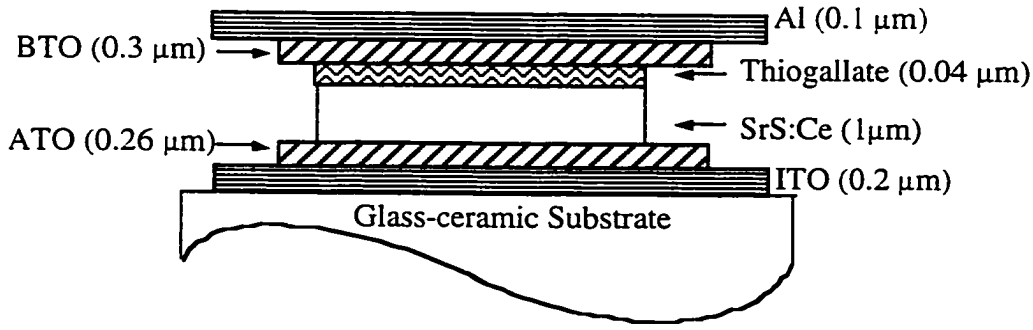


Figure 5-1. Architecture of a double layer TFEL device

Electrical and Optical Characterization

In order for effective comparison, the double layer devices were subjected to the same post deposition annealing temperatures and times as the single layer devices. This section reports the effect of the post deposition annealing temperature on the threshold voltage, L_{40} and emission spectra.

Threshold voltage

The threshold voltage as a function of annealing temperature is plotted in Figure 5-2. Annealing at higher temperatures resulted in a reduction in the threshold voltage. The 810°C anneal led to the lowest threshold voltage of 183 volts.

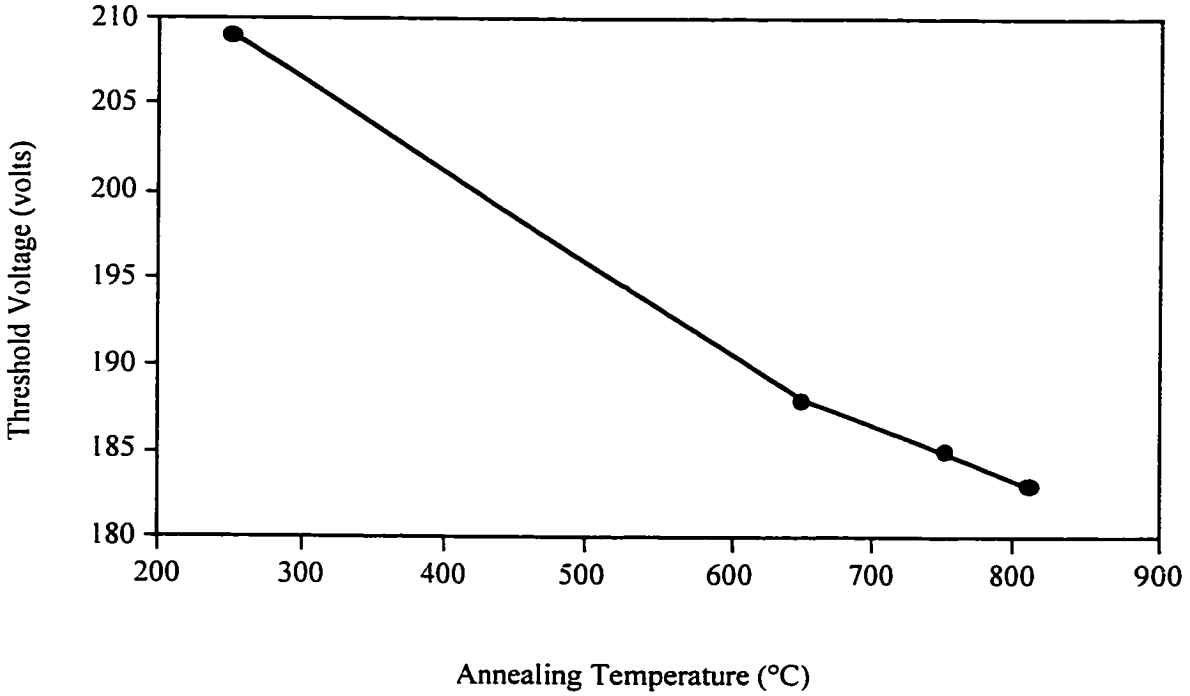


Figure 5-2. Relationship between the threshold voltage and the post deposition annealing temperature for double layer TFEL devices

Brightness

The effect of post deposition annealing on the brightness, as characterized by the L_{40} value, is shown in Figure 5-3. As in the case of the single layer devices, post deposition annealing significantly improved the brightness. Annealing at 810 °C resulted in greater than a seven fold increase in the brightness compared with the as-deposited condition with a maximum measured L_{40} of 58.7 cd/m^2.

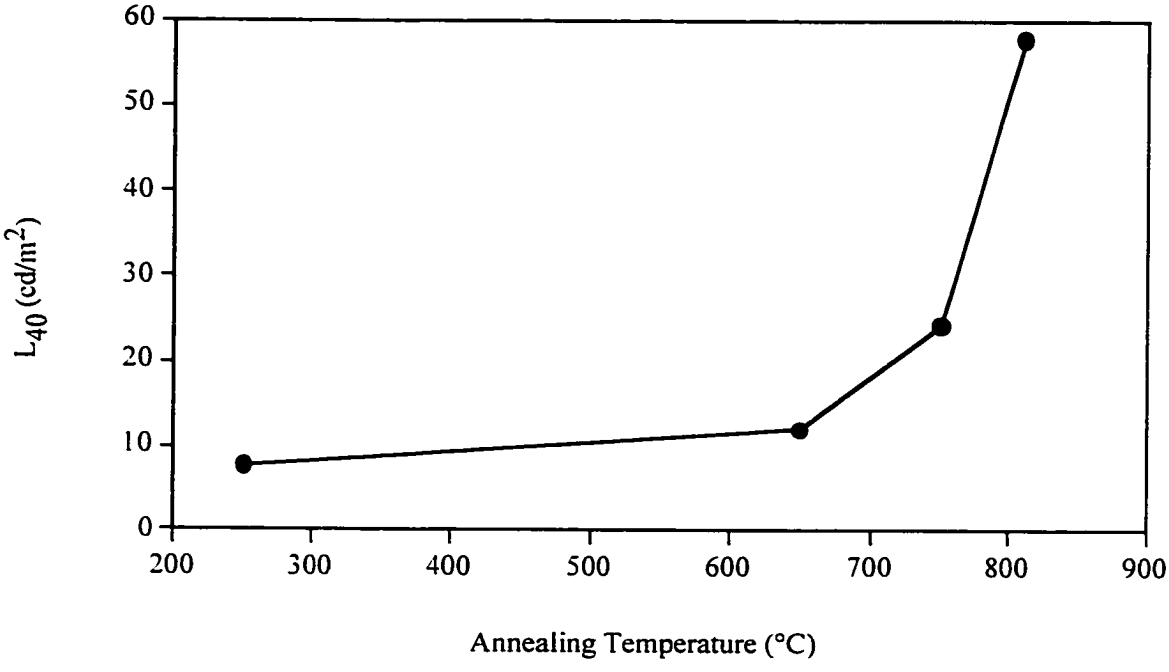


Figure 5-3. Relationship between L_{40} and the post deposition annealing temperature for double layer TFEL devices

Luminous efficiency

As seen in Figure 5-4, post deposition annealing resulted in a significant improvement in the luminous efficiency of the double layer TFEL device. The highest luminous efficiency of 0.24 l/w was found in the phosphor film of the 810°C annealed double layer TFEL device.

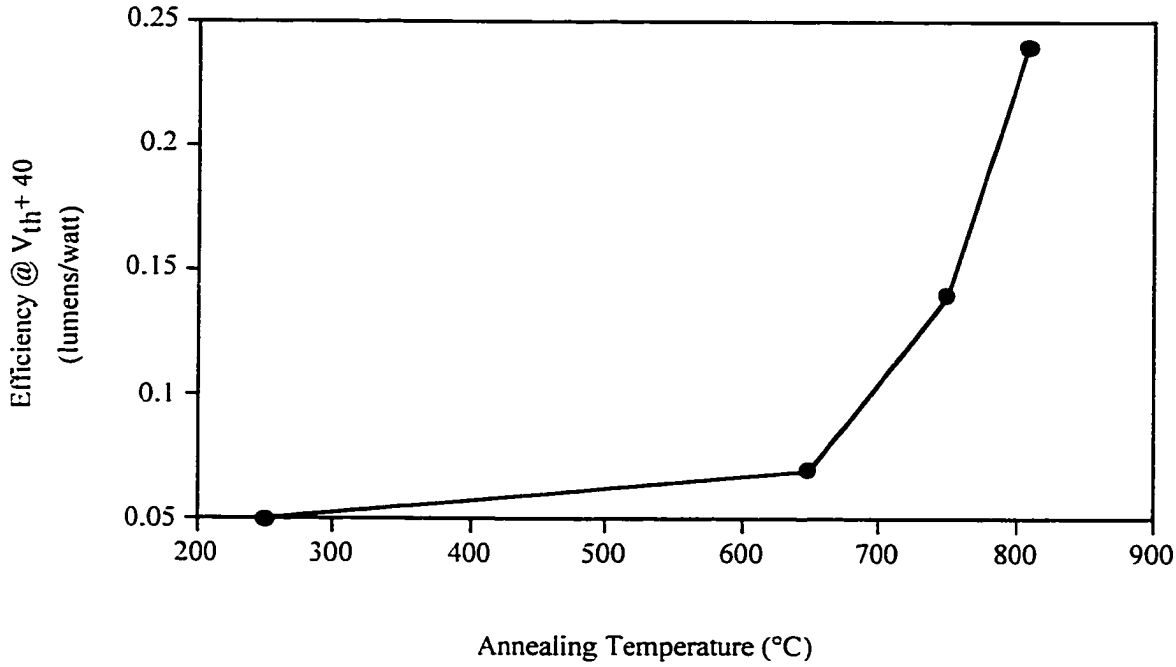


Figure 5-4. Relationship between efficiency (at the threshold voltage + 40 volts) and the post deposition annealing temperature for double layer TFEL devices

Emission spectra

The CIE coordinates of the peak emission wavelengths measured for the double layer TFEL devices are listed in Table 5-1 and are plotted on a CIE diagram in Figure 5-5. No discernible trend in a shift towards green or blue emission was observed as a result of increased annealing temperature.

Table 5-1. CIE coordinates measured for the annealed double layer TFEL devices.

Annealing Treatment	CIE Coordinates (x,y)
As-Deposited	(.23,.39)
650°C/120s	(.21,.37)
750°C/120s	(.23,.40)
810°C/120s	(.24,.36)

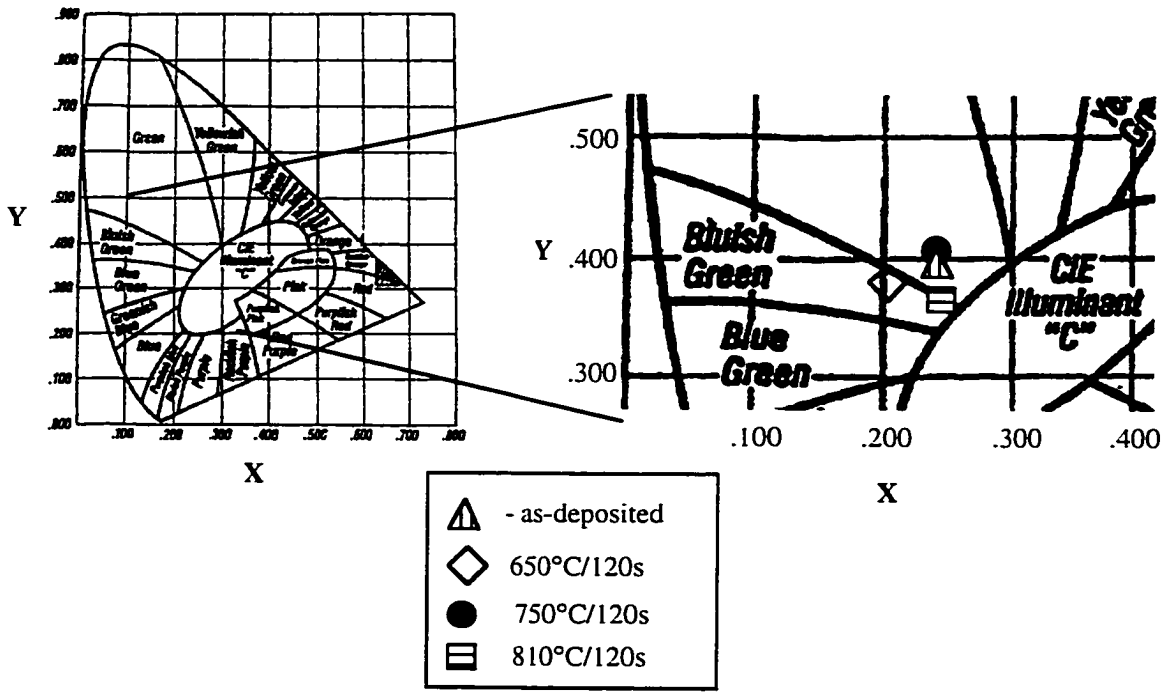


Figure 5-5. CIE diagram with the CIE coordinates for the annealed double layer TFEL devices

Microstructural Characterization

The previous sections have shown that post deposition annealing led to a significant improvement in the EL properties of double layer TFEL devices. As reported in chapter 4, the improved EL device performance of single layer TFEL devices as a function of annealing temperature was attributed to the improvement in the phosphor layer crystal quality as a result of post deposition annealing. In order to better understand the reasons for the improved EL performance of double layer TFEL devices, the microstructure of the phosphor layer was characterized using XRD, SIMS and TEM. The results from these analyses are presented below.

X-Ray diffraction

The results from the XRD analysis performed on the double layer devices are listed in Table 5-2, 5-3, 5-4 and 5-5. The double layer phosphor films, regardless of the annealing treatment, were textured with a preferred (200) crystallographic orientation. The FWHM of the (200) peak decreased with increasing post deposition annealing temperature as seen in Figure 5-6.

Table 5-2. XRD summary table for the as-deposited double layer TFEL device.

Angle	D-Spacing	Intensity	Peak
29.5325	3.0223	100.00	SrS (200)
25.3750	3.5072	10.59	SrS (111)
30.3775	2.9401	8.91	ITO
61.4650	1.5073	5.99	SrS (400)

Table 5-3. XRD summary table for a double layer TFEL device annealed at 650°C/120s.

Angle	D-Spacing	Intensity	Peak
29.6500	3.0105	100.00	SrS (200)
61.5475	1.5055	6.66	SrS (400)
36.2000	2.4794	5.54	ITO
25.5725	3.4806	3.91	SrS (111)

Table 5-4. XRD summary table for a double layer TFEL device annealed at 750°C/120s.

Angle	D-Spacing	Intensity	Peak
29.6475	3.0108	100.00	SrS (200)
61.6325	1.5037	6.84	SrS (400)
36.1525	2.4826	5.53	ITO
25.5525	3.4832	2.85	SrS (111)

Table 5-5. XRD summary table for a double layer TFEL device annealed at 810°C/120s.

Angle	D-Spacing	Intensity	Peak
29.6775	3.0078	100.00	SrS (200)
61.6275	1.5038	8.00	SrS (400)
36.1525	2.4826	5.53	ITO
50.2575	1.8139	2.54	SrS (311)

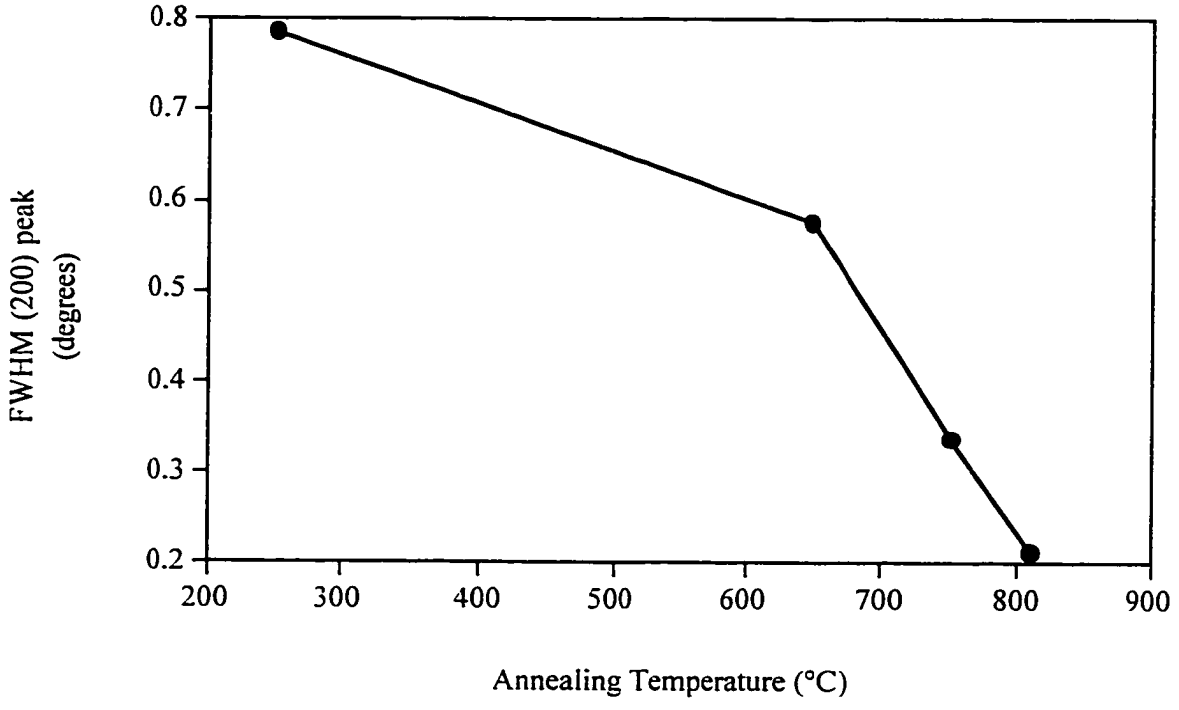


Figure 5-6. FWHM of the SrS (200) peak as a function of post deposition annealing temperature in double layer TFEL devices

SIMS

SIMS analysis was performed on the phosphor layer of the as-deposited and 810°C annealed double layer TFEL devices. The presence of the thiogallate capping layer is confirmed by the presence of the gallium peak in the SIMS profile of the as-deposited phosphor layer shown in Figure 5-7a. The thickness of the phosphor layer was

determined in part by the emergence of the aluminum signal due to the presence of the ATO dielectric layer. The SIMS profile of the 810°C annealed phosphor layer indicated a change in the gallium and cerium signal as a result of annealing (Figure 5-7b). Both profiles indicated that the level of strontium remained constant throughout the phosphor layer. The SIMS analysis indicated that annealing at 810°C resulted in the migration of both gallium and cerium from the capping layer into the SrS:Ce layer.

TEM

Cross section TEM micrographs of the as-deposited phosphor double layer are presented in Figure 5-8. The Al, BTO, thiogallate and SrS:Ce layers can be seen in Figure 5-8a. As seen in Figure 5-8c, the capping layer conforms to the surface of the SrS:Ce film. Measurements taken from cross section TEM micrographs show the thiogallate film to be 600 ± 100 Å in thickness. The mean grain diameter of the as-deposited SrS:Ce columnar grains was measured to be 400 ± 175 Å.

The effect of annealing at 810°C is evident in the cross sectional TEM micrograph in Figure 5-9. Annealing had resulted in a change in the grain morphology in the top 5000 ± 600 Å of the film. In this transformed region, the grain morphology changed from columnar to equiaxed. The mean equiaxed grain size was measured to be 2000 ± 400 Å. Within the tranformed region, spherical voids were observed. The mean void size was 600 ± 200 Å. The columnar SrS:Ce grains had coarsened considerably due to annealing with a mean grain diameter of 1300 ± 300 Å.

Grain size measurements were made from the cross-sectional TEM micrographs in both the equiaxed and the columnar region. The grain size of the columnar SrS:Ce grains along with the equiaxed grain size increased with increased post deposition annealing temperature as seen in Figure 5-10. The standard deviation was used for the error bars plotted in Figure 5-10.

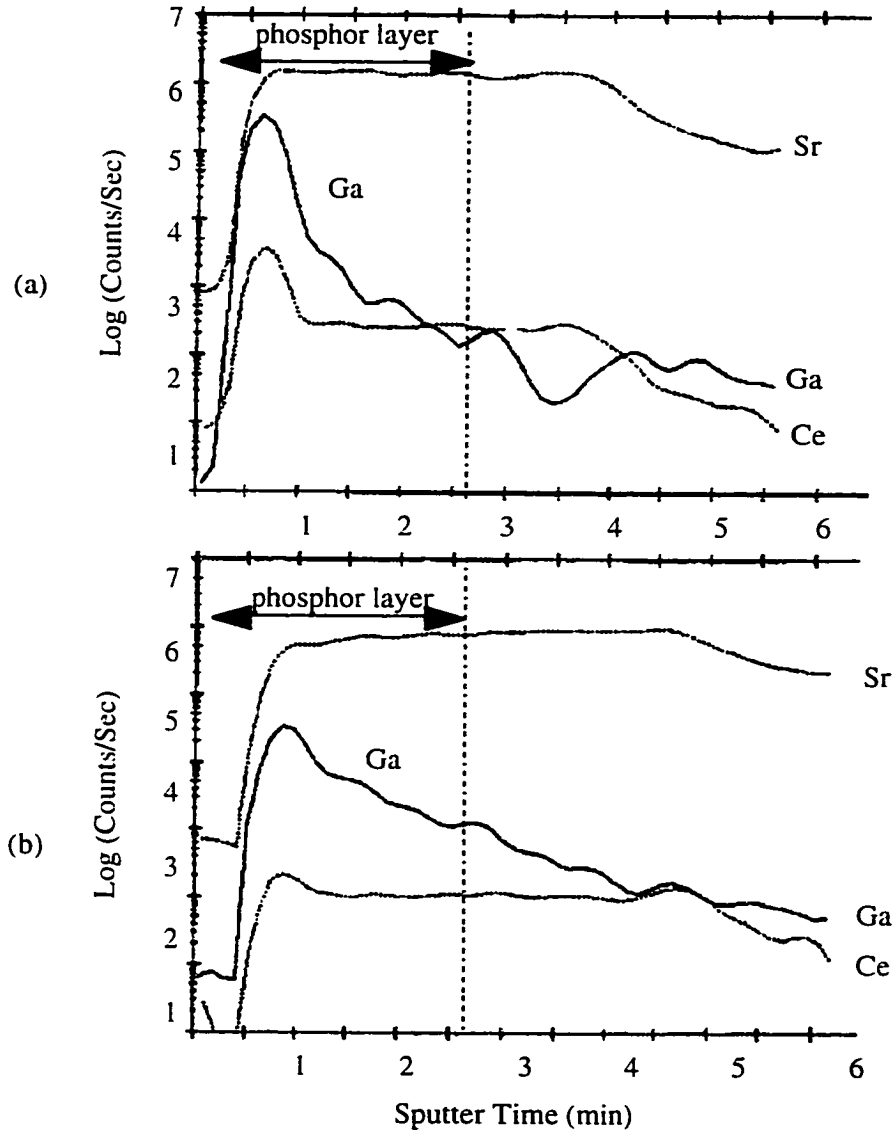


Figure 5-7. SIMS profiles of the phosphor layer in an (a) as-deposited and (b) 810°C annealed double layer TFEL device

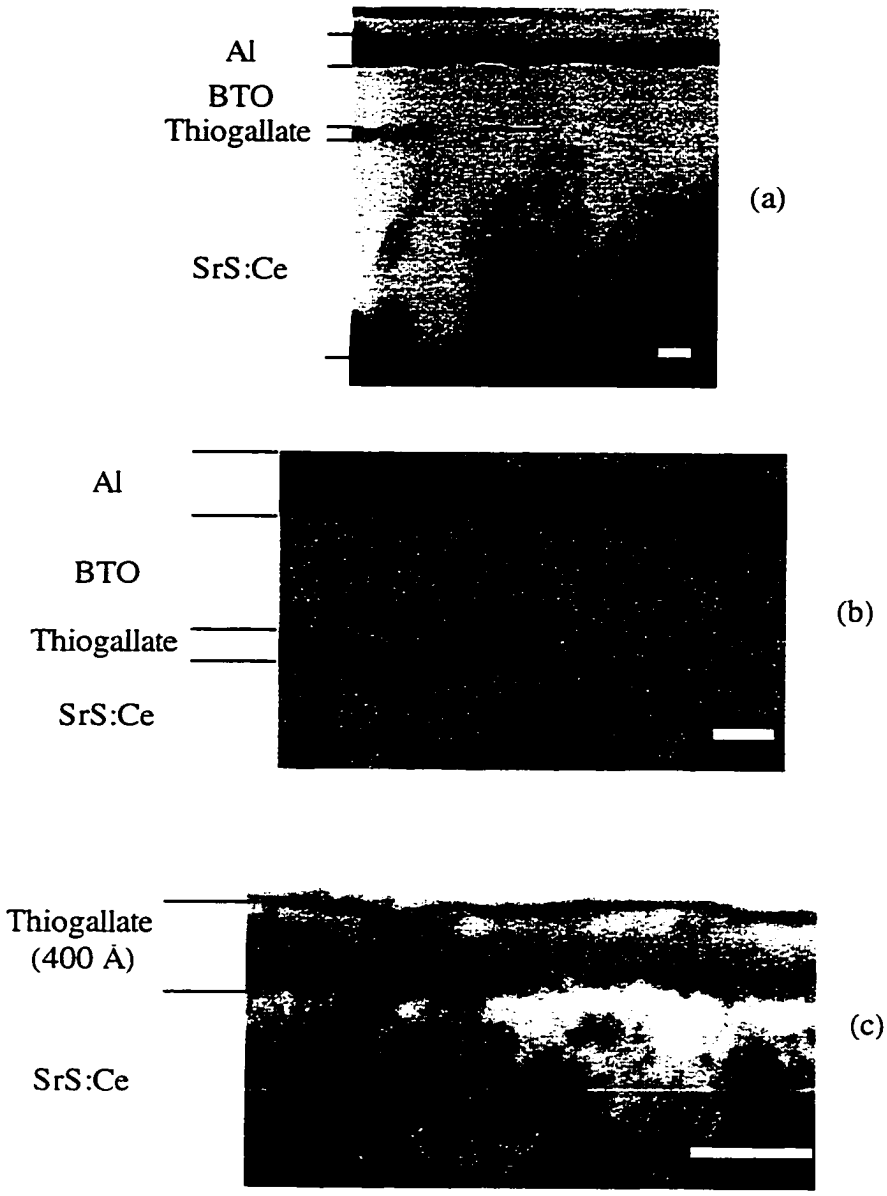


Figure 5-8. Cross sectional TEM micrographs of the phosphor layer in an as-deposited double layer TFEL device (the inserted white bar represents 1000Å in all three micrographs)

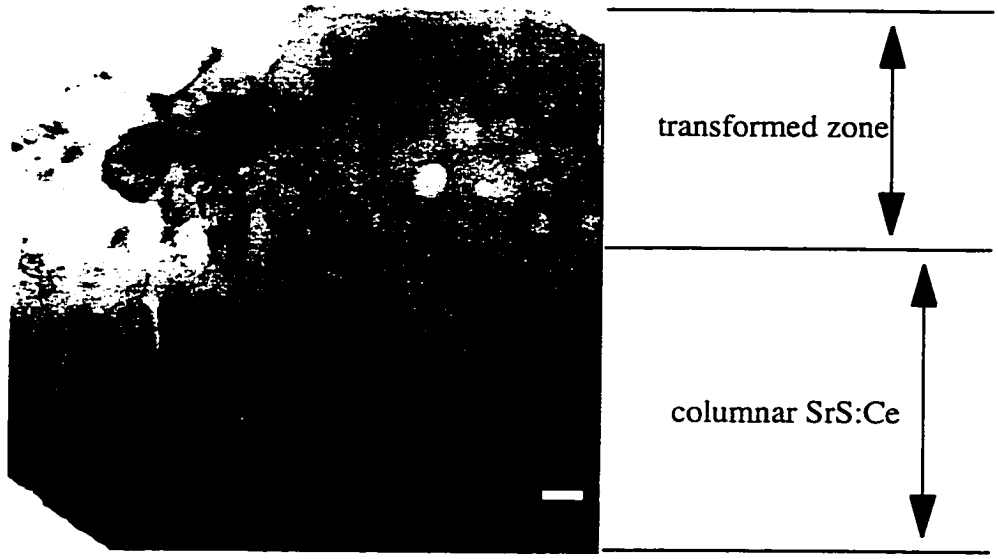


Figure 5-9. Cross sectional TEM micrograph of the phosphor layer annealed at 810°C/120s in a double layer TFEL device (the inserted white bar represents 1000Å)

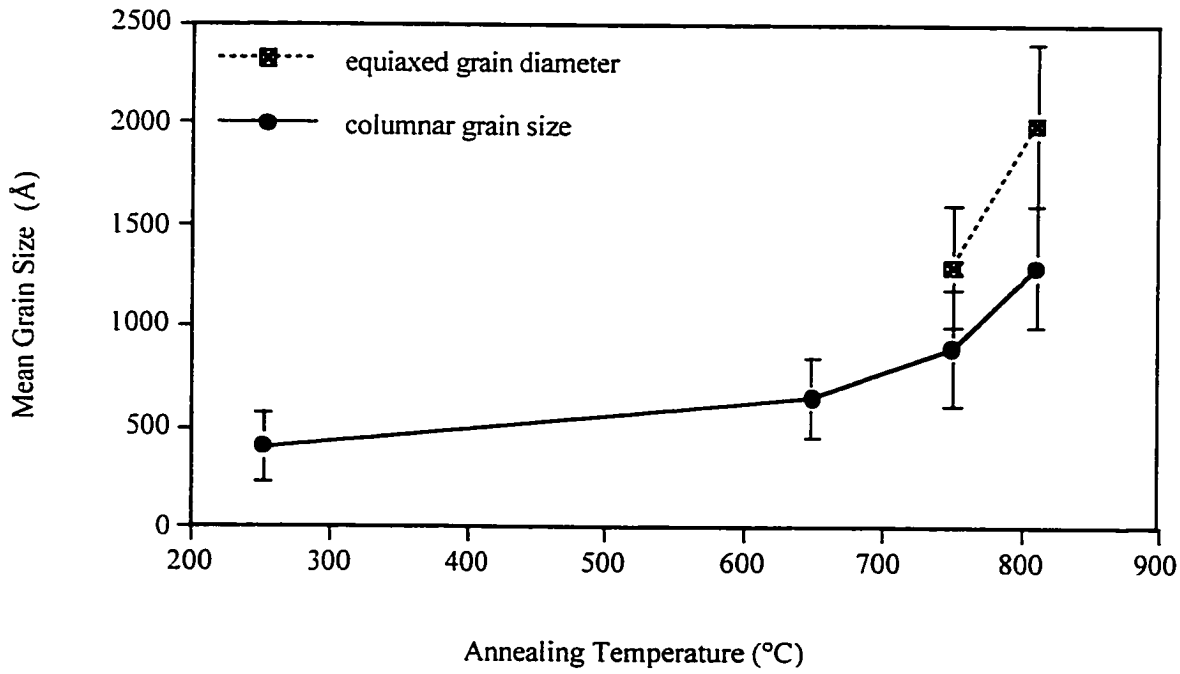


Figure 5-10. SrS:Ce grain size (in the columnar and transformed region) as a function of post deposition annealing temperature for double layer TFEL devices

Multi-Layer Devices

The enhanced EL performance of the double layer TFEL devices led to investigating the effect of adding more thiogallate to SrS:Ce phosphor layer. This was accomplished by the growing alternating layers of 1700 Å thick films of SrS:Ce and 300 Å thick films of thiogallate, e.g., multi-layer phosphor. A schematic of the device architecture is shown in Figure 5-11.

MULTI-LAYER DEVICES

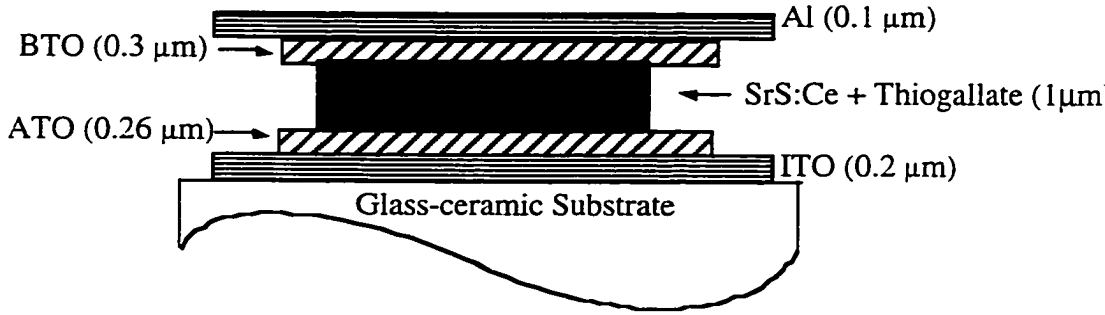


Figure 5-11. Architecture of a multi-layer device

Electrical and Optical Characterization

In order for effective comparison, the multi-layer devices were subjected to the same annealing temperatures and times used in the previous studies. This section reports the effect of the annealing temperature on the threshold voltage, L_{40} and emission spectra.

Threshold voltage

The threshold voltage as a function of post deposition annealing temperature is plotted in Figure 5-12. Annealing at higher temperatures resulted in a reduction in the threshold voltage. The 810°C anneal led to the lowest threshold voltage of 154 volts.

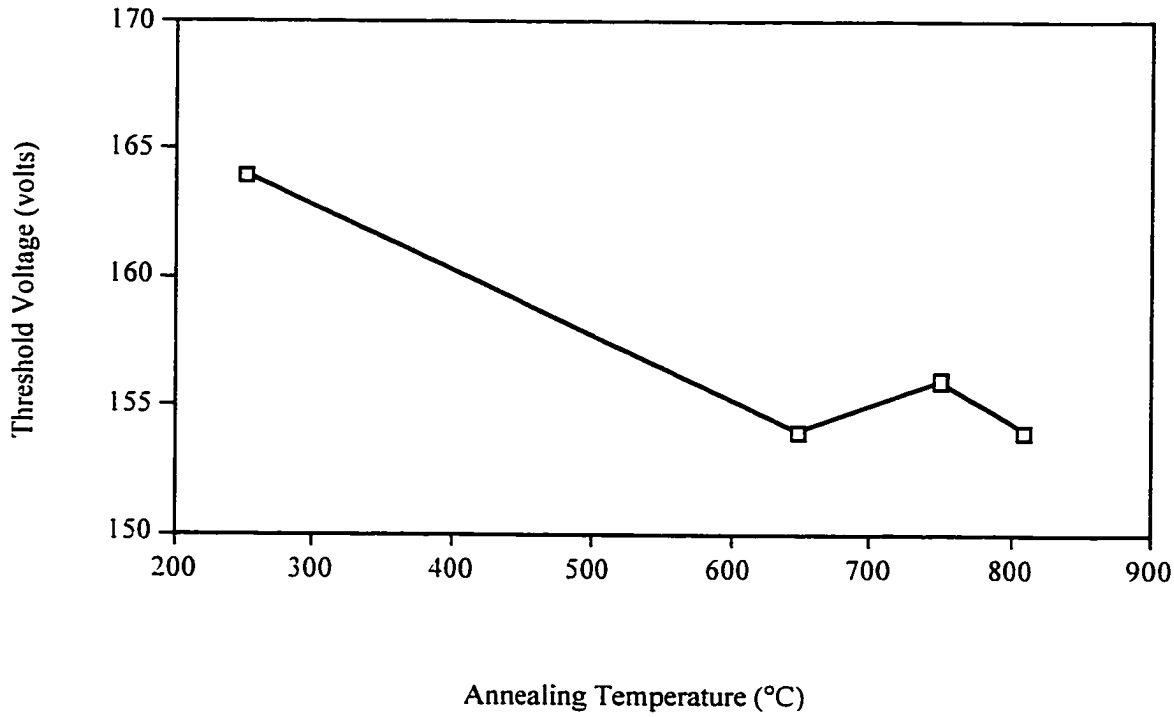


Figure 5-12. Relationship between the threshold voltage and the post deposition annealing temperature for multi-layer TFEL devices

Brightness

The effect of post deposition annealing on the brightness, as characterized by the L_{40} value, is shown in Figure 5-13. As in the other devices studied, post deposition annealing resulted in a significant increase in the brightness of the multi-layer TFEL devices. The largest increase in brightness occurred between the 750°C and the 810°C

anneal. Annealing at 810 °C resulted in the maximum measured L_{40} of 90 cd/m^2. This represented a twenty fold increase in the brightness compared to that of the as-deposited device.

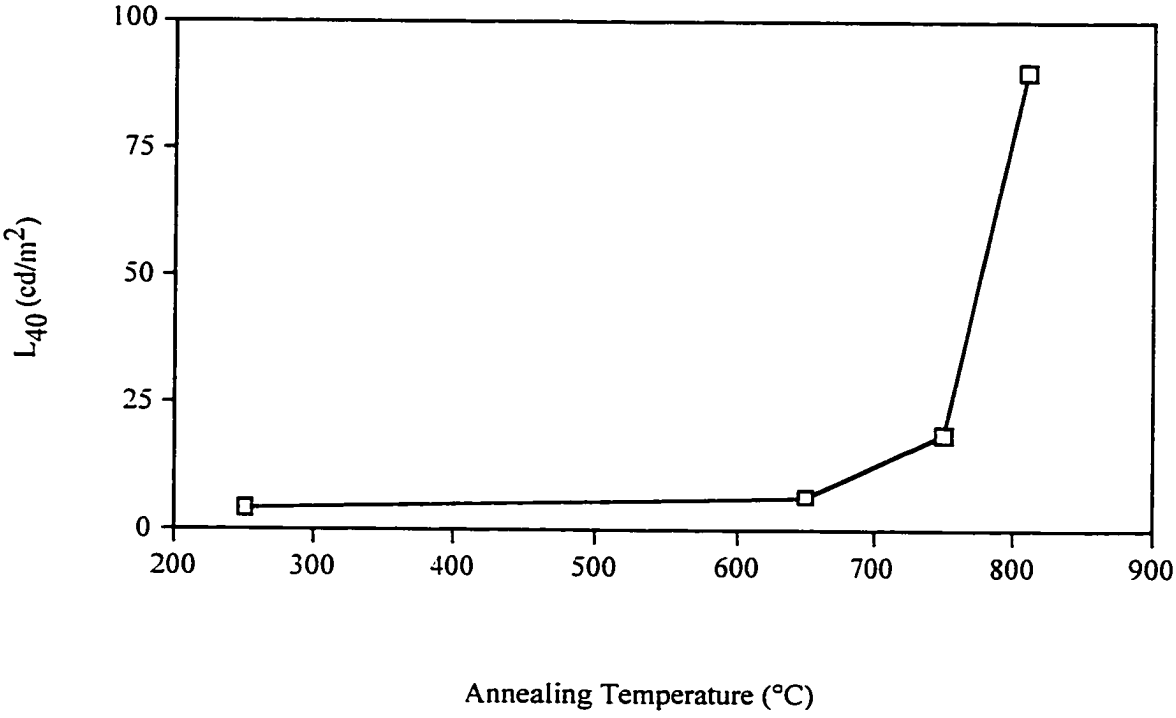


Figure 5-13. Relationship between L_{40} and the post deposition annealing temperature for multi-layer TFEL devices

Luminous efficiency

As seen in Figure 5-14, post deposition annealing resulted in a significant improvement in the luminous efficiency of the multi-layer TFEL devices. The luminous efficiency of the phosphor layer in the 810°C annealed multi-layer TFEL device was 0.57 l/w. This value was almost double that for the similarly annealed double layer device.

Once again, the largest increase in the luminous efficiency occurred between the 750°C and 810°C anneal.

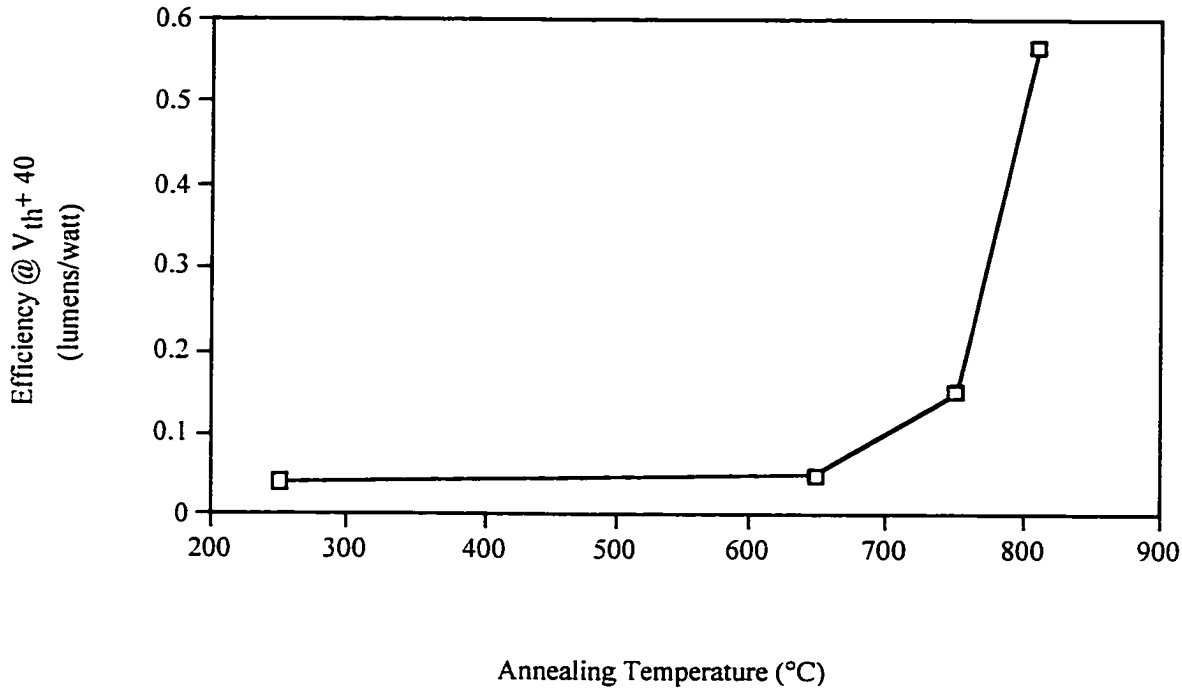


Figure 5-14. Relationship between efficiency (at the threshold voltage + 40 volts) and the post deposition annealing temperature for multi-layer TFEL devices

Emission spectra

The CIE coordinates of the peak emission wavelengths measured for the multi-layer TFEL devices are listed in Table 5-6 and are plotted on a CIE diagram in Figure 5-15. Annealing has led to a more green emission as proven by the increasing CIE y coordinates.

Table 5-6. CIE coordinates measured for the annealed multi-layer TFEL devices.

Annealing Treatment	CIE Coordinates (x,y)
As-Deposited	(.24,.39)
650°C/120s	(.22,.39)
750°C/120s	(.24,.42)
810°C/120s	(.26,.48)

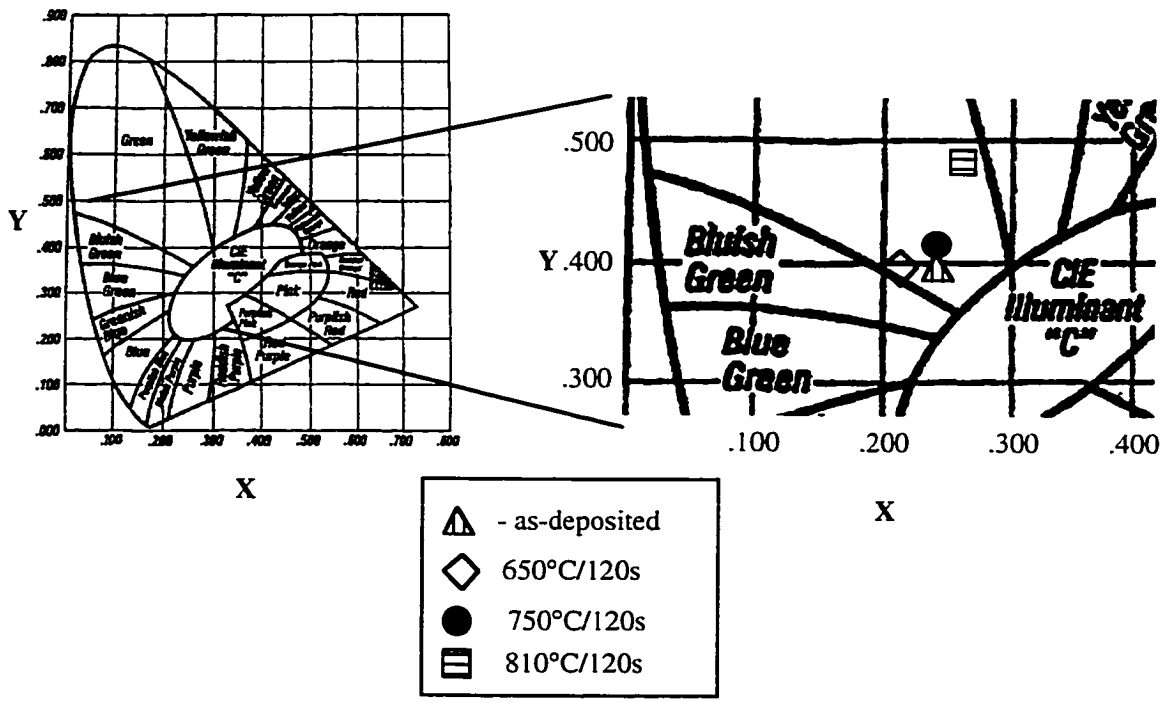


Figure 5-15. CIE diagram with the CIE coordinates for the annealed multi-layer devices

Microstructural Characterization

The previous sections reported that post deposition annealing led to a significant improvement in the EL properties of multi-layer TFEL devices. In the double layer devices, addition of thiogallate resulted in a significant change in the annealed microstructure as compared with the phosphor layer in single layer devices. In order to better understand the effect of the multiple layers of thiogallate on the microstructure of the phosphor film, XRD, SIMS and TEM analysis were performed. The results from these analyses are presented below.

X-Ray diffraction

The results from the XRD analyses performed on the multi-layer devices are listed in Table 5-7, 5-8, 5-9 and 5-10. The multi-layer phosphor films, regardless of the annealing condition, were textured with a preferred (220) crystallographic orientation. The FWHM of the (220) peak decreased with increasing annealing temperature as shown in Figure 5-16.

Table 5-7. XRD summary table for the as-deposited multi-layer TFEL device.

Angle	D-Spacing	Intensity	Peak
42.1600	2.1417	100.00	SrS (220)
30.3025	2.9472	23.84	ITO
35.3125	2.5397	17.64	ITO
29.4850	3.0270	15.06	SrS(200)

Table 5-8. XRD summary table for a multi-layer TFEL device annealed at 650°C/120s.

Angle	D-Spacing	Intensity	Peak
42.4050	2.1299	100	SrS (220)
29.7275	3.0029	19.20	SrS (200)
30.3125	2.9462	17.24	ITO
35.3275	2.5386	13.77	ITO

Table 5-9. XRD summary table for a multi-layer TFEL device annealed at 750°C/120s.

Angle	D-Spacing	Intensity	Peak
42.4872	2.1262	100.00	SrS (220)
29.7450	3.0013	26.50	SrS (200)
36.1525	2.4826	15.53	ITO
30.3360	2.9437	12.46	ITO

Table 5-10. XRD summary table for a multi-layer TFEL device annealed at 810°C/120s.

Angle	D-Spacing	Intensity	Peak
42.5750	2.1218	100.00	SrS (220)
29.7525	3.0004	36.24	SrS (200)
35.2425	2.5446	10.72	ITO
30.3500	2.9427	9.46	ITO

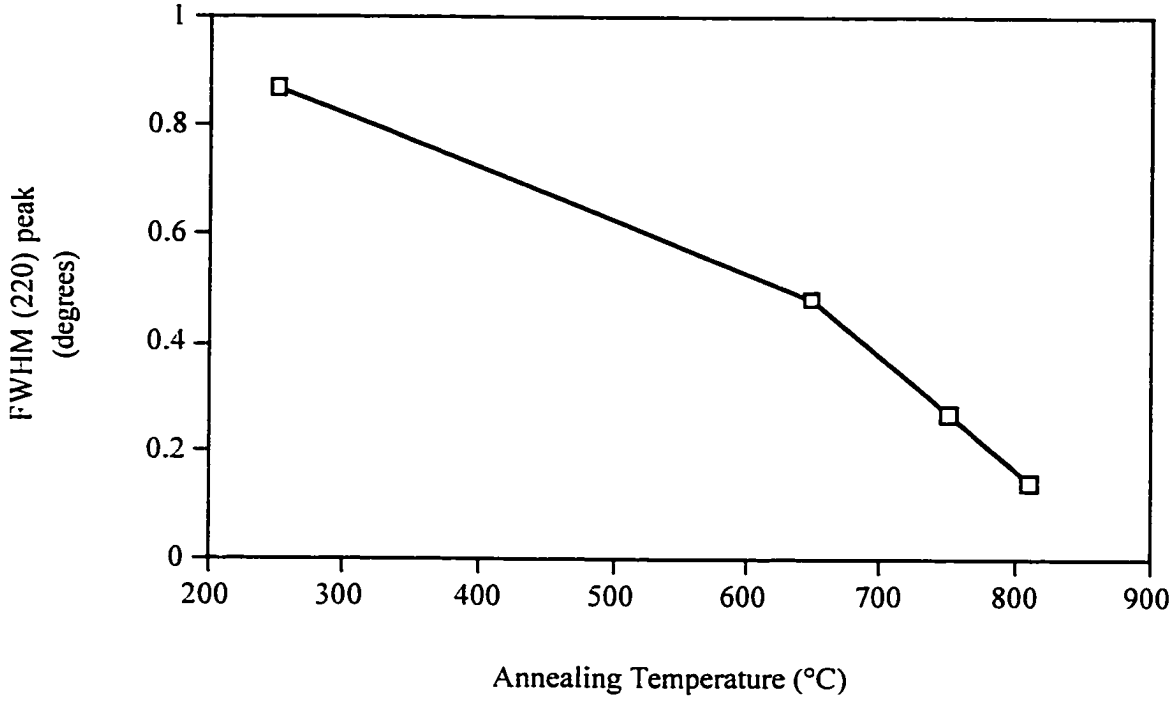


Figure 5-16. FWHM of the SrS (220) peak as a function of post deposition annealing temperature for multi-layer TFEL devices

SIMS

SIMS analysis was performed on the as-deposited and 810°C annealed phosphor layers of the multi-layer TFEL devices. The SIMS profiles, given in Figure 5-17, show a significant change in the gallium signal as a result of annealing. Post deposition annealing resulted in the apparent migration of gallium to the top interface of the film. The cerium signal also changed as a result of post deposition annealing with a similar migration to the top interface. Both profiles indicated that the level of strontium throughout the phosphor layer was unaffected by annealing

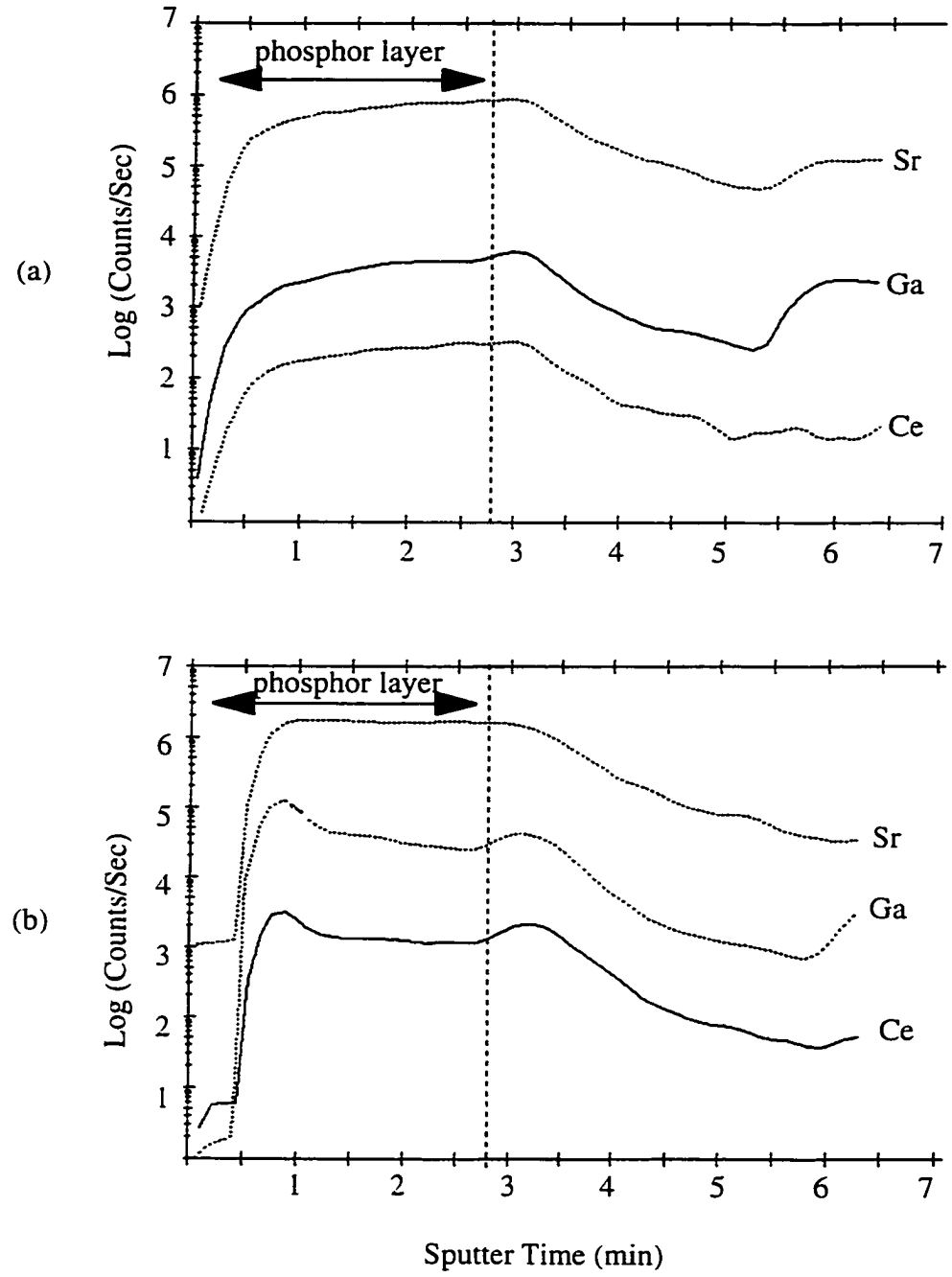
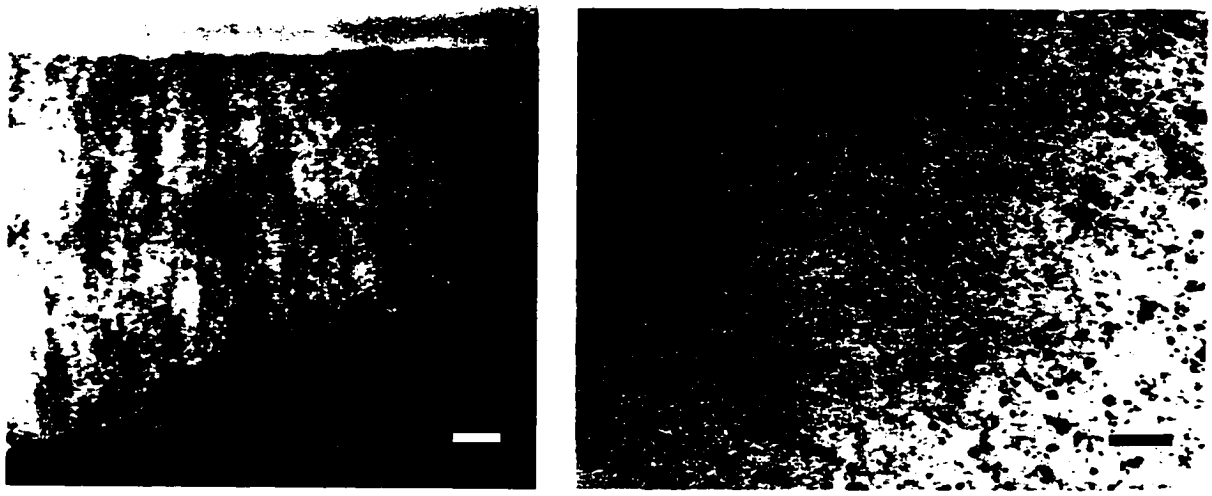


Figure 5-17. SIMS profiles of the phosphor layer in an (a) as-deposited and (b) 810°C annealed multi-layer TFEL device

TEM

TEM micrographs of the phosphor layer in an as-deposited multi-layer TFEL device are presented in Figure 5-18. The as-deposited structure clearly shows the columnar grain morphology common to all of the as-deposited microstructures. The alternating layers of thiogallate are not discernible in cross sectional TEM micrographs. The average grain diameter of the phosphor layer was measured to be 300 ±100 Å.

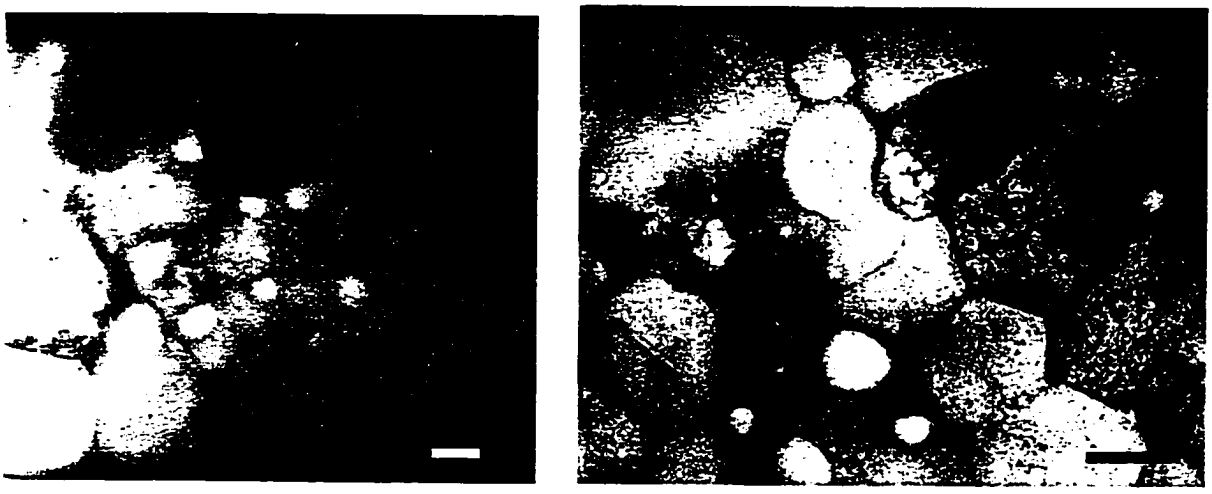


(a) (b)

Figure 5-18. TEM micrographs of an as-deposited phosphor layer in a multi-layer TFEL device (a) cross section and (b) plan view (the inserted bar represents 1000Å in both micrographs)

The effect of annealing at 810°C can be seen from the cross sectional and plan view TEM micrographs of the phosphor layer shown in Figure 5-19. Unlike the double layer film, co-deposition of the thiogallate led to a homogenous equiaxed grain morphology. Unique to the 810°C annealing treatment were the presence of spherical voids, seen in the micrographs as white circular regions, distributed throughout the phosphor layer. The average void grain size was measured to be 600 ± 200 Å. The

average grain size was 5000 ± 500 Å. The phosphor layer grain and void sizes were measured from plan view TEM micrographs. The grain size increased with increasing annealing temperature as seen in Figure 5-20.



(a) (b)

Figure 5-19. TEM micrographs of the phosphor layer in a multi-layer TFEL device annealed at 810°C for 120s (a) cross section and (b) plan view (the inserted bar represents 1000Å in both micrographs)

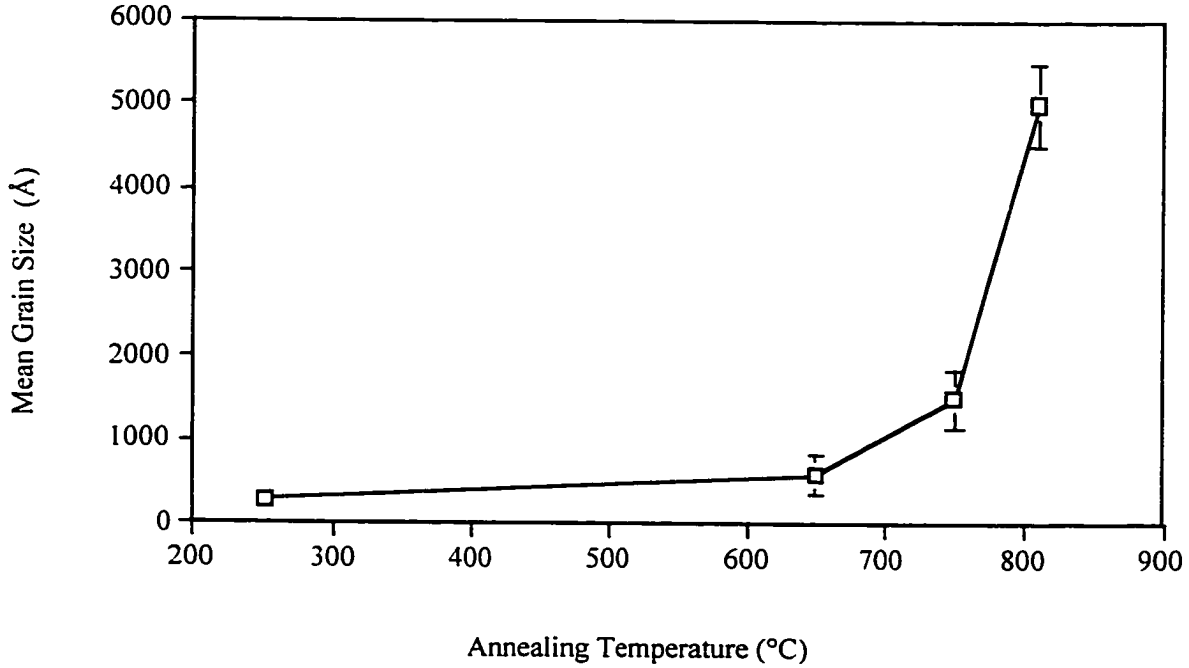


Figure 5-20. SrS:Ce grain size as a function of post deposition annealing temperature for multi-layer TFEL devices

Ga_2S_3 Doped SrS:Ce Target Devices

The results of the multi-layer experiments led to the incorporation of Ga_2S_3 into the SrS:Ce sputter target. Direct addition of the Ga_2S_3 was thought to be a more cost effective and efficient method of incorporating gallium and excess sulfur into the phosphor film. Included below are the results of the characterization experiments performed on the Ga_2S_3 doped SrS:Ce devices. The Ga_2S_3 doped SrS:Ce devices studied consisted of a 1 μm thick layer of the phosphor material (SrS:Ce + 7 wt.% Ga_2S_3). A schematic of the device architecture is shown in Figure 5-21.

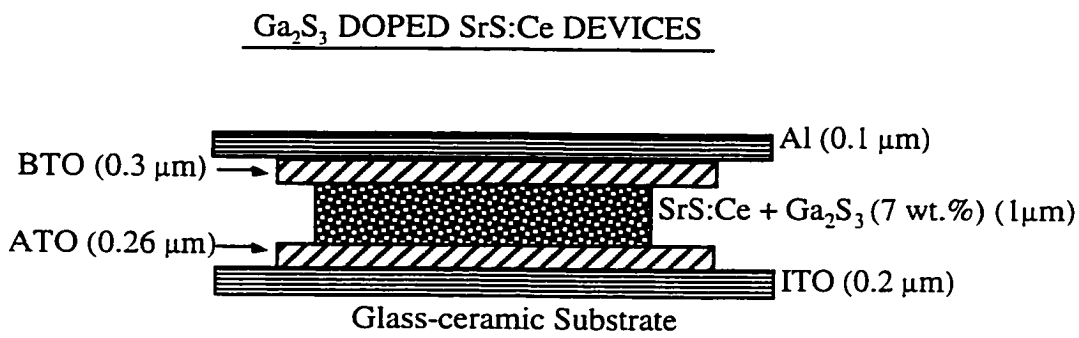


Figure 5-21. Architecture of a Ga_2S_3 doped SrS:Ce TFEL device

Electrical and Optical Characterization

In order for effective comparison, the Ga_2S_3 doped SrS:Ce devices were subjected to the same annealing temperatures and times used in the previous experiments. This section reports the effect of the post deposition annealing temperature on the threshold voltage, L_{40} and emission spectra.

Threshold voltage

The threshold voltage as a function of post deposition annealing temperature for Ga_2S_3 doped SrS:Ce devices is plotted in Figure 5-22. Annealing at higher temperatures resulted in a reduction in the threshold voltage. The 810°C anneal led to the lowest threshold voltage of 134 volts.

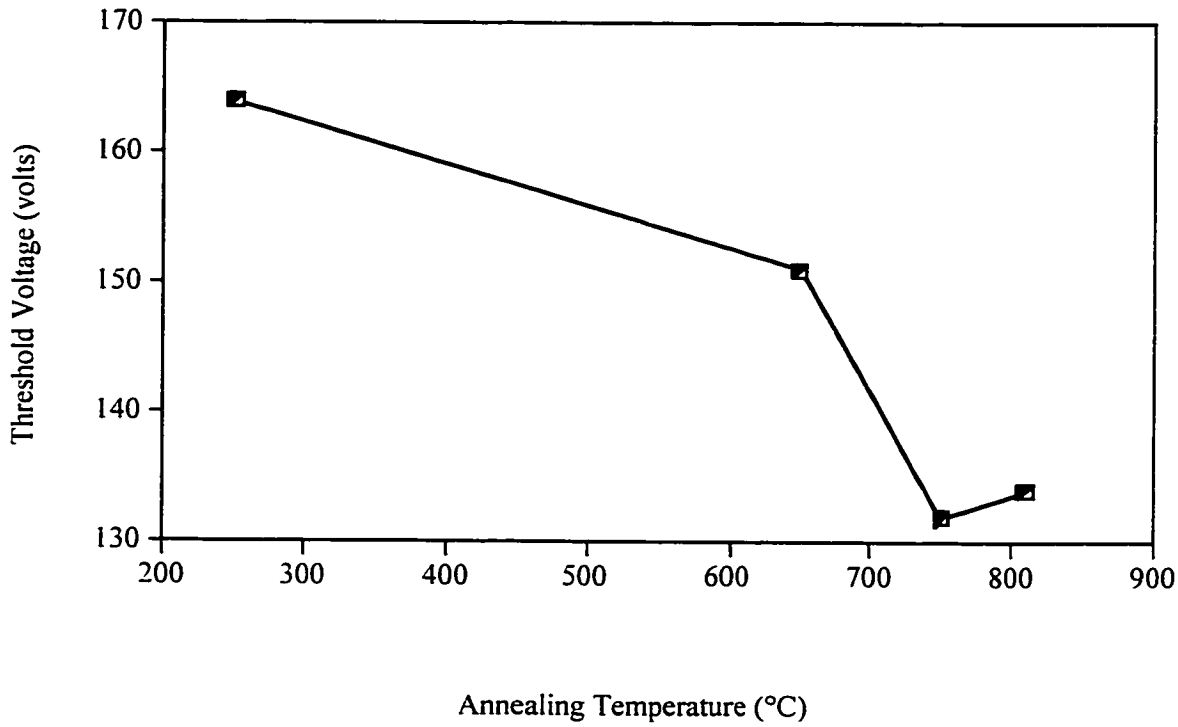


Figure 5-22. Relationship between the threshold voltage and the post deposition annealing temperature for Ga_2S_3 doped SrS:Ce TFEL devices

Brightness

The effect of post deposition annealing on the brightness, as characterized by the L_{40} value, is shown in Figure 5-23. As in the other devices , post deposition annealing significantly increased the device brightness. The largest increase in brightness occurred

between the 750°C and the 810°C anneal. Annealing at 810 °C resulted in a twenty fold increase in the brightness compared to the as-deposited condition with a maximum measured L_{40} of 110 cd/m^2.

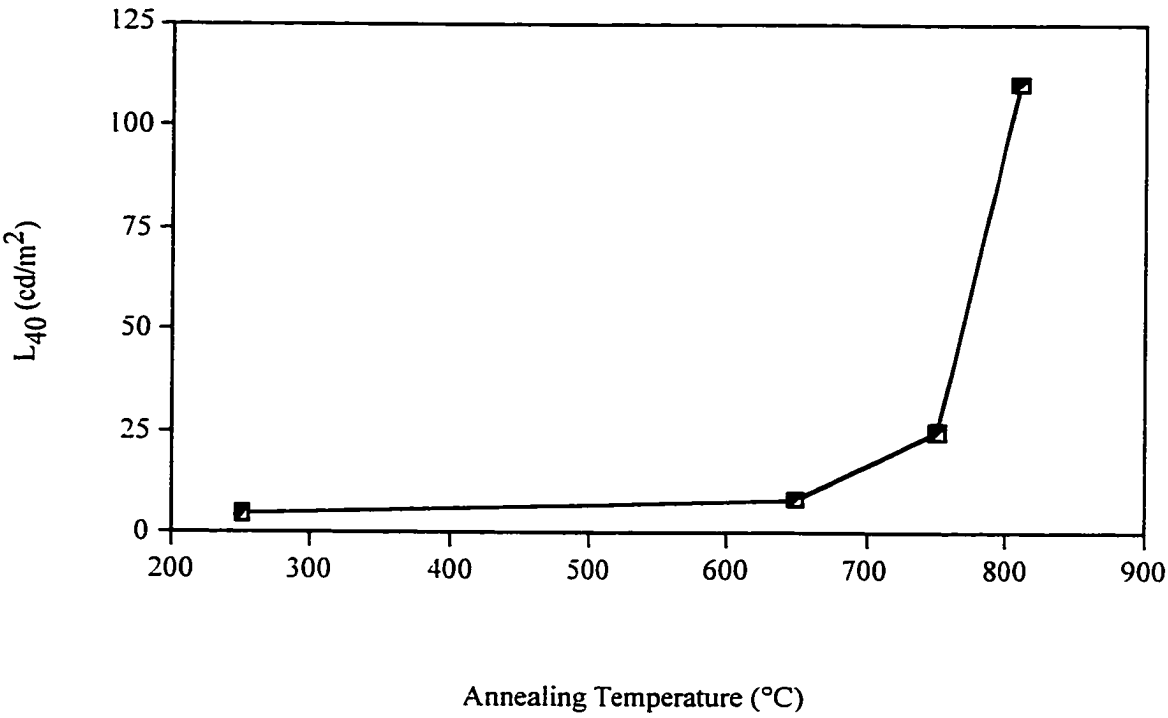


Figure 5-23. Relationship between L_{40} and the post deposition annealing temperature for Ga_2S_3 doped SrS:Ce TFEL devices

Luminous efficiency

As seen in Figure 5-24, post deposition annealing resulted in a significant improvement in the luminous efficiency of the Ga_2S_3 doped SrS:Ce TFEL devices. The largest increase in luminous efficiency occurred between the 750°C and the 810°C anneal. The luminous efficiency of the phosphor layer in the 810°C annealed Ga_2S_3 doped SrS:Ce TFEL device was 0.72 l/w.

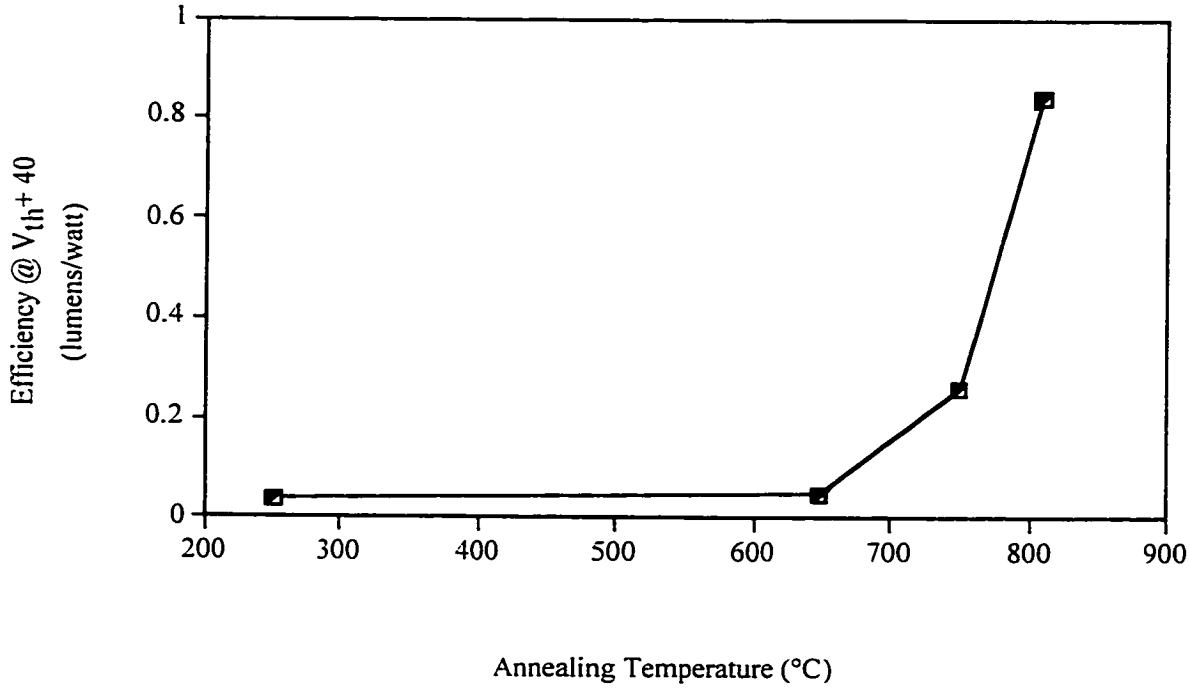


Figure 5-24. Relationship between efficiency (at the threshold voltage + 40 volts) and the post deposition annealing temperature for Ga_2S_3 doped SrS:Ce TFEL devices

Emission spectra

The emission spectra as a function of annealing temperature is plotted in Figure 5-25. The peak emission of the as-deposited Ga_2S_3 doped SrS:Ce TFEL device was 480 nm while the peak emission of the Ga_2S_3 doped SrS:Ce TFEL device annealed at 810 °C was 500 nm. The corresponding CIE coordinates for the Ga_2S_3 doped SrS:Ce TFEL devices are listed in Table 5-11 and are plotted on the CIE diagram in Figure 5-26. Consistent with the emission spectra, the CIE coordinates shifted to a more green emission with increased annealing temperature.

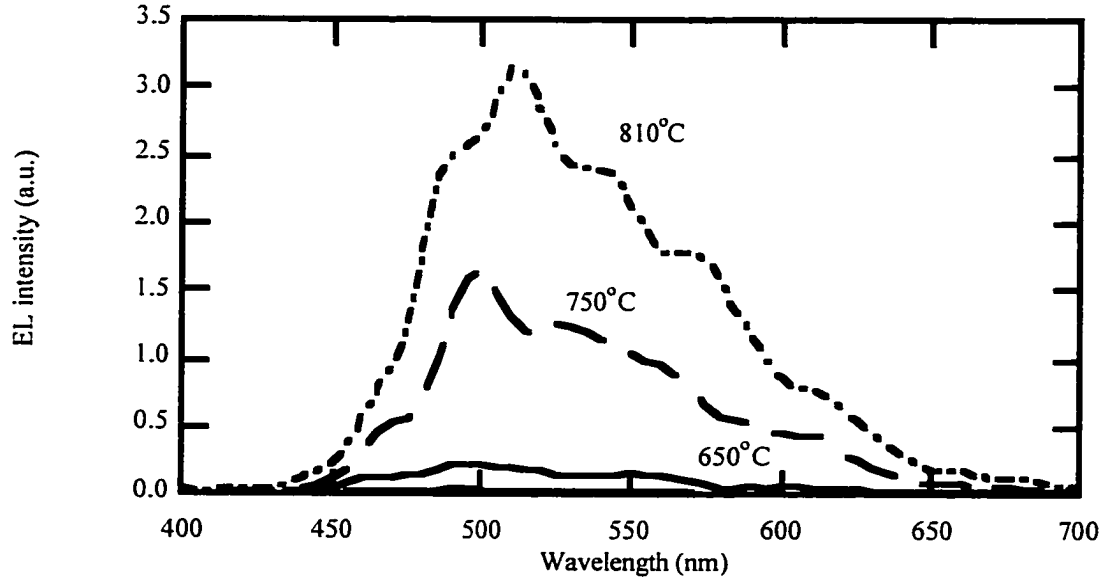


Figure 5-25. Emission spectra of Ga_2S_3 doped SrS:Ce TFEL devices as a function of post deposition annealing temperature

Table 5-11. CIE coordinates measured for Ga_2S_3 doped SrS:Ce TFEL devices.

Annealing Treatment	Peak Emission Wavelength (nm)	CIE Coordinates (x,y)
As-Deposited	480	(.24,.39)
650°C/120s	480	(.23,.37)
750°C/120s	485	(.24,.44)
810°C/120s	500	(.26,.48)

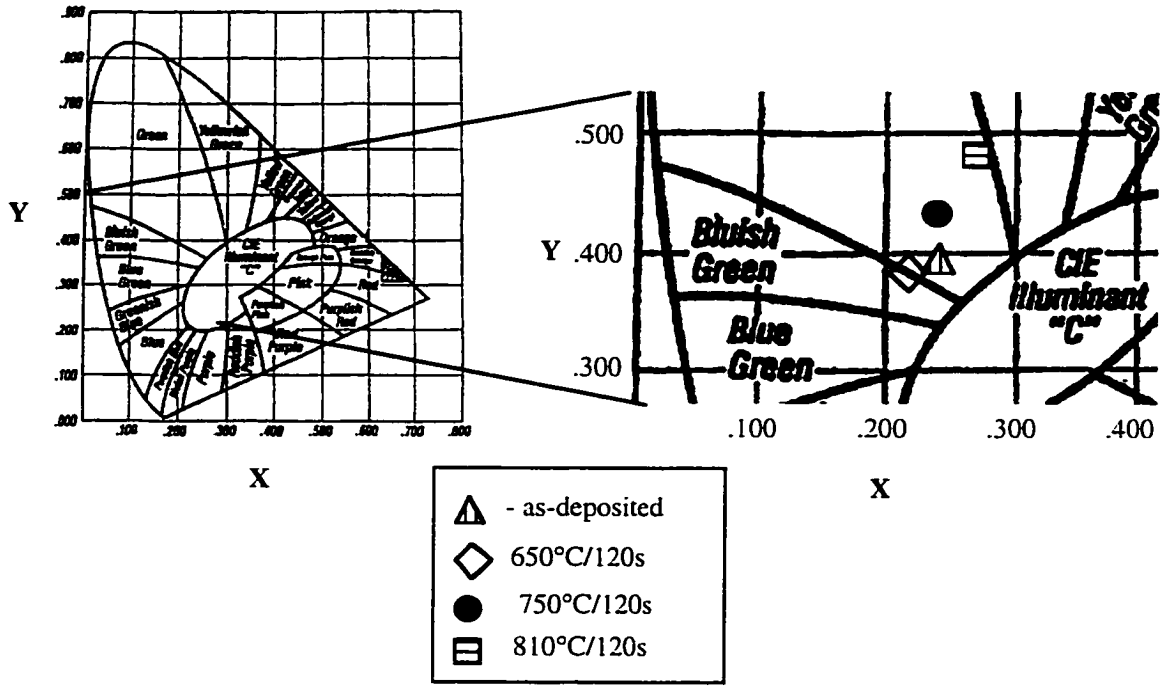


Figure 5-26. CIE diagram with the CIE coordinates for the annealed multi-layer devices

Microstructural Characterization

Post deposition annealing led to a significant improvement in EL properties of the Ga_2S_3 doped SrS:Ce TFEL devices. As reported earlier, annealing resulted in significantly changing the microstructure of the phosphor layer in the double layer and multi-layer TFEL devices. In order to better understand the effect of the Ga_2S_3 incorporation into the SrS:Ce sputter target on the microstructure of the phosphor layer microstructure, XRD, SIMS and TEM analysis were performed. The results from these analyses are presented below.

X-Ray diffraction

The results from the XRD analyses performed on the Ga_2S_3 doped SrS:Ce TFEL devices are listed in Table 5-12, 5-13, 5-14 and 5-15. The Ga_2S_3 doped SrS:Ce phosphor films, regardless of the annealing condition, were textured with a preferred (200) crystallographic orientation. The FWHM of the (200) peak decreased with increasing annealing temperature as shown in Figure 5-27.

Table 5-12. XRD summary table for an as-deposited Ga_2S_3 doped SrS:Ce TFEL device.

Angle	D-Spacing	Intensity	Peak
29.4825	3.0273	100	SrS (200)
30.3575	2.9420	29.13	ITO
25.4275	3.5001	22.89	SrS (111)
42.0825	2.1454	22.25	SrS (220)

Table 5-13. XRD summary table for a Ga_2S_3 doped SrS:Ce TFEL device annealed at 650°C/120s.

Angle	D-Spacing	Intensity	Peak
36.3050	2.4725	100	ITO
39.1825	2.2973	51.72	ITO
29.6850	3.0071	35.35	SrS (200)
42.4475	2.1278	15.40	SrS (220)

Table 5-14. XRD summary table for a Ga_2S_3 doped SrS:Ce TFEL device annealed at 750°C/120s.

Angle	D-Spacing	Intensity	Peak
29.6325	3.0123	100	SrS (200)
36.2525	2.4760	14.94	ITO
39.1325	2.3001	7.45	ITO
61.5975	1.5044	6.92	SrS (400)

Table 5-15. XRD summary table for a Ga_2S_3 doped SrS:Ce TFEL device annealed at 810°C/120s.

Angle	D-Spacing	Intensity	Peak
29.6725	3.0083	100	SrS (200)
32.9525	2.,7160	10.15	ITO
61.5925	1.5045	7.63	SrS (400)
36.3025	2.4727	7.30	ITO

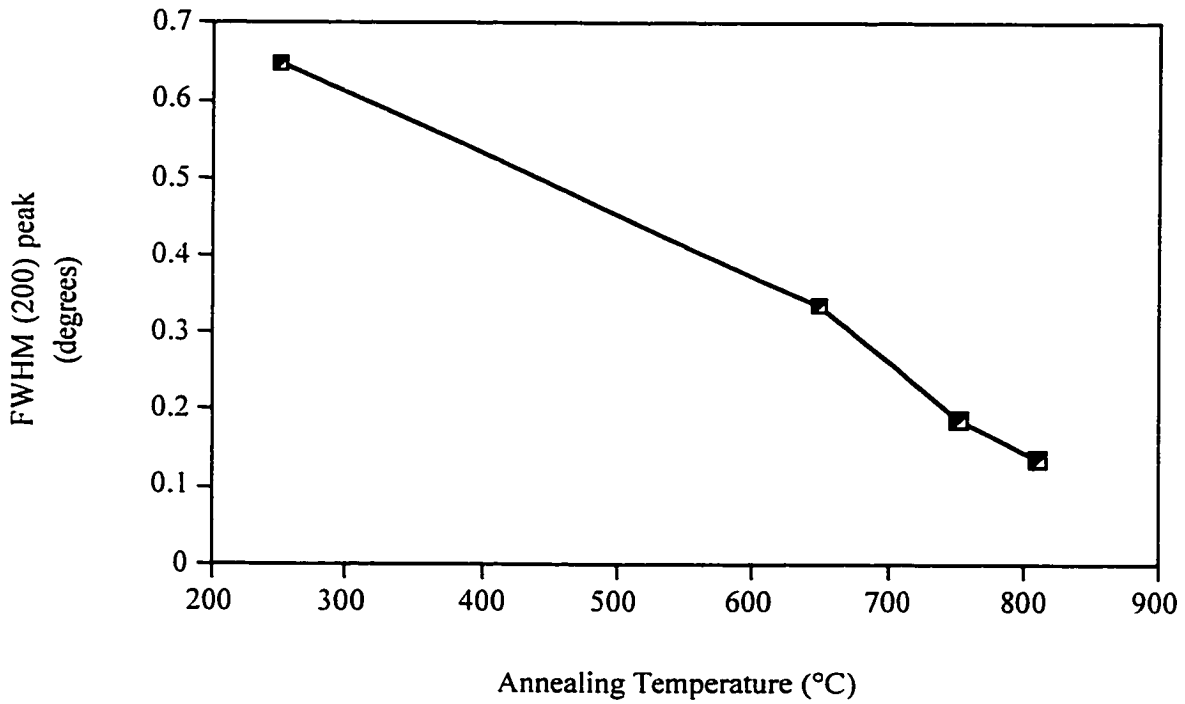


Figure 5-27. FWHM of the SrS (200) peak as a function of post deposition annealing temperature

SIMS

SIMS analysis was performed on the as-deposited and 810°C annealed phosphor layers of the Ga_2S_3 doped SrS:Ce TFEL devices. The SIMS profiles, given in Figure 5-28, indicated a significant change in the gallium and cerium signals as a result of annealing. Both profiles show that the levels of strontium and sulfur remain constant throughout the phosphor layer. These results agree with the SIMS analyses performed on the phosphor layers of the double layer and multi-layer TFEL devices. These SIMS results suggested that the migration of gallium may play a critical role in the observed change in grain morphology and grain size as a result of post deposition annealing.

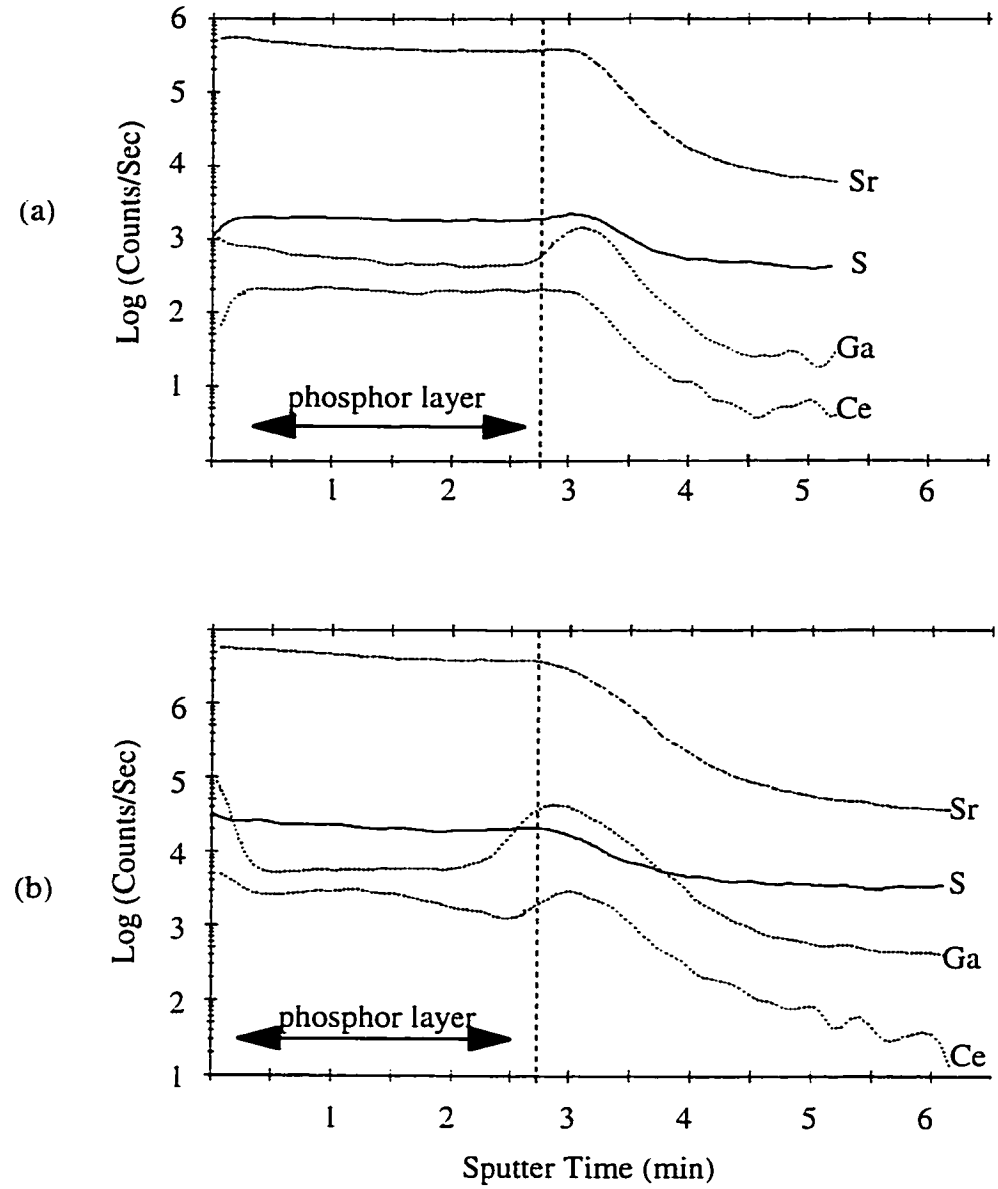
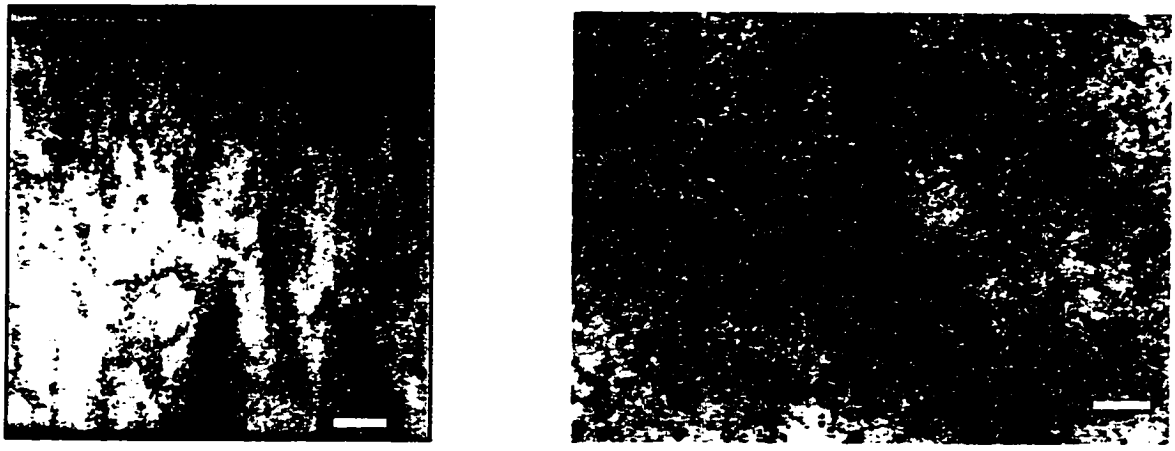


Figure 5-28. SIMS profiles of the phosphor layer in an (a) as-deposited and (b) 810°C annealed Ga_2S_3 doped SrS:Ce TFEL device

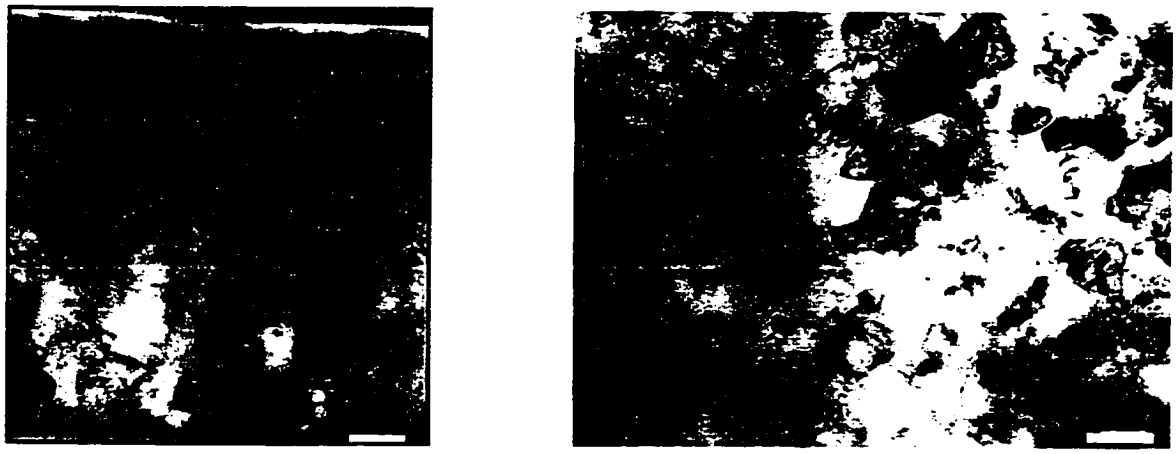
TEM

TEM micrographs of the as-deposited Ga_2S_3 doped SrS:Ce TFEL device are presented in Figure 5-29. The as-deposited structure clearly shows a columnar grain morphology. The as-deposited phosphor layer is composed of small diameter columnar grains with an average column diameter of 400 ± 150 Å. The effect of annealing at 750°C for 120s is shown in the set of TEM micrographs in Figure 5-30. It is evident from these micrographs that grain growth had occurred and a transformation in grain morphology from columnar to equiaxed had already begun to take place. The mean grain diameter for these samples was 900 ± 300 Å. Like the multi-layer films, Ga_2S_3 doping of the SrS:Ce led to a homogenous equiaxed grain morphology in the 810°C annealed samples. As seen in the set of TEM micrographs shown in Figure 5-31, significant grain growth had taken place as a result of the 810°C anneal. The 810°C annealed resulted in equiaxed grains with a mean grain size of 5100 ± 1200 Å. Grain size measurements were made from plan view TEM micrographs. The mean grain size of the SrS:Ce grains increased with increasing post deposition annealing temperature as seen in Figure 5-32. Unlike in the transformed region of the double layer and through the phosphor layer of the multi-layer devices annealed at 810°C, no voids were seen in the phosphor layer of the Ga_2S_3 doped SrS:Ce TFEL devices annealed at 810°C.



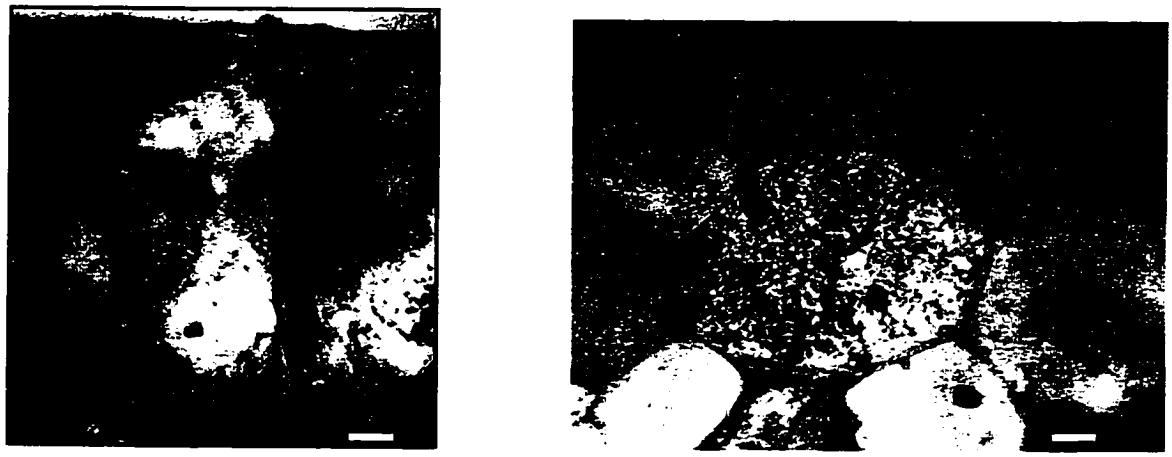
(a) (b)

Figure 5-29. TEM micrographs of an as-deposited phosphor layer in Ga_2S_3 doped SrS:Ce TFEL device (a) cross-sectional view and (b) plan view (the inserted white bar represents 1200Å in both micrographs)



(a) (b)

Figure 5-30. TEM micrographs of the phosphor layer annealed at 750°C/120s in Ga_2S_3 doped SrS:Ce TFEL device (a) cross-sectional view and (b) plan view (the inserted white bar represents 1200Å in both micrographs)



(a) (b)

Figure 5-31. TEM micrographs of the phosphor layer annealed at 810°C/120s in Ga_2S_3 doped SrS:Ce TFEL device (a) cross-sectional view and (b) plan view (the inserted white bar represents 1000Å in both micrographs)

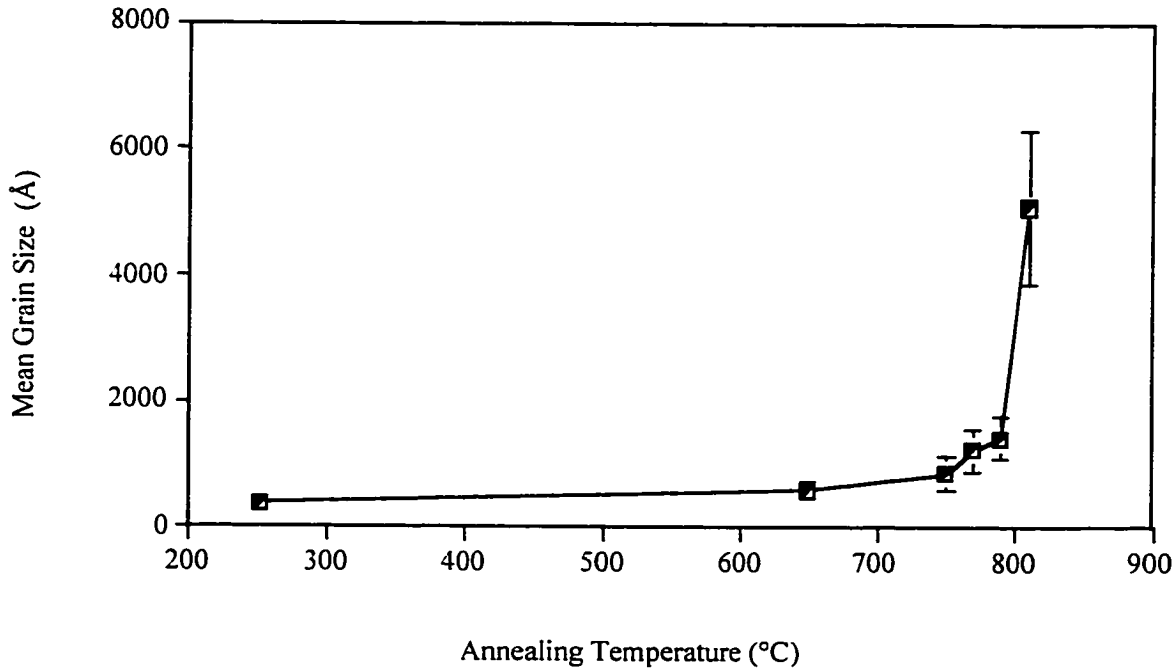


Figure 5-32. SrS:Ce grain size as a function of post deposition annealing temperature for Ga_2S_3 doped SrS:Ce TFEL devices

Discussion

Post deposition annealing at 810°C of the TFEL devices containing SrS:Ce phosphor films with gallium and excess sulfur resulted in enhanced EL performance. The factors responsible for the improvement in the electrical and optical properties will be discussed collectively for the double layer, multi-layer and Ga_2S_3 doped SrS:Ce TFEL devices. A discussion of the effects of annealing on the microstructure of the different phosphor layers will follow. The role that gallium and excess sulfur play in the increased SrS:Ce grain size and transformation to a equiaxed grain morphology will be included. Lastly, the role of the phosphor layer microstructure on the improved EL brightness and efficiency will be discussed.

Threshold Voltage

The threshold voltage for all the devices studied decreased with increased post deposition annealing temperature, as seen in Figure 5-33. As discussed in chapter 4, the reduction of the threshold voltage with annealing has been attributed to the increased electrical conductivity of the phosphor layer due to improved crystallinity [Oka93], [Hir89].

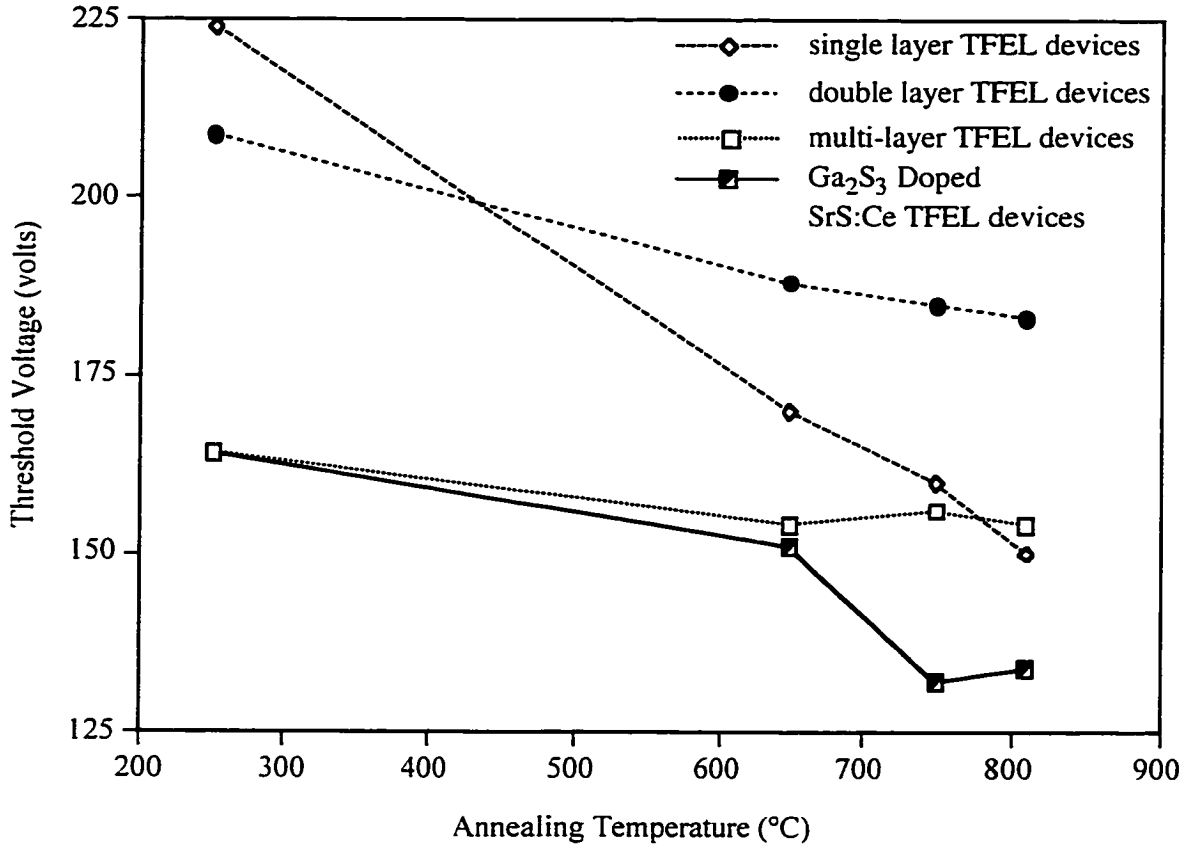


Figure 5-33. Threshold voltage as a function of post deposition annealing temperature for the different TFEL devices studied

The threshold voltage of the Ga_2S_3 doped SrS:Ce TFEL device was 16 volts lower than that of the single layer TFEL device (annealed at 810°C for 120s). This reduction in threshold voltage may be attributable to either improvement in crystalline quality or to the excess sulfur in the Ga_2S_3 doped SrS:Ce TFEL devices. As previously mentioned in chapter 2, annealing in a sulfur ambient improved TFEL device properties [Ohm95], [Oni88]. The investigators proposed that addition of sulfur resulted in improved crystallinity. Using x-ray FWHM values as a measure of crystallinity, the FWHM of the SrS (220) reflection in the Ga_2S_3 doped SrS:Ce TFEL devices is narrower than that of the

FWHM of the SrS (220) reflection in the single layer TFEL device. Additionally, the excess sulfur added to the films could result in a reduction in the number of sulfur vacancies ultimately resulting in an increase in the phosphor layer conductivity [Hir89].

The reason for the relatively large threshold voltage measured for the double layer devices is unclear. The heterogeneity of the microstructure along with presence of voids in the transformed region may play a role in lowering the phosphor layer conductivity and thus resulting in a higher threshold field. The presence of spherical voids in the phosphor layer of the multi-layer TFEL devices could result in the higher threshold voltages compared with the Ga_2S_3 doped SrS:Ce TFEL devices.

Brightness and Luminous Efficiency

The L_{40} value for the different devices as a function of post deposition annealing temperature is plotted in Figure 5-34. It is clear that increased post deposition annealing temperature resulted in an increase in L_{40} for the devices studied. As discussed earlier, previous studies have attributed the increase in brightness with post deposition annealing on the increase in crystalline quality [Ohm95], [Oko93]. The L_{40} values for all devices studied are comparable between the as-deposited, the 650°C and the 750°C anneals. The addition of gallium and excess sulfur resulted in a significant increase in L_{40} as a result of the 810°C anneal. The increase in brightness of the phosphor films annealed at 810°C correlated with the amount of gallium and excess sulfur added to the SrS:Ce films. The L_{40} of the Ga_2S_3 doped SrS:Ce TFEL device annealed at 810°C for 120s was approximately five times that of the L_{40} of the 810°C annealed single layer TFEL device.

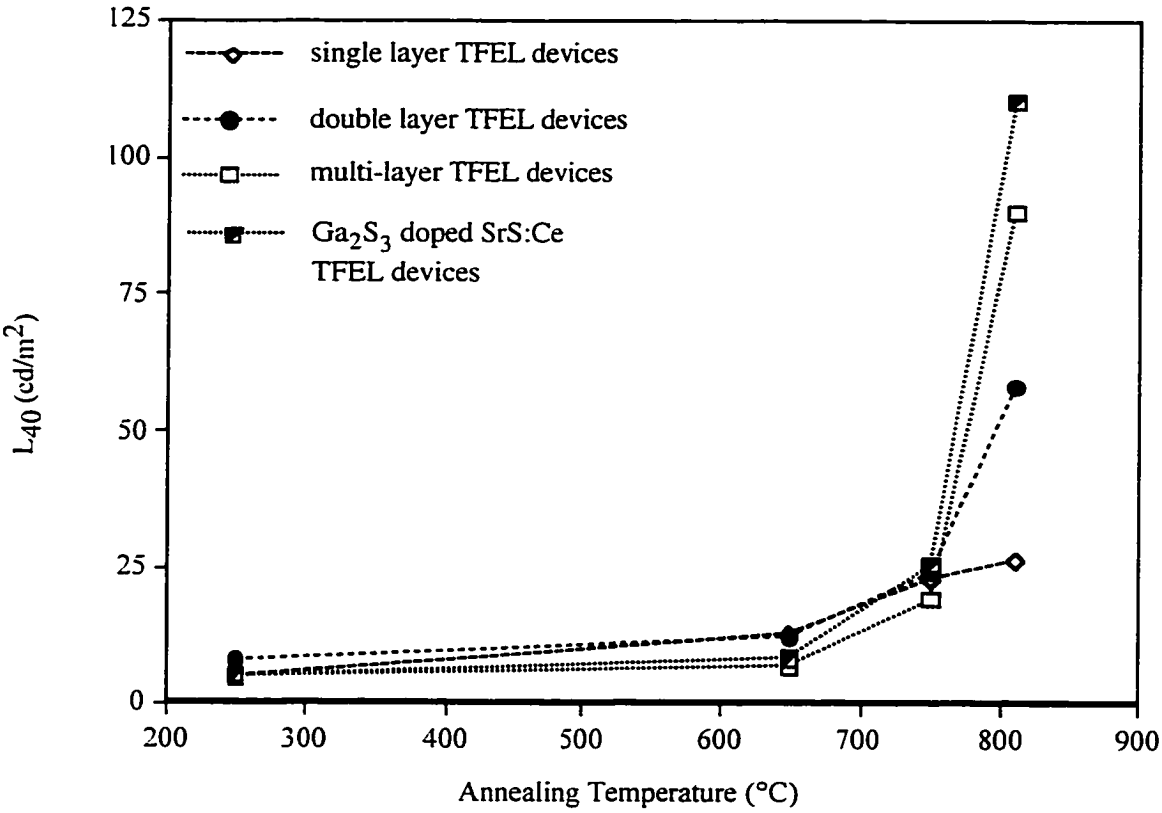


Figure 5-34. L_{40} as a function of the post deposition annealing temperature for the TFEL devices studied

The effect of post deposition annealing temperature on the luminous efficiency of the various TFEL devices studied is plotted in Figure 5-35. The higher annealing temperatures resulted in significantly increased luminous efficiencies. It should be noted that the largest increase in the L_{40} and luminous efficiency values for the gallium containing devices is seen between the 750 °C and 810 °C anneals. The addition of gallium and excess sulfur resulted in a significant increase in the luminous efficiency as a result of the 810°C anneal. The increase in luminous efficiency of the phosphor films annealed at 810°C correlated with the amount of gallium and excess sulfur added to the

SrS:Ce films. The luminous efficiency of the Ga_2S_3 doped SrS:Ce TFEL device annealed at 810°C for 120s was approximately six times greater than that for the similarly annealed single layer TFEL device. The rapid increase in the L40 and luminous efficiencies suggest that annealing at 810°C had resulted in a dramatic increase in the crystalline quality of the phosphor layer.

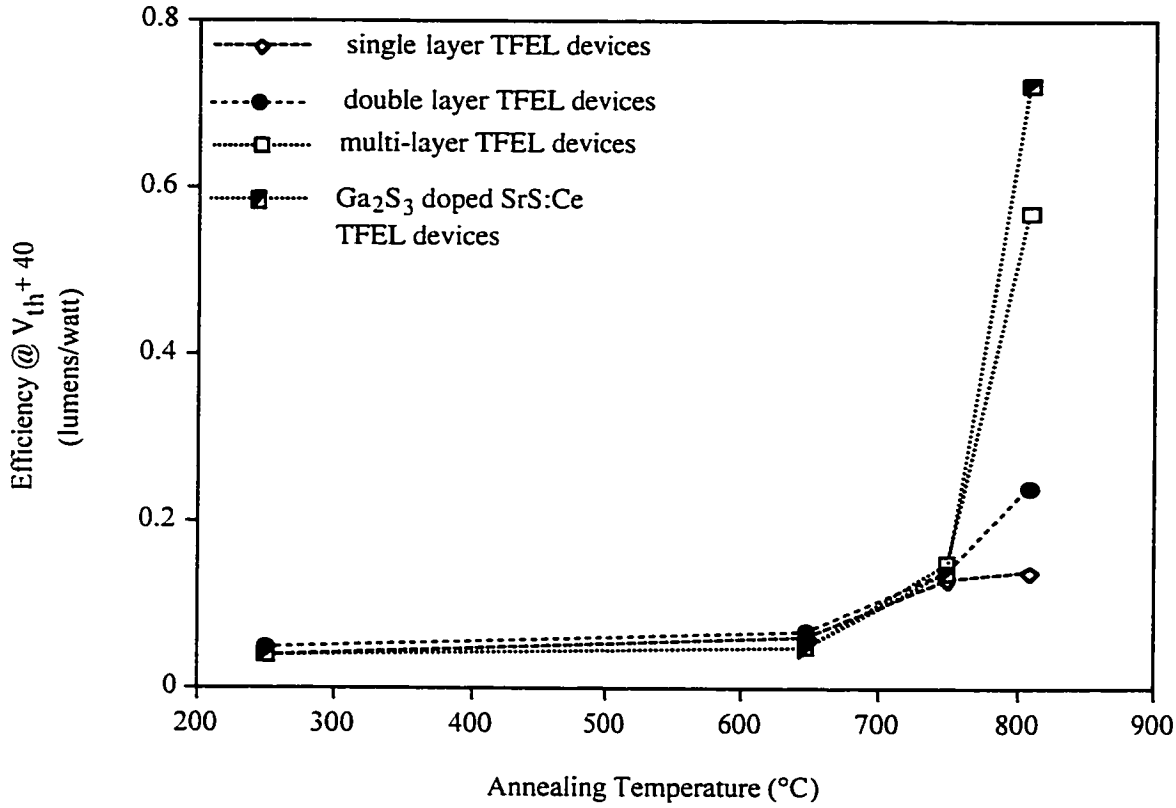


Figure 5-35. Luminous efficiency (at the threshold voltage + 40 volts) as a function of the post deposition annealing temperature for the TFEL devices studied

Emission Spectra

The change in emission spectra due to the addition of gallium and excess sulfur to the SrS:Ce phosphor layer is shown in Figure 5-36. The emission spectra plotted are from devices that were annealed at 810°C for 120s. The peak emission shifted

to higher wavelengths, i.e., green shifted as a result of addition of Ga_2S_3. A possible reason for this shift is proposed by Warren et al. [War97]. Using electron paramagnetic resonance, the investigators determined that the density of Ce^{3+} sites and Ce^{3+} sites associated with a strontium vacancy (Ce^{3+}-V_{Sr}) sites. While light emission is possible from both sites, i.e., both sites are EL active, emission from a Ce^{3+} associated with a strontium vacancy could lead to a green shift since it is a lower symmetry site than the isolated nearly-cubic Ce^{3+} site [Hut96]. The density of Ce^{3+}-V_{Sr} sites was three times higher in the Ga_2S_3 doped SrS:Ce films than in the SrS:Ce films. The authors suggest that the formation of the Ce^{3+}-V_{Sr} complex in the Ga_2S_3 doped SrS:Ce films could be responsible for the observed green shift.

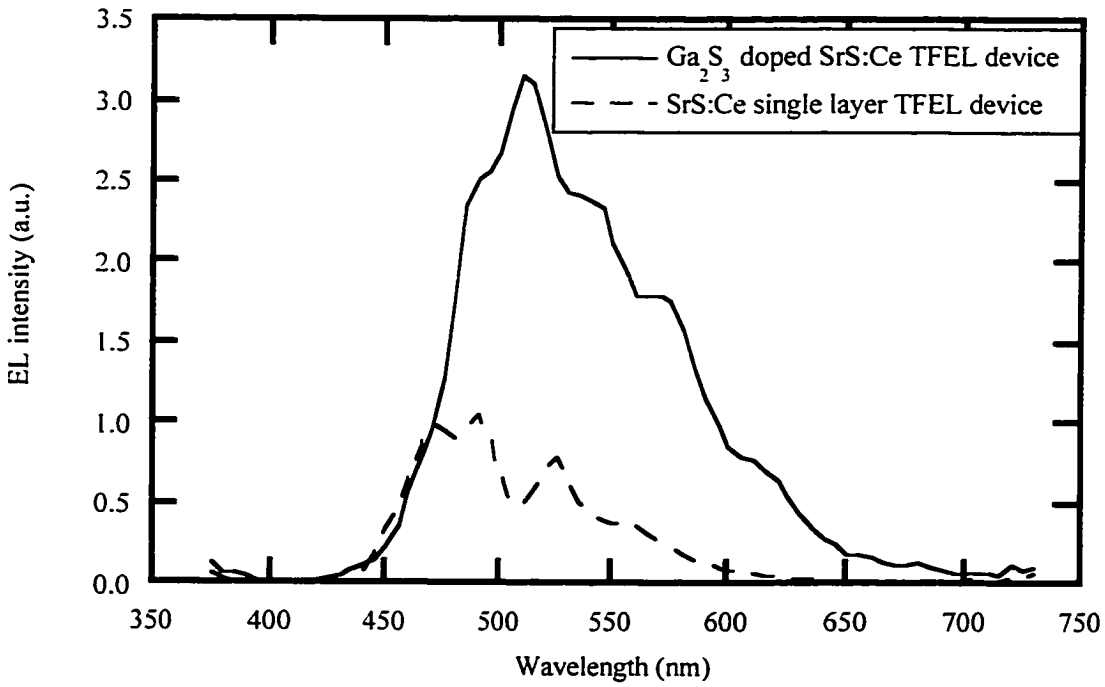


Figure 5-36. Emission spectra from Ga_2S_3 doped SrS:Ce and single layer TFEL devices annealed at 810°C

Crystalline Quality

The crystalline quality, as measured by XRD, is a measure of the amount of strain in a thin film. Strain in a thin film can be a result of the non-equilibrium deposition conditions associated with film growth. In order to accommodate the inherent strain, defects such as dislocations are generated. The same defects which can act as sites for non-radiative recombination resulting in decreased luminescence. The presence of strain results in broadening of the x-ray diffraction line [Cul78]. The results indicate that post deposition annealing resulted in the increase in crystalline quality of all the phosphor films. This suggests that annealing has reduced the number of crystalline defects and thus improved the local Ce^{3+} crystal field. As seen in Figure 5-37, the FWHM of the (220) peak of the Ga_2S_3 doped SrS:Ce device is narrower than the FWHM of the (220) peak of the single layer TFEL device, regardless of the post deposition annealing temperature. The reduction in the FWHM suggests that the inherent strain induced defect population in the Ga_2S_3 doped SrS:Ce phosphor layer has been further reduced as a result of annealing. This would suggest that the annealing should have resulted in a further improvement in the crystal field of the Ce^{3+} ion in the phosphor layer containing gallium and excess sulfur.

An interesting observation from the x-ray analysis is that no additional significant peaks (relative intensity > 5%) were detected as a result of the addition of gallium and excess sulfur. In the case of the double and multi-layers three possible reasons exist: 1) the amount of thiogallate added may not be detectable, 2) the thiogallate is amorphous in the as-deposited state and remains that way and 3) the thiogallate may be

reacting with the SrS:Ce to form an amorphous phase upon annealing. Preliminary work had indicated that the as-deposited thiogallate transformed from amorphous to crystalline at an annealing temperatures above 700°C. The concentration of thiogallate contained in the double layer films ($V_f \leq 6$ %) and the multi-layers ($V_f \leq 15$%) phosphor films should have been detectable if crystalline. This suggests that the formation of an amorphous phase is most likely.

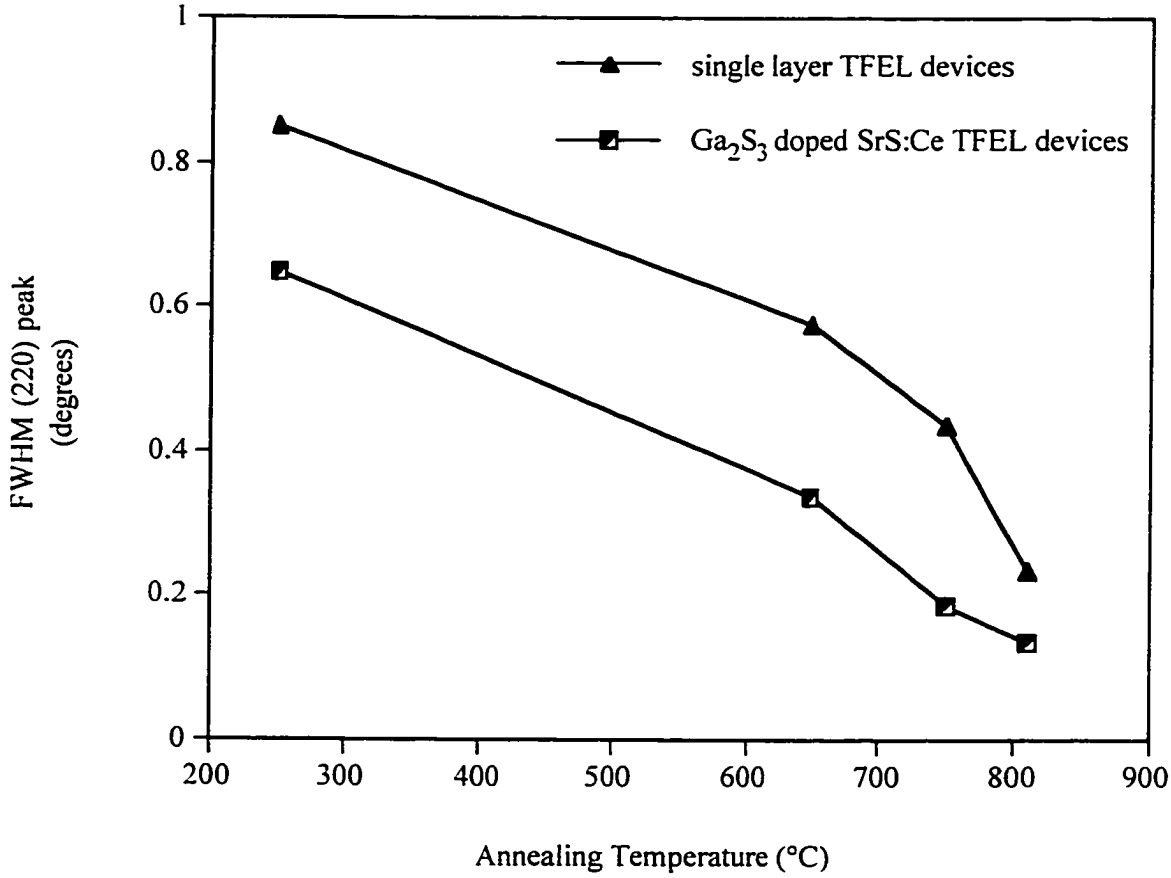


Figure 5-37. FWHM of the (220) peak as a function of post deposition annealing temperature for Ga_2S_3 doped SrS:Ce and single layer TFEL devices

Compositional Analysis

The results of the SIMS analysis performed on the phosphor film of double layer TFEL devices suggest that the gallium in the thiogallate diffused through the SrS:Ce phosphor film as a result of the post deposition annealing. A similar change in the gallium profile is seen in the SIMS analysis of the phosphor film in the multi-layer and Ga_2S_3 doped SrS:Ce TFEL devices. Collectively, these results suggest that gallium, either in elemental form or in the form of a gallium compound is diffusing through the film as a result of post deposition annealing. It is highly unlikely that the gallium is diffusing through as elemental gallium. In order for efficient operation, the capacitance of the phosphor layer should be sufficiently high for high internal field generation. The presence of elemental gallium in the phosphor layer would provide a means for high conductivity paths through the phosphor layer resulting in electrically shorting the device. While the SIMS analysis provides chemical compositional of the phosphor film as a whole, it did not yield information on the exact location of the gallium as it related to the microstructure.

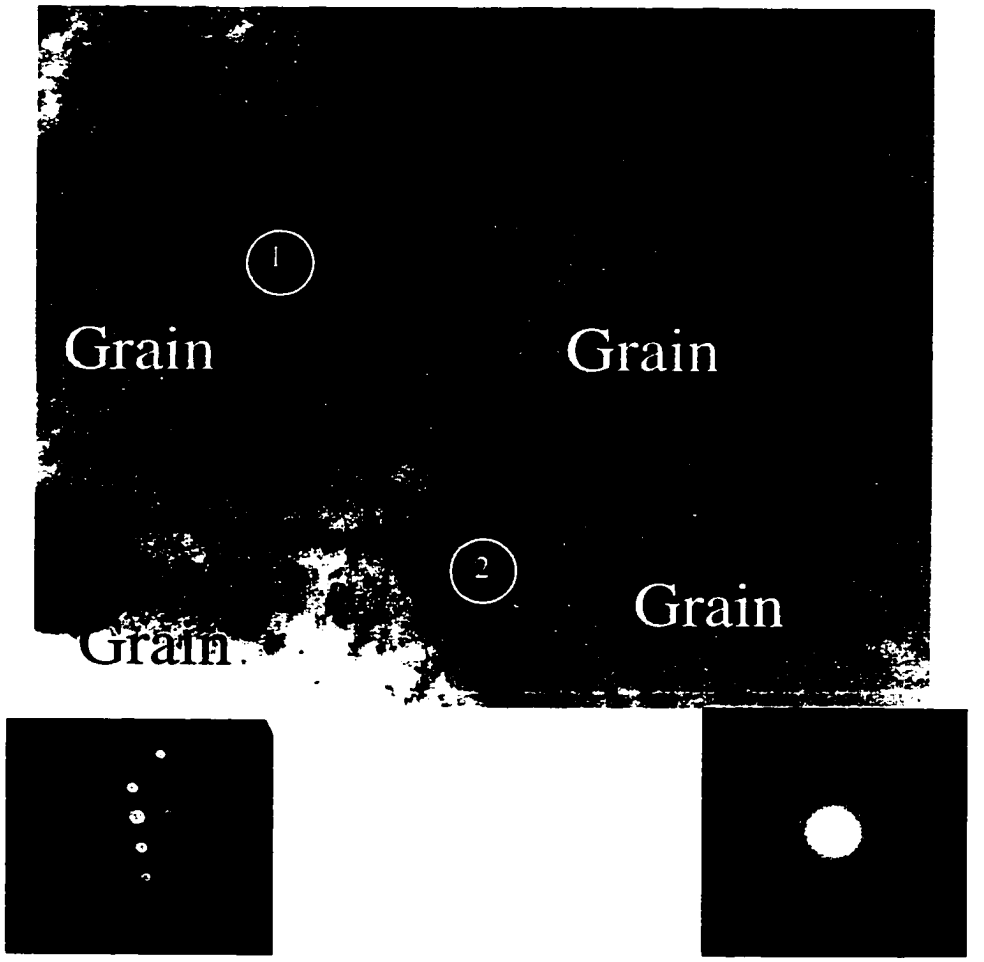
In order to more accurately determine the chemical composition of the grain boundary phase, plan view TEM samples of the phosphor layer from a Ga_2S_3 doped SrS:Ce TFEL devices were examined in a Philips CM200 field emission TEM. The main advantage of a field emission TEM, with respect to this work, is the high probe currents that can be used for chemical analysis via energy dispersive spectroscopy (EDS). Both EDS point and EDS line scans were obtained to determine the chemical composition of the area of interest. EDS data was obtained using 20 Å probe. The EDS line scans were

defined as a series of 40 points along a line, spaced 40 Å apart. The dwell time for EDS acquisition at each point was 0.4 seconds. The small dwell times were used in order to avoid damaging the TEM sample with the electron beam. The EDS data obtained in this experiment should be used to compare the relative differences in composition between the grain and grain boundary region. Small dwell times, specimen drift and x-ray peak overlap are some of the many problems which limit the accuracy of the analysis. The error associated with EDS analysis is routinely between 10 and 15% [Rom92].

A representative region of the phosphor layer, from a Ga_2S_3 doped SrS:Ce TFEL device annealed at 810°C, is shown in the plan view TEM micrograph in Figure 5-38. In this micrograph, the triple point region is denoted by the circled area "2". A diffraction pattern taken from within this triple point region was composed of diffuse rings confirming that it was amorphous in nature. This compares with the diffraction pattern taken from the adjoining grain which was composed of a typical crystalline spot pattern. The absence of lattice fringes in the grain boundary region compared with the adjoining grains in the high resolution TEM (HRTEM), presented in Figure 5-39, confirms the amorphous nature of the grain boundary region.

EDS analysis of several grains and the corresponding triple point regions showed that the grains were virtually gallium free ($C_{Ga} \sim 1$ at. %). Spectra obtained from the triple point regions showed a significant increase in the gallium concentration ($C_{Ga} \sim 30$ at. %). The average chemical composition of several grains and grain boundary triple point regions, determined via EDS analysis, is presented in Table 5-15. As indicated earlier, the values in Table 5-15 are not absolute and are used only to show relative differences in

chemical composition between the grain and grain boundary region. The results of an EDS line scan, acquired through a grain boundary triple point are shown in Figure 5-40. The indicated scan started at point (a) and concluded at point (a'). The profile indicates the amorphous grain boundary phase is significantly enriched in gallium. Similar EDS spot scans taken from the as-deposited Ga_2S_3 doped SrS:Ce sample showed a uniform gallium distribution of approximately 3 at. %, with no observable pockets of segregation.



diffraction pattern from selected area 1

diffraction pattern from selected area 2

Figure 5-38. Plan view TEM micrograph of the phosphor layer from a Ga_2S_3 doped SrS:Ce TFEL device annealed at 810°C with corresponding diffraction patterns from the grain (selected area 1) and the grain boundary region (selected area 2)

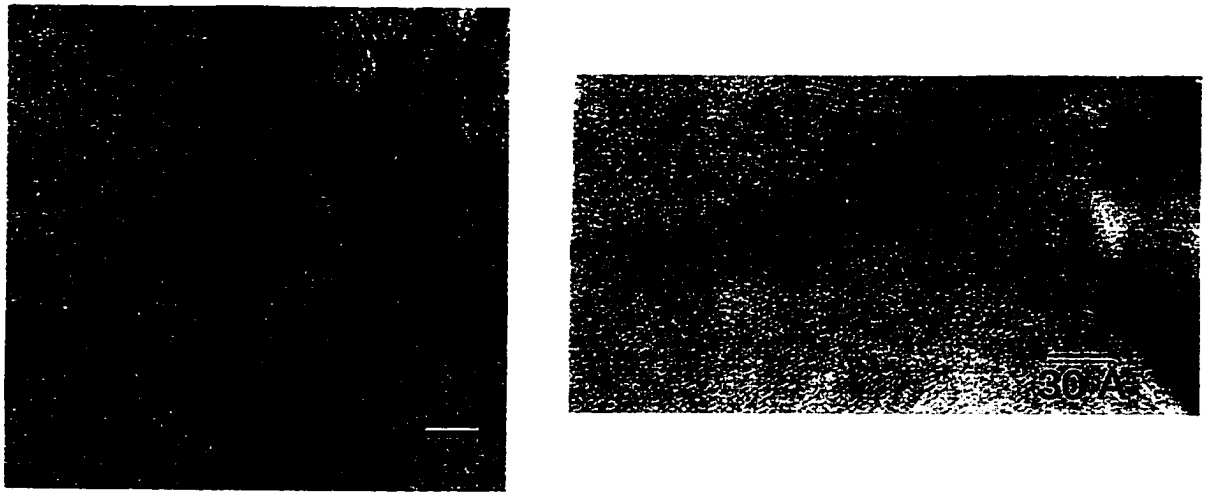
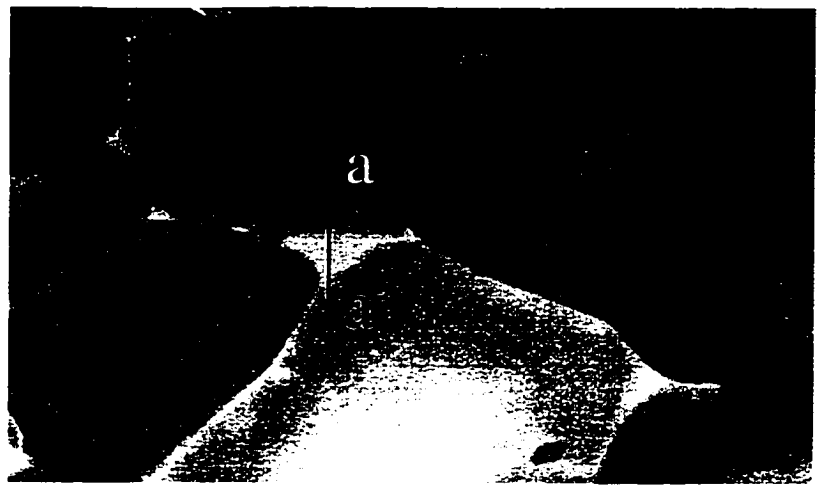


Figure 5-40. HRTEM micrographs of the grain boundary phase in the phosphor layer of a Ga_2S_3 doped SrS:Ce TFEL device annealed at 810°C

Table 5-15. Average compositions of the grains and grain boundary regions in the phosphor layer of a Ga_2S_3 doped SrS:Ce TFEL devices annealed at 810°C obtained via EDS analysis.

Element	Composition in Grain (at.%)	Composition in Grain Boundary Region (at.%)
Strontium	59.42	30.55
Sulfur	37.25	39.30
Gallium	0.91	29.45
Cerium	2.42	0.96



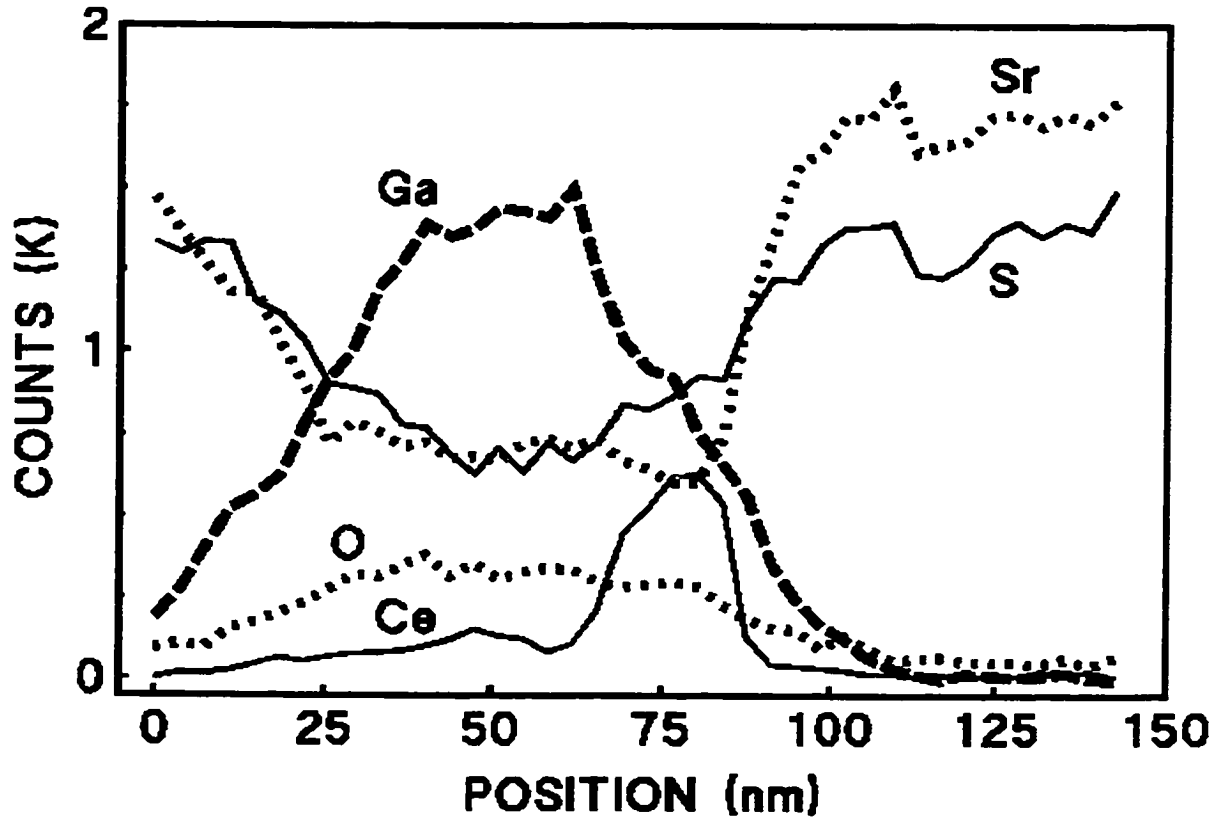


Figure 5-40. Plan view TEM micrograph of the phosphor layer in a Ga_2S_3 doped SrS:Ce TFEL device and the corresponding EDS line scan profile along line a-a'

Grain Growth

The SrS:Ce grain size as a function of post deposition annealing temperature, for all the devices, studied is shown in Figure 5-41. Annealing of the double layer TFEL devices at 810 °C resulted in the transformation in the grain morphology in the top half of the phosphor film. The SIMS results suggested that the migration of gallium was associated with the morphology change. Analysis of the annealed cross section of the phosphor layer in the multi-layer TFEL device confirmed that increased amounts of thiogallate resulted in a complete change in the grain morphology. The mean grain size of the phosphor film in the Ga_2S_3 doped SrS:Ce TFEL devices annealed at 810°C are almost four times as large as the mean grain size of the phosphor film in the single layer TFEL devices. The data shows that the largest increase in the grain size for phosphor films containing gallium and excess sulfur is seen between the 750°C and 810°C anneals. Along with the grain coarsening, a change in grain morphology from columnar to equiaxed was also observed between these two temperatures. In order to better characterize the grain growth observed in the phosphor layer of Ga_2S_3 doped SrS:Ce TFEL devices as a function of temperature, anneals at two additional temperatures were performed: 770°C and 790°C. The inclusion of these two points further narrows the range at which the maximum grain growth occurs to between 790°C and 810°C.

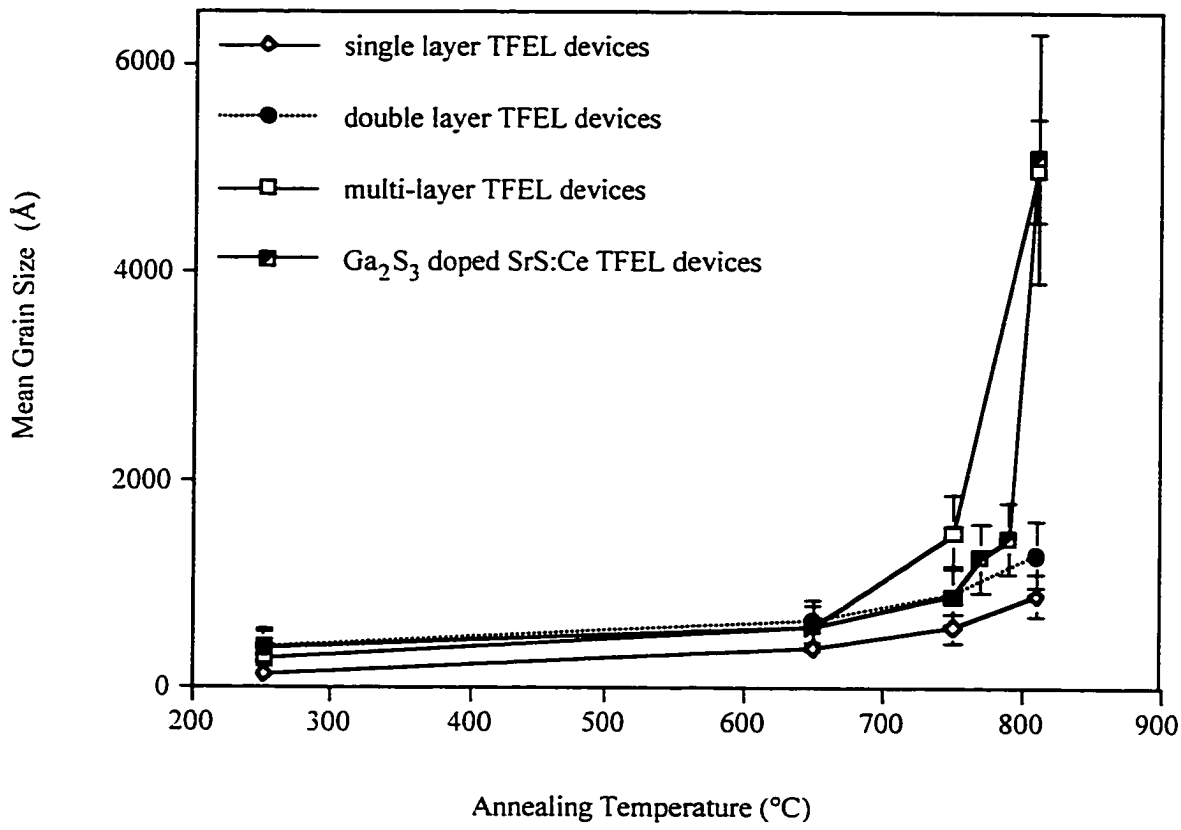


Figure 5-41. Mean SrS:Ce grain sizes as a function of post deposition annealing temperature for the devices studied

The increase in the SrS:Ce grain size between the 750 °C and 810 °C for the multi-layer and Ga_2S_3 doped SrS:Ce TFEL devices suggest that the grain growth process in this temperature regime was different from the process observed for the SrS:Ce films. The data from the microstructural characterization analyses suggest that the enhanced SrS:Ce grain coarsening seen in the phosphor layers of the multi-layer and Ga_2S_3 doped SrS:Ce TFEL devices may be attributable to liquid phase assisted grain growth. SIMS analysis shows the migration of gallium or a gallium containing compound through the SrS:Ce film as a result of annealing. TEM analysis reveals the presence of a gallium rich region at the

grain boundary triple points as well as the amorphous nature of the region which suggest the formation of second phase that segregates to the triple points. The presence of the gallium rich region at the triple points and not along the grain boundaries suggest that uniform wetting of the grains by the low melting phase has taken place. A phase diagram in the SrS-Ga_2S_3 would confirm the thermodynamic plausibility of the existence of a low melting phase, however no such diagram exists. A comparable phase diagram in the CaS-Ga_2S_3 system shows the existence of a low melting eutectic compound between Ga_2S_3 and calcium thiogallate ($CaGa_2S_4$) at 900°C [Yag90].

The low melting phase could enhance the diffusion of the individual atoms during the grain growth process by providing a high diffusivity path. In general, at any temperature, the magnitude of the diffusion through a liquid is much greater than the diffusion through a lattice [Por81]. Previous work in the Al_2O_3 system has shown that the presence of a small amount of liquid phase forming impurities can significantly increase the grain growth rate of alumina [Ben85]. The enhanced grain growth rate attributed to the presence of a liquid phase is also reported in the copper-indium-selenide system [Tut95],[Alb94],[Roc94]. The studies deduced that the large grained film was a product of a liquid-phase assisted growth process in which the liquid phase acts as a fluxing agent for the growth of $CuInSe_2$.

The Effect of Phosphor Layer Microstructure on the EL properties

As discussed in chapter 4, EPR and PL characterization indicated that post deposition annealing led to a more ideal local Ce^{3+} ion environment which was believed to

result in enhanced TFEL device performance. The Ga_2S_3 doped SrS:Ce TFEL devices annealed at 810°C resulted in the best EL properties of all the devices studied. As stated earlier, the increase in gain size of the phosphor layer was found to correlate with the increase in the brightness and efficiency of the TFEL device. Interestingly, the shape of the grain size versus annealing temperature curve for the Ga_2S_3 doped SrS:Ce TFEL devices is the same as the curves for the brightness and luminous efficiency versus annealing temperature. More specifically, the largest increase in the phosphor layer grain size, L_{40} and efficiency all approximately occur between the 750°C and 810°C anneal. This indicates that the increased grain size may have played a significant role in the improved device performance.

As in all the devices studied, post deposition annealing resulted in the reduction in strain. A comparison of the FWHM values for the annealed phosphor layers suggest that the films containing gallium and excess sulfur are less strained than films containing only SrS:Ce (Figure 5-37). Furthermore, the mean grain size in the phosphor layer of the Ga_2S_3 doped SrS:Ce TFEL devices annealed at 810°C was nearly four times as large as the mean SrS:Ce grain size in the single layer TFEL devices. The reduction in grain boundary surface area due to increased grain size correlated well with the increase in EL efficiency between the annealed single layer and Ga_2S_3 doped SrS:Ce TFEL devices.

The calculation of the difference in grain boundary areas between the annealed phosphor films of the Ga_2S_3 doped SrS:Ce and single layer TFEL devices is given in Figure 5-42. For the phosphor film in the single layer device annealed at 810 °C (d_{grain} = 900Å), the total grain boundary area per cubic micron was previously calculated in chapter 4 to be

$2.21 * 10^{-7}$ cm^2. Since the grain morphology of the grains in the phosphor film of the Ga_2S_3 doped SrS:Ce TFEL devices are equiaxed, a slightly different calculation is used to account for the interfacial surface area. The calculation of the grain boundary area involves the calculation of the number of grains that occupy one cubic micron of the phosphor layer. This is equal to dividing the phosphor layer area by the volume of an average equiaxed grain. Using the measured mean grain diameter of 5000 Å, it was found that there are approximately 15 grains/ μm^3. Since all the sides of a grain are shared, the resultant grain boundary surface area associated with a single grain must be divided in half. The total grain surface area per cubic centimeter is then obtained by multiplying the total number of grains by the surface area associated with a single grain. Since the grains are modeled as spheres, the total grain surface area calculated takes into account both the surface area associated with a grain boundary and the surface area associated with the interface. In order to obtain the grain boundary surface area, the interfacial surface area must be subtracted from the total surface area. For the phosphor film in the Ga_2S_3 doped SrS:Ce TFEL device, the total grain boundary area per cubic micron is calculated to be $8.00 * 10^{-15}$ cm^2. Comparing the grain boundary surface areas per cubic micron of phosphor layer, addition of gallium and excess sulfur resulted in a five fold decrease in the grain boundary area.

Calculation of the Total Grain Boundary Area / μm^3 of Phosphor Film

Condition: equiaxed grains (d_{mean} = 5000 Å)

$$\frac{\text{Number of grains}}{\mu m^3} = \frac{1\mu m^3}{\frac{4}{3}\pi r^3} = \mathbf{15.27\ grains}$$

$$\frac{\text{Total Grain Boundary Area}}{\mu m^3} = [\text{Total Grain Surface Area}] - [\text{Total Interface Area}]$$

$$= \left[\left(\frac{\text{grains}}{\mu m^3}\right) \times \left(\frac{4\pi r^2}{2}\right)\right] - [2 \times \text{interface surface area})]$$

$$\frac{\text{Total Grain Boundary Area}}{\mu m^3} = \mathbf{8.00*10^{-15}\ cm^2}$$

Figure 5-42. Calculation of the total grain boundary area / μm^3 of phosphor film in Ga_2S_3 doped SrS:Ce TFEL devices

The five fold decrease in grain boundary volume would suggest that there is a greater concentration of Ce^{3+} ions residing in a more ideal crystalline site i.e., away from the grain boundaries in the phosphor layer of the Ga_2S_3 doped SrS:Ce TFEL device. However, due to the extremely low concentration of Ce^{3+} (0.12 at.%) and the fact that no Ce^{3+} segregation was observed to the grain boundary, a decrease in grain boundary area would have minimal effects on the Ce3+ concentration near or at the grain boundaries. EPR characterization performed on the films confirmed a statistically insignificant

increase in the concentration of EL active Ce^{3+} ions between the annealed phosphor layers of the single layer and Ga_2S_3 doped SrS:Ce TFEL devices [War97].

While the data showed that while the Ce^{3+} EPR line width decreased with increased post deposition annealing temperature, as seen in Figure 5-43, the difference in the Ce^{3+} line width between SrS:Ce phosphor films and those containing gallium and excess sulfur was only 10%. As stated earlier, the Ce^{3+} EPR line width is a measure of the uniformity of the Ce^{3+} crystal field. The EPR confirms the earlier FWHM analysis that suggested that that there was a further reduction of strain in phosphor films containing excess gallium and sulfur. However this improvement can not adequately explain the enhanced luminous efficiencies as a result of the addition of gallium and excess sulfur.

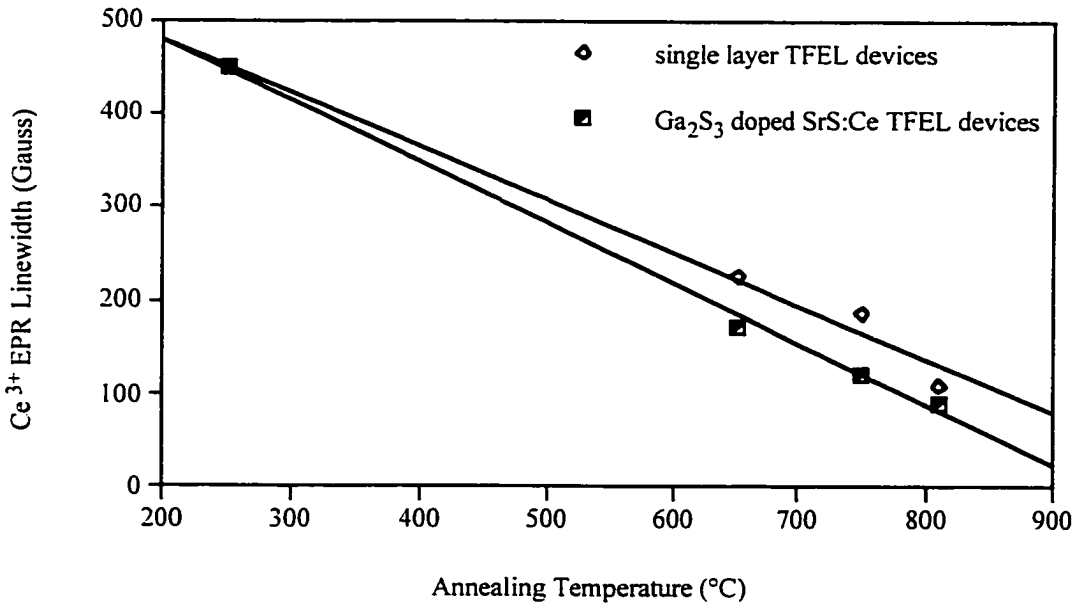


Figure 5-43. Ce^{3+} EPR line width as a function of post deposition annealing temperature for single layer and Ga_2S_3 doped SrS:Ce TFEL devices

The results of PL characterization of the single layer and Ga_2S_3 doped SrS:Ce TFEL devices are shown in Figure 5-44 [Den96]. An effective decay time of 24 ns was obtained for the Ga_2S_3 doped SrS:Ce TFEL device annealed at 810°C from the fluorescent transients. This is greater than the 20 ns decay time obtained for the annealed single layer TFEL devices. The increase in decay time provided further evidence of the reduction in the number of luminescent quenching mechanisms with the addition of gallium and excess sulfur.

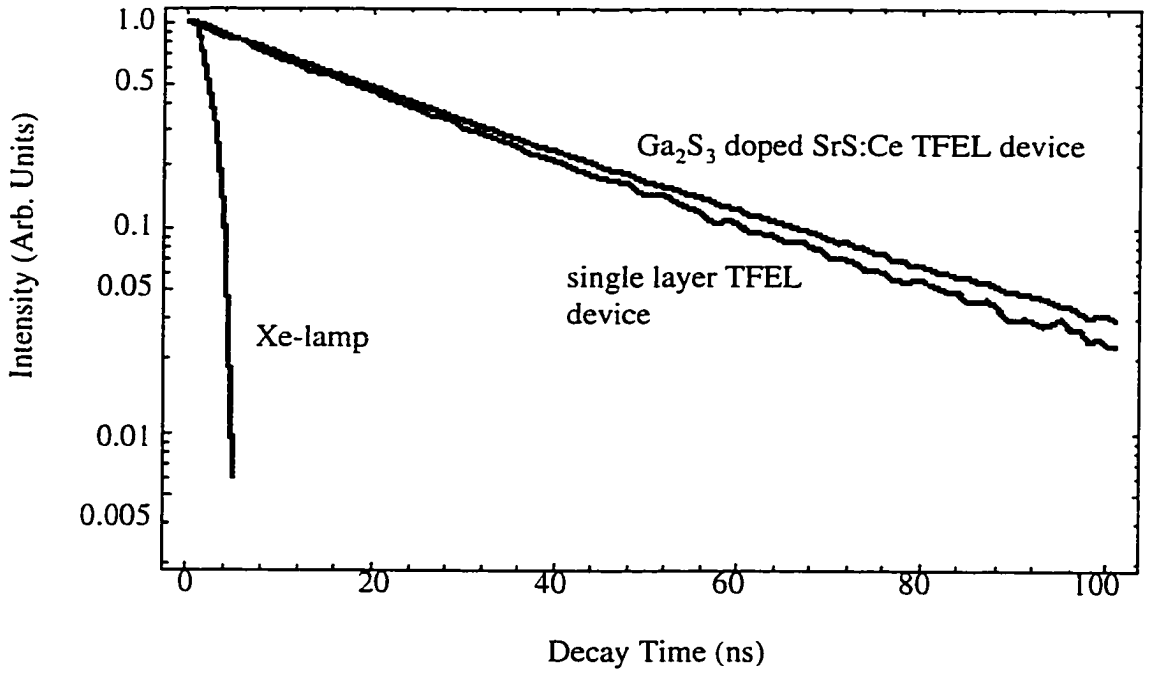


Figure 5-44. Fluorescent transients of annealed single layer and Ga_2S_3 doped SrS:Ce TFEL devices

The improvement in luminous efficiency as a function of annealing can be explained in all of the devices studied via the improvement in crystalline quality of the phosphor layer resulting in an increase in the concentration of EL active Ce^{3+} ions and the reduction in the number of luminescent traps. However, due to the negligible change in EL active Ce^{3+} ion concentration and decay times between the phosphor layers of the single layer and Ga_2S_3 doped SrS:Ce TFEL devices, other explanations are required.

Referring back to the earlier discussion on efficiencies, the observed change in grain size with the addition of gallium and excess sulfur can result in changes to the internal and external luminescent efficiencies.

$$\eta_{internal} = \eta_{hot} \times \eta_{exc} \times \eta_{lum} \qquad (2.4)$$

$\eta_{internal}$ = internal electroluminescence efficiency

η_{hot} = fraction of tunneled electrons hot enough to cause impact excitation

η_{exc} = fraction of centers that undergo impact excitation

η_{lum} = fraction of electrons excited to a higher energy level undergoing radiative decay

As described in the above equation, the internal electroluminescence efficiency is a product of three terms. The reduction in grain boundary area can result in the reduction in scattering of the tunneled electrons thus resulting in an increase in η_{hot}. Grain boundary

scattering of electrons has been attributed in many systems. Assuming that only the nearly cubic Ce^{3+} ions and the Ce^{3+}-V_{Sr} cites can undergo EL excitation, EPR data suggests that the total number of these sites does not change appreciably due to the presence of gallium or excess sulfur. The similar PL decay times suggest that the type of luminescent traps in the phosphor layer are similar after annealing at 810°C, however the increased intensity of the EL emission suggest that there may be far fewer traps in the phosphor films containing gallium and excess sulfur. The reduction in grain boundary area, in the annealed films containing gallium and excess sulfur, could result in the decrease in the number of absorption centers. This mechanism of radiative recombination by defect levels is consistent with the relative difference in the intensity of EL emission between the annealed single layer and Ga_2S_3 doped SrS:Ce TFEL devices.

As mentioned earlier, the total EL efficiency is a product of the internal and external efficiencies. The external efficiency is a measured by degree of amount of light generated in the phosphor layer transmitted through the bottom glass substrate. Scattering of the generated light is responsible for the majority of the light detected through the glass substrate. The ideal wave guide characteristics of TFEL devices ($n_{\text{top dielectric}} < n_{\text{phosphor layer}} > n_{\text{bottom dielectric}}$) result in a need for some scattering in order for any light transmission through the bottom glass substrate. In fact, the light detected in the optical characterization measurements accounts only for that fraction of the generated light transmitted through the glass substrate. A rough measurement of the degree of scattering indicated that Ga_2S_3 doped SrS:Ce TFEL devices reflected 5 times more incident light than the single layer TFEL devices. Coincidentally, the peak EL emission

associated with the 810°C annealed Ga_2S_3 doped SrS:Ce TFEL device (500 nm) corresponds to the mean SrS grain size in the phosphor layer (d_{mean} =5000Å). Due to the presence of the gallium rich phase in between the SrS:Ce grains, the phosphor layer can be modeled as distinct particles in a medium. Under these conditions, scattering of the emitted light is governed by the Rayleigh condition [Kin76]. The Rayleigh condition states that scattering is optimized when the particle size scattering the light is the same as the radiation of the wavelength being scattered. The increase in brightness can also be attributable to the increased scattering of the light generated in the phosphor layer.

CHAPTER 6
CONCLUSIONS AND FUTURE WORK

Post deposition annealing of as-deposited SrS:Ce phosphor thin films resulted in improved TFEL device properties, namely decreases in threshold voltage accompanied by increases in brightness (L_{40}) and luminous efficiency. Microstructural characterization revealed an improvement in crystal quality with increasing annealing temperatures. The narrowing of FWHM of the (220) x-ray diffraction peak showed evidence that annealing led to the elimination of strain induced defects associated with non-equilibrium deposition. Annealing also resulted in grain growth. The average grain size increased from 150 ± 100Å for the as-deposited films to 900 ± 200Å for the films annealed at 810°C for 120s. The effective activation energy for grain growth was calculated to be 0.88 eV. TEM analysis also showed that the grain morphology remained columnar, regardless of the annealing condition. EPR characterization indicated a significant increase in the nearly cubic Ce^{3+} concentration which supported the earlier contention that annealing led to a better Ce^{3+} crystal field. PL studies indicated that annealing led to a significant increase in the luminescent decay time suggesting that traps leading to a quenching were reduced.

Post deposition annealing improved the device properties of the TFEL devices containing SrS:Ce phosphor films with gallium and excess sulfur. XRD analysis showed that the FWHM of the (220) reflection in the Ga_2S_3 doped SrS:Ce phosphor layer narrowed with increased annealing temperatures. This suggests that the inherent strain

induced defect population in the phosphor layer was further reduced as a result of annealing. TEM analysis showed that microstructure of the phosphor layer of the SrS:Ce containing gallium and excess sulfur annealed at 810°C was significantly different. The mean grain size was measured at 5000Å with a change in grain morphology from columnar to equiaxed. The grain coarsening was attributed to the formation of a low melting point phase which acted as a flux to grain growth.

EPR and PL characterization showed that post deposition annealing of the phosphor films resulted in the improvement in the local Ce^{3+} crystal field which resulted in an increase in the concentration of nearly cubic Ce^{3+} ions. However, a comparison of the nearly cubic Ce^{3+} ion concentration in the Ga_2S_3 doped SrS:Ce phosphor layer and SrS:Ce phosphor layer showed very little change. The PL fluorescent transients also showed very little change in the decay times of the Ce^{3+} emission between the annealed films. This suggested that the significant increase in EL device properties can not be attributable to increased amount of nearly cubic Ce^{3+} ions. Rather two other effects need to be considered. The significant difference in mean grain size resulted in a six fold decrease in grain boundary area. These grain boundaries can introduce defect states into the band gap of the SrS host lattice. These defect sites can act as radiative decay sites resulting in lowered EL luminescence. Finally, the increased brightness and luminous efficiency can be attributed to increased scattering of the generated light. The mean grain size in the annealed Ga_2S_3 doped SrS:Ce phosphor layer was equal to the peak emission wavelength. The mean grain size satisfies the condition for Rayleigh scattering where scattering is optimized when the particle size is equal to the wavelength of the emitted radiation.

While this research showed the effect of annealing on the grain size and the EL properties of thin film phosphors, the exact mechanism by which the property enhancement occurs is still unclear.

To calculate the relative absorption in the films, absorption measurements can be taken from large grained and small grained films with similar FWHM. This would ensure measuring the maximum contribution of the grain boundary phase to the absorption. Care would also to use light of an equivalent wavelength of the peak emission.

In order to eliminate the effect of scattering, the phosphor film would be excited under PL excitation conditions in an integrating sphere. The use of an integrating sphere would eliminate the effects of light guiding since , theoretically , all the light emitted should be accounted for. The total PL excitation emission intensity would be measured and if the PL intensity were roughly the same, then scattering could not be ruled out as a possible reason for the increased brightness.

Lastly, in order to reduce the optimum annealing temperatures, substitution of germanium sulfide (GeS_2) for Ga_2S_3 would be investigated. If the grain coarsening is attributable to a liquid phase, then it would interesting to investigate whether the same coarsening would occur in the presence of a lower melting phase. The melting point of Ga_2S_3 is approximately 1100 °C whereas the melting point of GeS_2 is 600 °C. Both sulfide belong to the chalcogenide family and are classified as glass formers. Other systems in which Ga_2S_3 has been substituted for by GeS_2 has shown a decrease in the eutectic phase formation.

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BIOGRAPHICAL SKETCH

Ananth Naman was born in Dhanbad, India, on October 5, 1970. His family immigrated to the United States in 1976. He graduated high school in 1986 and matriculated to Boston University. After the completion of his freshman year, he transferred to the University of Florida. He received his Bachelor of Science degree in Materials Science and Engineering in May of 1990. After a year off, he started his master's research under the guidance of Dr. J.J. Mecholsky and Dr. K.A. Anusavice in 1991. He received his Master of Science degree in Materials Science and Engineering in May of 1994. The title of his masters thesis was "The Effect of Crystallinity on the Fracture Toughness and Fractal Dimension of Lithia Disilicate Glass Ceramics." He started his doctoral research with Dr. K.S. Jones in January of 1994. After the completion of his Ph.D. degree requirements, Mr. Naman will join the wafer product development group at Seagate Technologies in Minneapolis, Minnesota.

I certify that I have read this study and that in my opinion it conforms to acceptable standards of scholarly presentation and is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy.

Kevin S. Jones, Chairman
Professor of Materials Science and Engineering

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This dissertation was submitted to the Graduate Faculty of the College of Engineering and to the Graduate School and was accepted as partial fulfillment of the requirements for the degree of Doctor of Philosophy.

December 1997

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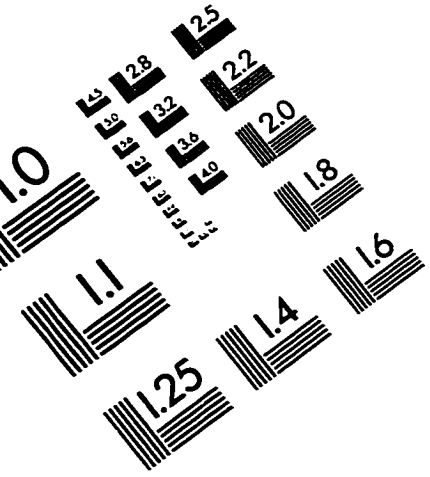
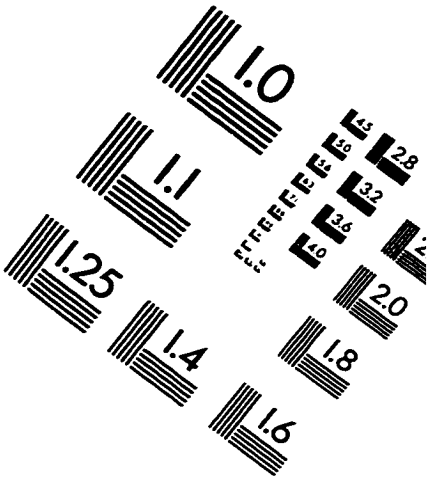
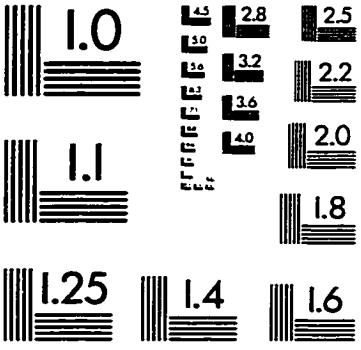
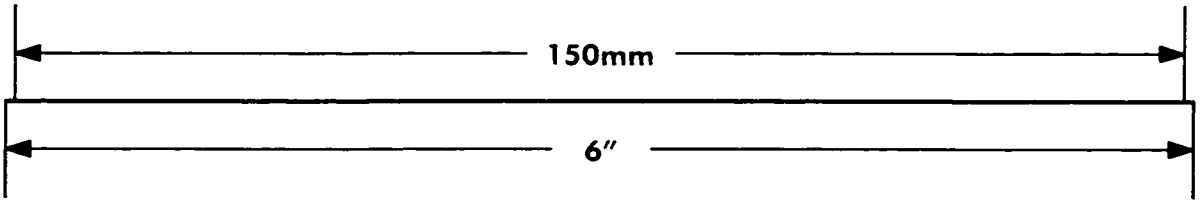
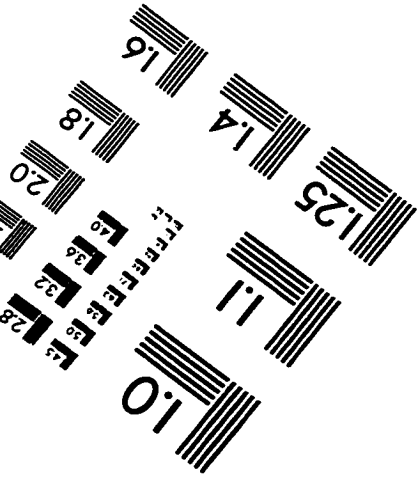
IMAGE EVALUATION TEST TARGET (QA-3)

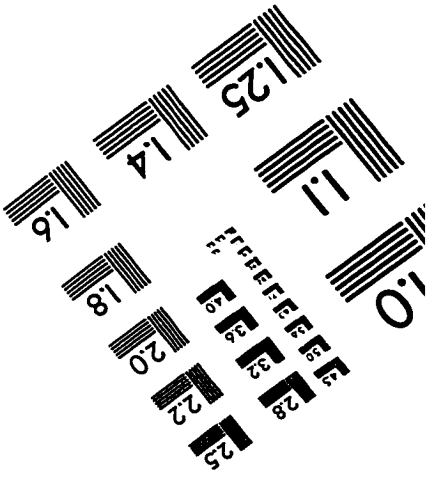












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